User's Guide
SLVU357–March 2010

Using the TPS650001/3/6 2.25 MHz Step-Down Converter with Dual LDO

The TPS650001/3/6 is a single chip Power Management ICs for portable applications. The device combines a single step-down converter with two low dropout regulators. The step-down converter enters a low power mode at light load for maximum efficiency across the widest possible range of load currents. For low noise applications the device can be forced into fixed frequency PWM mode. The step-down converter allows the use of a small inductor and capacitors to achieve a small solution size. The step-down converter has Power Good status output that can be used for sequencing. The LDOs are capable of supplying 300mA and can operate with an input voltage range between 1.6V and 6.0V, allowing them to be supplied from the step-down converter or directly from the main battery. The step-down converter and the LDOs have separate voltage inputs and enables, allowing for design and sequencing flexibility.

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1 Introduction

1.1 Applications

- Point of Load
- Embedded Processor Power
- Cell Phones, Smart-phones
- PDAs, Pocket PCs
- Portable Media Players

1.2 Features

- Input Voltage Rating : 2.3-V up to 6.0-V
- Output Voltages of DCDC converter and LDOs internally fixed (see Table 1)
- Output Current Rating 600-mA (DCDC converter) / 300-mA (LDOs)
- Spread Spectrum Clock (SSC) for best EMI performance
- 2.25-MHz Switching Frequency
- 16 pin 3mm × 3mm QFN package

Table 1. TPS650001/3/6 Output Voltage Specifications

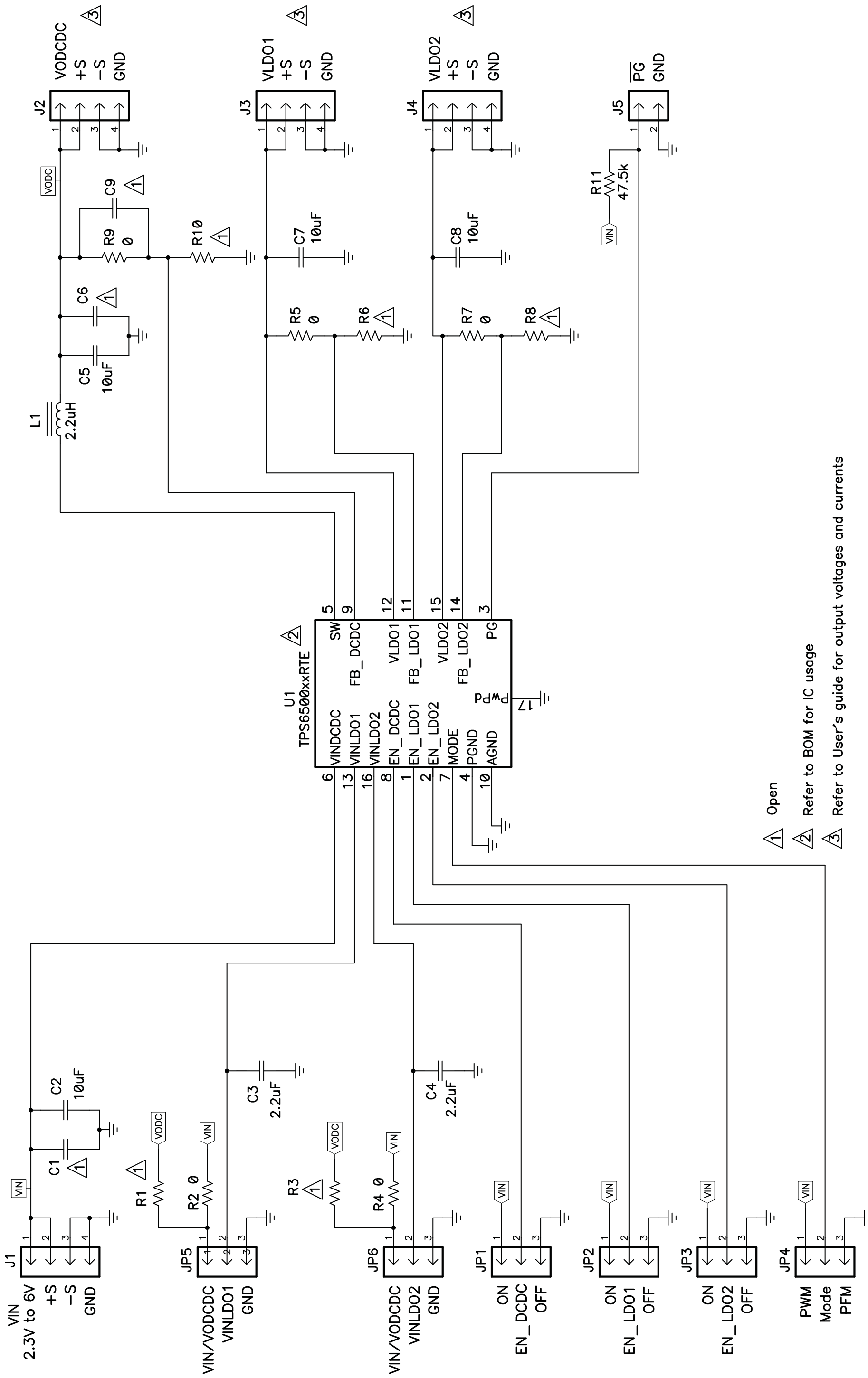
	VOUTDCDC	VLDO1	VLDO2
TPS650001	1.2 V	1.8 V	2.8 V
TPS650003	1.5 V	3.3 V	1.8 V
TPS650006	1.2 V	1.8 V	3.3 V

2 TPS650001/3/6 EVM Electrical Performance Specifications

Table 2. TPS650001/3/6EVM Electrical and Performance Specifications

PARAMETER		NOTES AND CONDITIONS		MIN	NOM	MAX	UNITS
INPUT CHARACTERISTICS							
V_{IN}	Input Voltage			2.3		6.0	V
V_{IN_UVLO}	Input UVLO	VIN falling		1.72	1.77	1.82	V
Hysteresis					160		mV
OUTPUT CHARACTERISTICS							
V_{ODCDC}	Output Voltage DCDC	V_{IN} = Nom, I_{OUT} = Nom, TPS650001, TPS650006			1.2		V
		V_{IN} = Nom, I_{OUT} = Nom, TPS650003			1.5		
	Accuracy DCDC1	VINDCDC 2.3V to 6V, With 1% tolerance resistors	PFM/PWM	–3.5%		3.5%	
			PWM		3%		
I_{OUTDC}	Output Current DCDC	V_{IN}DCDC = 2.3 V to 2.5 V				300	mA
		V_{IN}DCDC = 2.5 V to 6 V				600	
VLDO1	Output Voltage LDO1	V_{IN} = Nom, I_{OUT} = Nom, TPS650001, TPS650006			1.8		V
		V_{IN} = Nom, I_{OUT} = Nom, TPS650003			3.3		
$I_{OUTLDO1}$	Output Current LDO1	Continuous output current				300	mA
VLDO2	Output Voltage LDO2	TPS650001			2.8		V
		TPS650003			1.8		
		TPS650006			3.3		
$I_{OUTLDO2}$	Output Current LDO2	Continuous output current				300	mA
	Accuracy LDOs	VINLDO = 1.6 V to 6 V, Iout = 1 mA to 175 mA, VLDOx = 1.2 V, With 1% tolerance resistors		–5.5%		5.5%	
		VINLDO = 1.5 V to 6 V, Iout = 1 mA to 300 mA, VLDOx = 1.2 V, With 1% tolerance resistors		–5.5%		5.5%	
SYSTEMS CHARACTERISTICS							
F_{SW}	Switching Frequency			1722	2250	2847	kHz

3 Schematic



For Reference Only, See Table 4: Bill of Materials for Specific Values

Figure 1. TPS650001/3/6 EVM Schematic

4 Connector and Test Point Description

4.1 JP1 – ENDCDC

Placing a shorting bar between ENDCDC and ON ties the EN pin of the DCDC converter to VIN, thereby enabling the DCDC converter. Placing a shorting bar between ENDCDC and OFF ties the EN pin of the DCDC converter to GND, thereby disabling the DCDC converter.

4.2 JP2 – ENLDO1

Placing a shorting bar between ENLDO1 and ON ties the EN pin of LDO1 to VIN, thereby enabling LDO1. Placing a shorting bar between ENLDO1 and OFF ties the EN pin of LDO1 to GND, thereby disabling LDO1.

4.3 JP3 – ENLDO2

Placing a shorting bar between ENLDO2 and ON ties the EN pin of LDO2 to VIN, thereby enabling LDO2. Placing a shorting bar between ENLDO2 and OFF ties the EN pin of LDO2 to GND, thereby disabling LDO2.

4.4 JP4 – MODE

JP4 selects the forced PWM or Power Save Mode (PSM) operation for the DCDC converter. Placing a shorting bar between MODE and PWM ties the MODE pin of TPS650001/3/6 to VIN, thereby selecting forced PWM operating mode for the DCDC converter. Placing a shorting bar between MODE and PFM ties the MODE pin of TPS650001/3/6 to GND, thereby selecting Power Save Mode operating mode for the DCDC converter at light-load conditions. If Power Save Mode is selected the DCDC converter will automatically switch to PWM mode at heavier load conditions.

4.5 JP5 – VINLDO1

This header is the input supply for LDO1. Placing a shorting bar between VINLDO1 and VINDC/VODCDC supplies LDO1 from VIN with R2. It can be also supplied from the output of the converter VODCDC with R1 (not assembled). An external power supply can be connected between JP5 pin 2 (VINLDO1) and pin 3 (GND). Please note that the resistors R1 and R2 should be removed when supplying the LDO from an external power supply.

4.6 JP6 – VINLOD2

This header is the input supply for LDO2. Placing a shorting bar between VINLDO2 and VINDC/VODCDC supplies LDO2 from VIN with R4. It can be also supplied from the output of the converter VODCDC with R3 (not assembled). An external power supply can be connected between JP6 pin 2 (VINLDO2) and pin 3 (GND). Note that the resistors R3 and R4 should be removed when supplying the LDO from an external power supply.

4.7 J1 – VIN/GND

The input power supply has to be connected to this header. The power supply must be connected between J1 pins 1 and 2 (positive connection) and J1 pins 3 and 4 (GND). The leads to the input supply should be twisted and kept as short as possible. The input voltage has to be between 3.3-V and 6-V.

4.8 J2 – VODCDC/GND

This header is the output of the step-down converter. This output voltage is internally fixed for the TPS650001/3/6 (see Table 1). VODCDC is capable of sourcing up to 600-mA. A load can be connected between J2 pins 1 and 2 (positive connection) and J2 pins 3 and 4 (GND).

4.9 J3 – VLDO1/GND

This header is the output of LDO1. This output voltage is internally fixed for the TPS650001/3/6 (see Table 1). VLDO2 is capable of sourcing up to 300-mA. A load can be connected between J3 pins 1 and 2 (positive connection) and J3 pins 3 and 4 (GND).

4.10 J4 – VLDO2/GND

This header is the output of LDO2. This output voltage is internally fixes for the TPS650001/3/6 (see Table 1). The default setting on the EVM is 2.8-V. VLDO2 is capable of sourcing up to 300-mA. A load can be connected between J4 pins 1 & 2 (positive connection) and J4 pins 3 & 4 (GND).

4.11 J5 – $\overline{PG}$

JP5 is pulled to GND if the output voltages of the DCDC converter and both LDOs are > 90% of their set point and all enable pins are pulled high.

JP5 pulled up to the selected pull-up voltage level if any of the output voltages VODCDC, VLDO1 or VLDO2 is <90% of its set point or all enable pins are pulled low

5 4 TPS650001/3/6 Typical Performance Data and Characteristic Curves

Figure 2 through Figure 9 present typical performance curves for the TPS650001/3/6. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

5.1 Efficiency

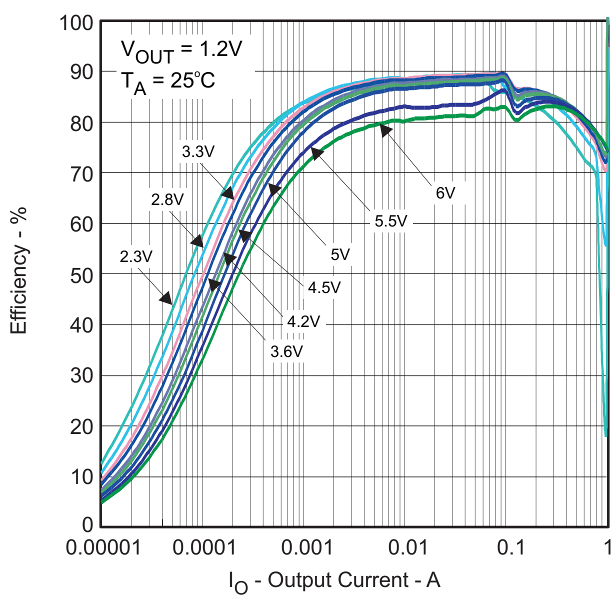


Figure 2. TPS650001/3/6 Efficiency vs Load Current

5.2 Line and Load Regulation

Figure 3 and Figure 4 show the load transient response of the DCDC converter and LDO, while Figure 5 and Figure 6 show the line transient response.

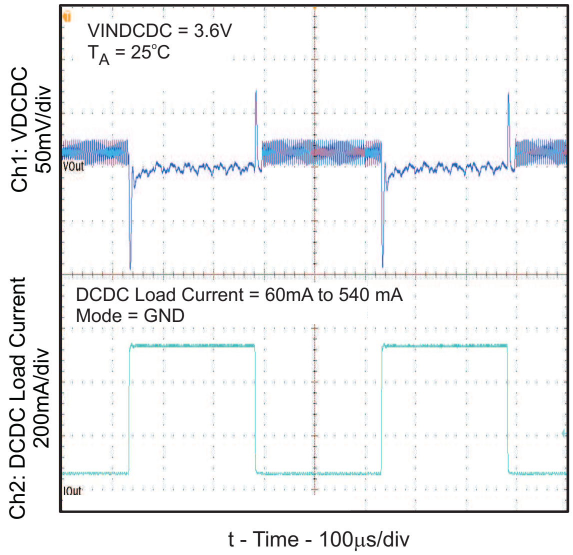


Figure 3. TPS650001/3/6 DCDC Converter Load Transient Response

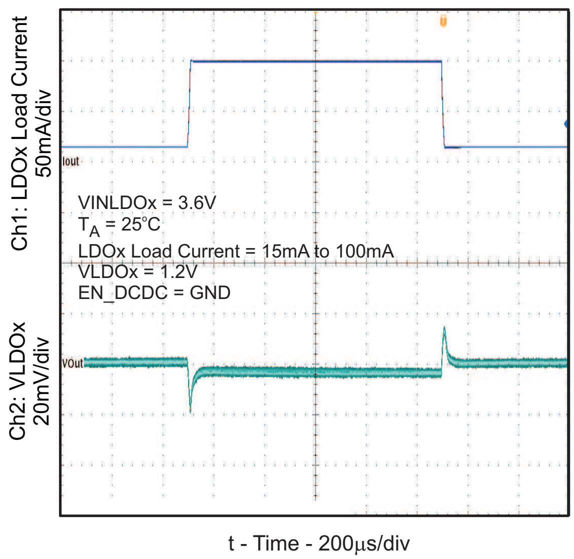


Figure 4. TPS650001/3/6 LDOx Transient Response

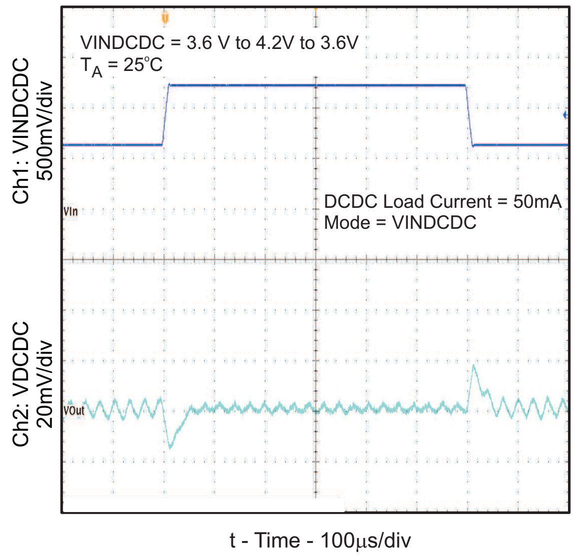


Figure 5. TPS650001/3/6 DCDC Converter Line Transient Response

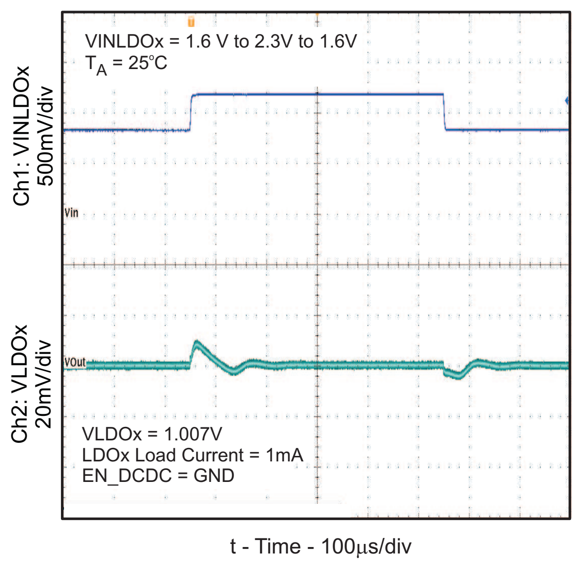


Figure 6. TPS650001/3/6 LDOx Line Transient Response

5.3 Output Voltage Ripple

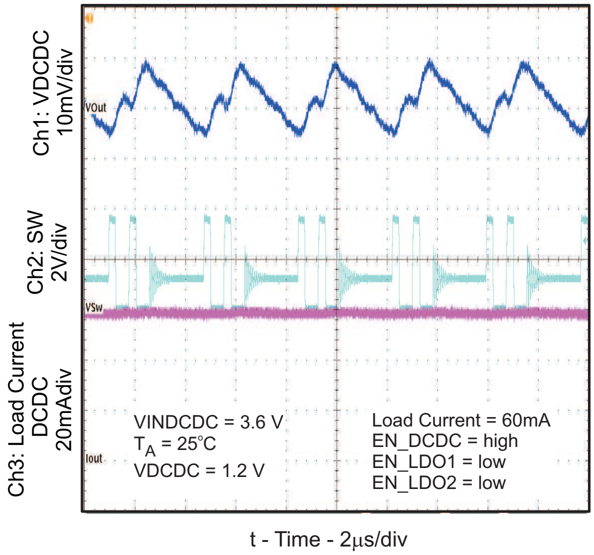


Figure 7. TPS650001/3/6 Output Voltage Ripple (MODE = low)

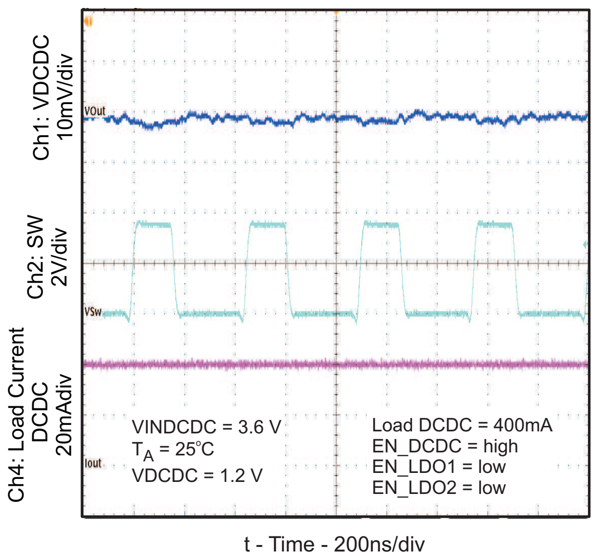


Figure 8. TPS650001/3/6 Output Voltage Ripple (MODE = high)

5.4 Startup Timing

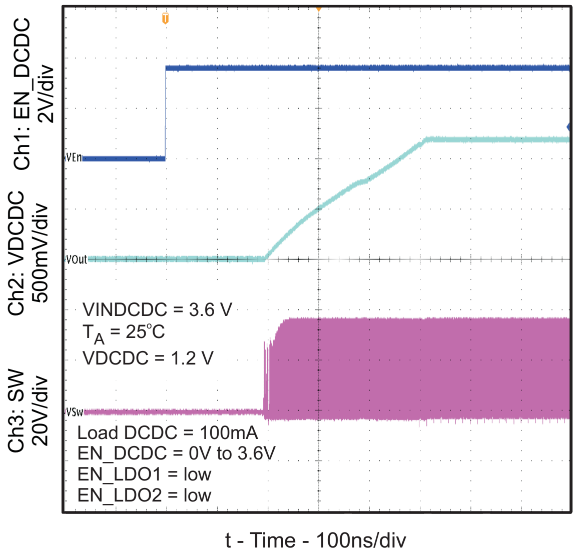


Figure 9. TPS650001/3/6 DCDC Converter Startup Timing

6 EVM Assembly Drawings and Layout

The following figures (Figure 10 through Figure 12) show the design of the TPS650001/3/6EVM printed circuit board. The EVM has been designed using a 2-Layer, 1oz copper-clad circuit board 2.0” x 2.4” (50.8mm x 61.09mm).

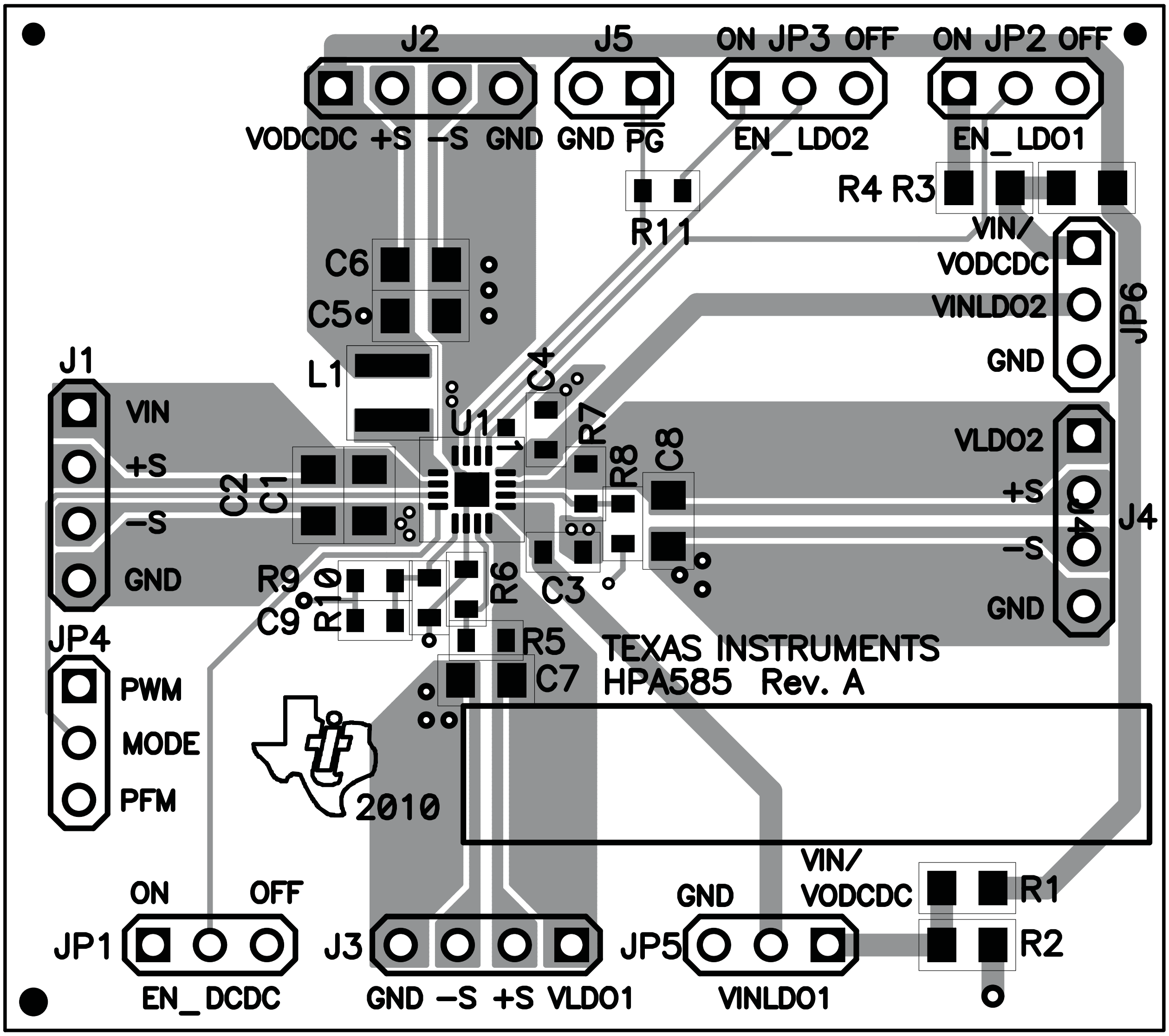


Figure 10. TPS650001/3/6 EVM Component Placement (Viewed from Top)

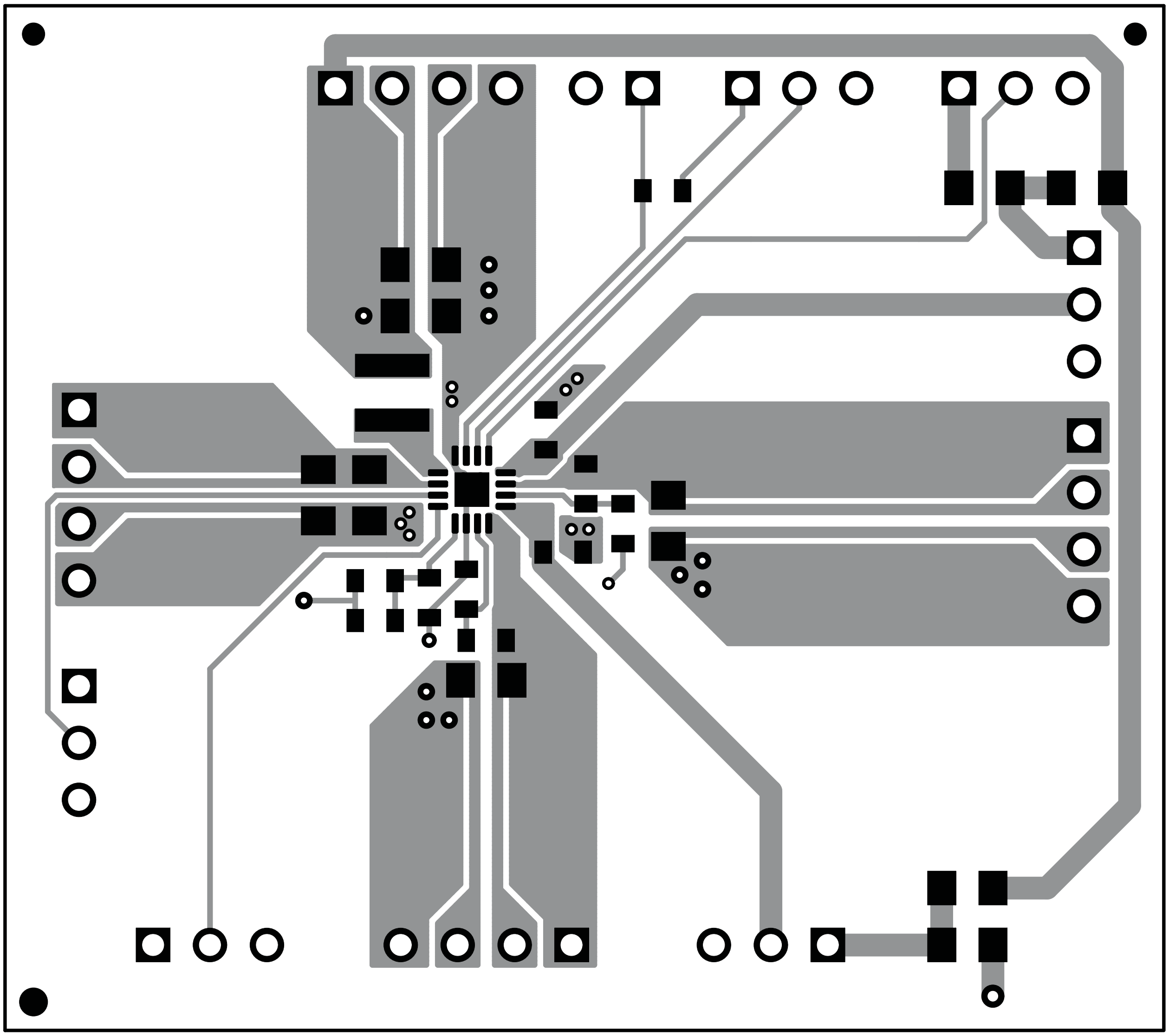


Figure 11. TPS650001/3/6 EVM Top Copper (Viewed from Top)

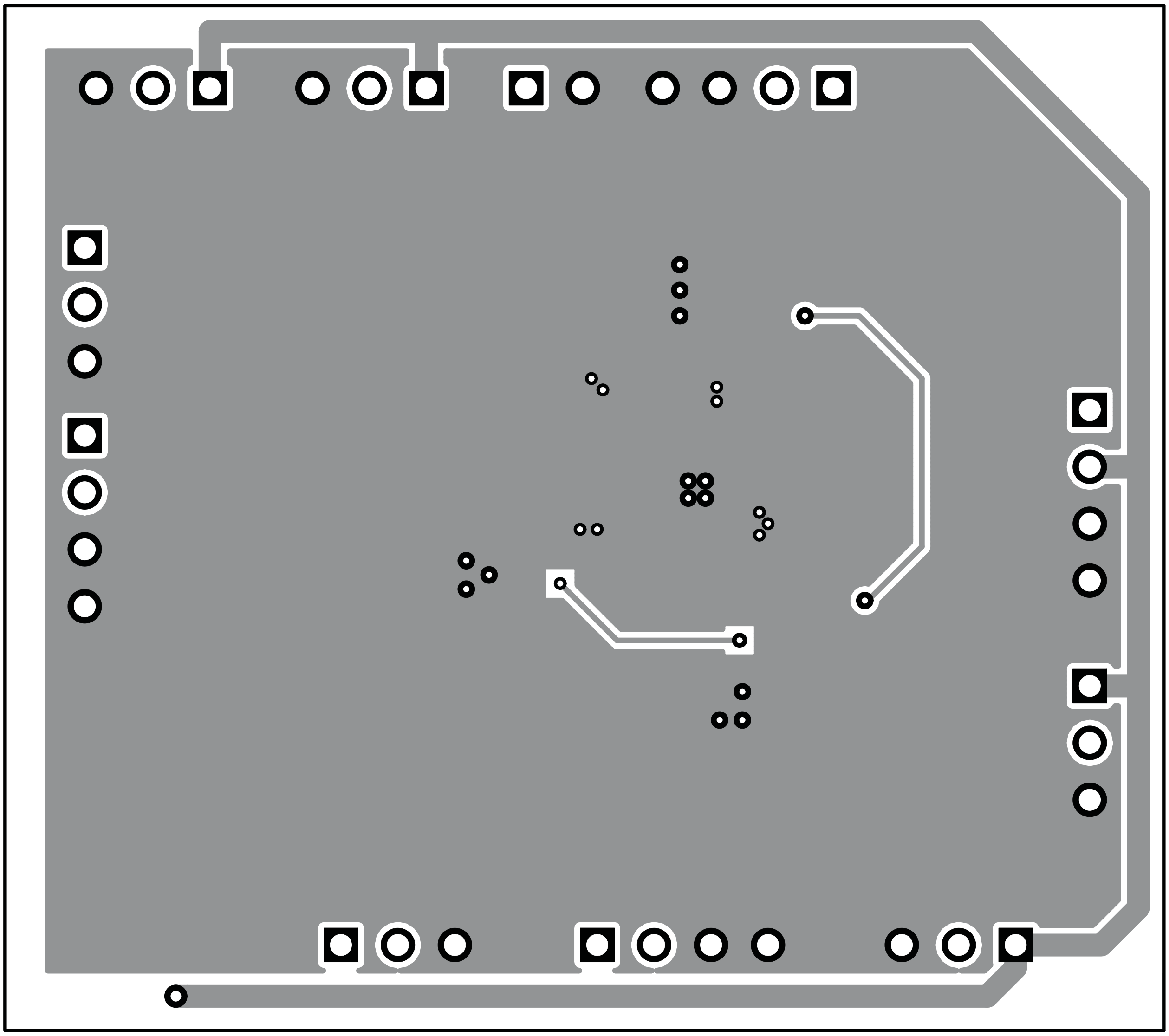


Figure 12. TPS650001/3/6 EVM Bottom Copper (Viewed from Bottom)

7 List of Materials

Table 3 lists the EVM components as configured according to the schematic shown in Figure 1.

Table 3. TPS650001/3/6EVM Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
0	C1, C6	open	Capacitor, Ceramic, 10V, X5R, 10%, l	0805	Std	Std
4	C2, C5, C7, C8	10µF	Capacitor, Ceramic, 10V, X5R, 10%, e	0805	Std	Std
2	C3, C4	2.2µF	Capacitor, Ceramic, 16V, X5R, 10%,	0603	Std	Std
0	C9	open	Capacitor, Ceramic, 50V, C0G, 5%	0603	Std	Std
4	J1, J2, J3, J4	PEC04SAAN	Header, Male 4-pin, 100mil spacing	0.100 inch x 4	PEC04SAAN	Sullins
1	J5	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
6	JP1 - JP6	PEC03SAAN	Header, Male 3-pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
1	L1	2.2µH	Inductor, SMT, 2.0A, 110milliohm	0.118 x 0.118 inch	LPS3015-222ML	Coilcraft
0	R1, R3	open	Resistor, Chip, 1/10W, 1%	0805	Std	Std
2	R2, R4	0	Resistor, Chip, 1/10W, 1%	0805	Std	Std
3	R5, R7, R9	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R6, R8, R10	open	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R11	17.5k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	U1 (HPA585-001)	TPS650001RTE	IC, 2.25 MHz Step Down Converter with Dual LDOs and SVS	QFN	TPS650001RTE	TI
0	U1 (HPA585-002)	TPS650003RTE	IC, 2.25 MHz Step Down Converter with Dual LDOs and SVS	QFN	TPS650003RTE	TI
0	U1 (HPA585-003)	TPS650006RTE	IC, 2.25 MHz Step Down Converter with Dual LDOs and SVS	QFN	TPS650006RTE	TI
1	--		PCB, 1.8 In x 2.04 In x 0.062 In		HPA585	Any
6	--		Shunt, 100 mil, Black	0.100	929950-00	3M
1	--		Label	1.25 x 0.25 inch	THT-13-457-10	Brady

Notes:
1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.