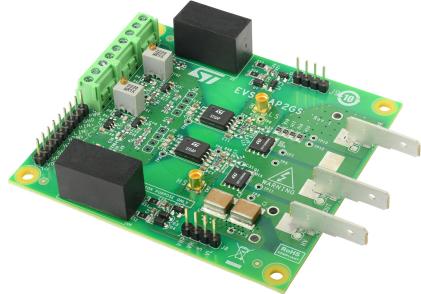


Demonstration board for STGAP2GS galvanically isolated single gate driver with e-mode GaN transistor



Product status link

[EVSTGAP2GS](#)

Features

- Board
 - Half bridge configuration, high voltage rail up to 650 V
 - SGT120R65AL: 650 V, 75 mΩ typ., 15 A, e-mode PowerGaN transistor
 - Negative gate driving
 - On-board isolated DC-DC converters to supply high-side and low-side gate drivers, fed by VAUX = 5 V, with 5.2 kV maximum isolation
 - VDD logic supplied by on-board 3.3 V or VAUX = 5 V
 - Easy jumper selection of driving voltage configuration: +6/0 V; +6/-3 V
- Device
 - High voltage rail up to 1200 V
 - Driver current capability: 2 A / 3 A source/sink @ 25 °C, VH = 6 V
 - Separate sink and source for easy gate driving configuration
 - Input-output propagation delay: 45 ns
 - UVLO function optimized for GaN
 - Gate driving voltage up to 15 V
 - 3.3 V, 5 V TTL/CMOS inputs with hysteresis
 - Temperature shut down protection

Description

The **EVSTGAP2GS** is a half bridge evaluation board designed to evaluate the **STGAP2GS** isolated single gate driver.

The gate driver is characterized by 2 A source and 3 A sink capability and rail-to-rail outputs, making the device also suitable for mid and high power inverter applications such as power conversion and motor driver inverters in industrial applications.

The device allows to independently optimize turn-on and turn-off by using dedicated gate resistors.

The device integrates protection functions including thermal shutdown and UVLO with optimized level for enhancement-mode GaN transistors, which enables easy design high efficiency and reliable systems. Dual input pins allow the selection of signal polarity control and implementation of HW interlocking protection to avoid cross-conduction in case of controller malfunction.

The device allows implementing negative gate driving, and the on board isolated DC-DC converters allows working with optimized driving voltage for e-mode GaN transistors.

The **EVSTGAP2GS** board allows evaluation of all the STGAP2GS features driving the SGT120R65AL 75 mΩ, 650 V e-Mode GaN transistors.

The board components are easy to access and modify in order to make driver performance evaluation easier under different application conditions and fine adjustment of final application components.

1 Schematic diagrams

Figure 1. Circuit schematic – gate drivers and connectors

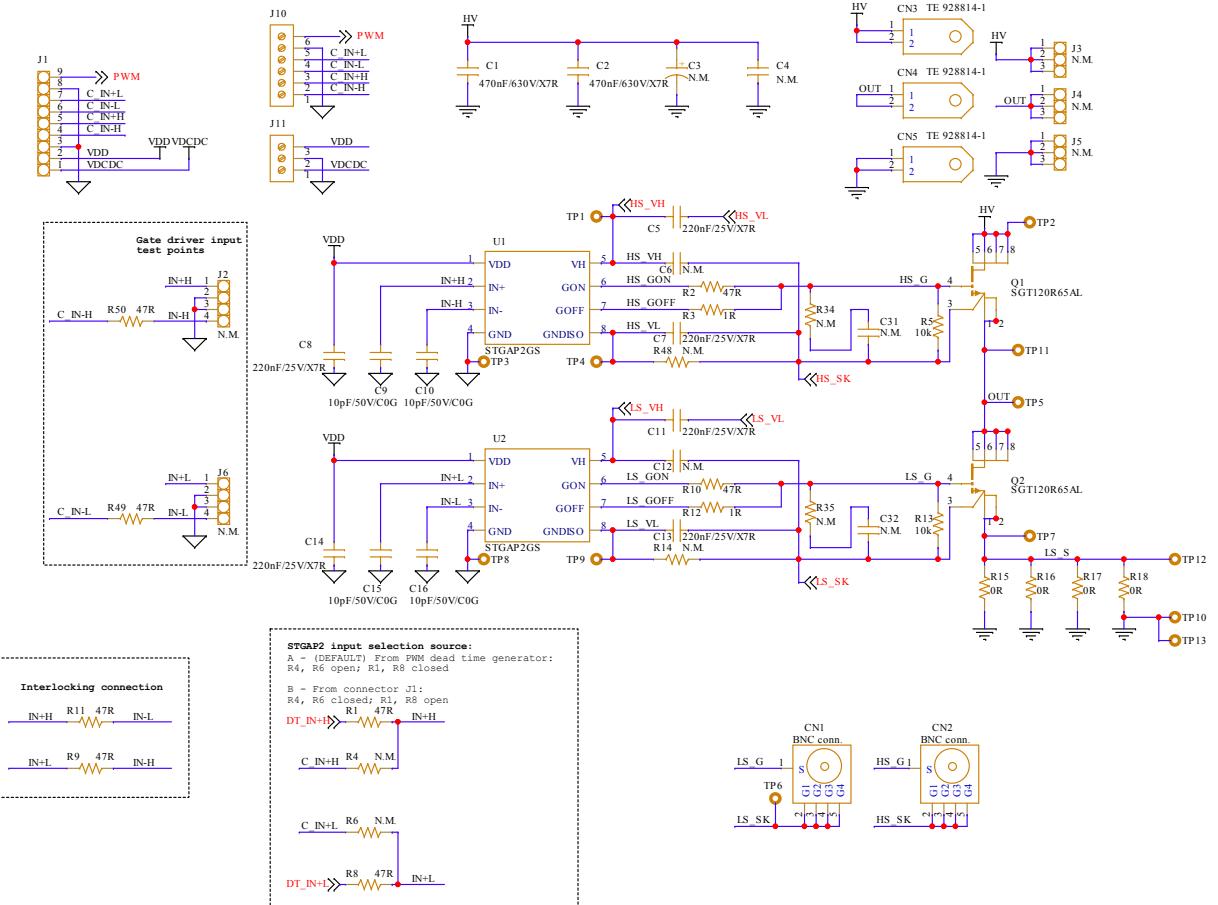


Figure 2. Circuit schematic – supply

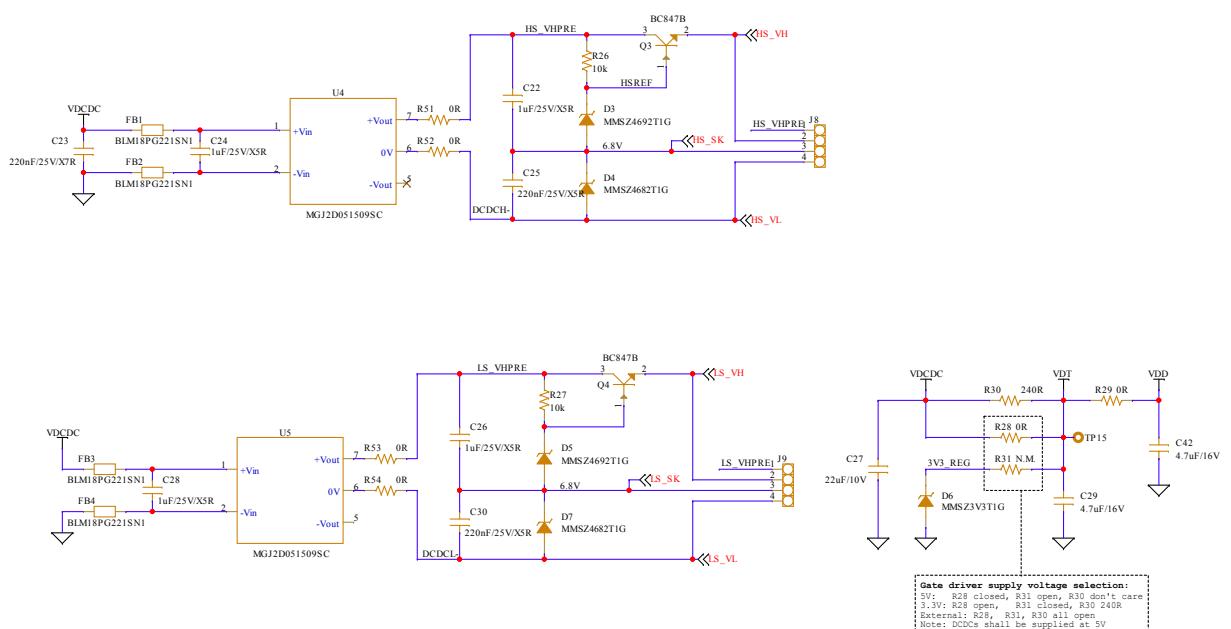
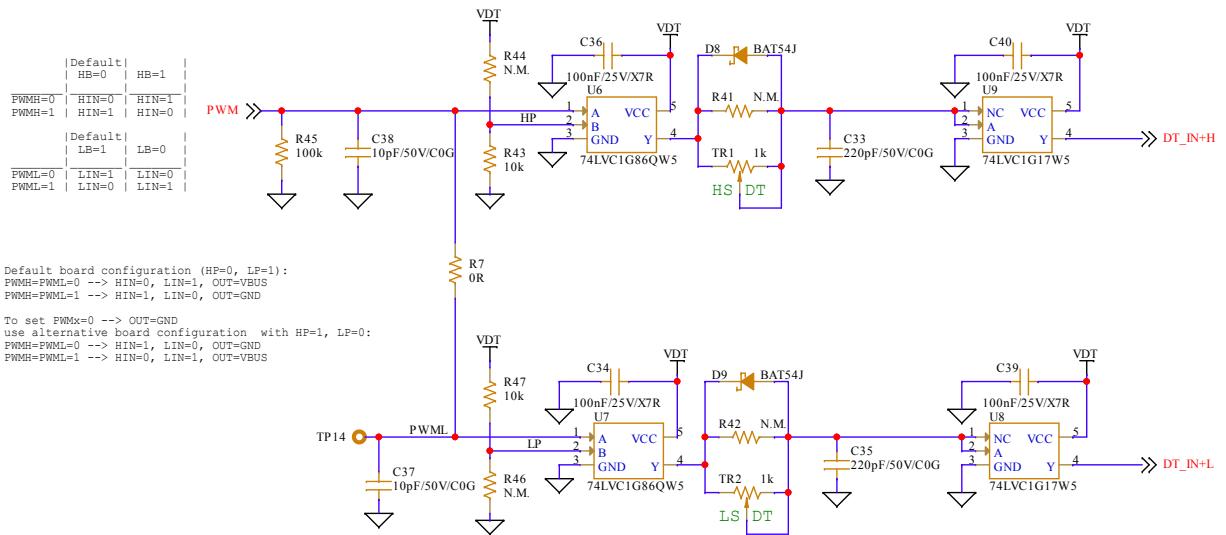


Figure 3. Circuit schematic – Dead time generation



2 Bill of material

Table 1. Bill of material

Reference	Part Value	Part Description
CN1, CN2	Cinch 135-3701-201 or equivalent	MMCX Straight Receptacle
CN3, CN4, CN5	TE 928814-1	Tab FASTON - Pitch 5.08 mm
C1, C2	470 nF / 630 V / X7R	SMT ceramic capacitor - Size 2225
C3	N.M.	THT electrolytic capacitor - Radial p10 d22
C4	N.M.	Film capacitor - Pitch 37.5 mm
C5, C7, C8, C11, C13, C14, C23	220 nF / 25 V / X7R	SMT ceramic capacitor - Size 0603
C6, C12, C31, C32	N.M.	SMT ceramic capacitor - Size 0603
C9, C10, C15, C16, C37, C38	10 pF / 50 V / C0G	SMT ceramic capacitor - Size 0603
C22, C24, C26, C28	1 µF / 25 V / X5R	SMT ceramic capacitor - Size 0603
C25, C30	220 nF / 25 V / X5R	SMT ceramic capacitor - Size 0603
C27	22 µF / 10 V	SMT ceramic capacitor - Size 0805
C29, C42	4.7 µF / 16 V	SMT ceramic capacitor - Size 0603
C33, C35	220 pF / 50 V / C0G	SMT ceramic capacitor - Size 0603
C34, C36, C39, C40	100 nF / 25 V / X7R	SMT ceramic capacitor - Size 0603
D3, D5	MMSZ4692T1G	6.8 V Zener voltage regulator - SOD123
D4, D7	MMSZ4682T1G	2.7 V Zener voltage regulator - SOD123
D6	MMSZ3V3T1G	3.3 V Zener voltage regulator - SOD123
D8, D9	BAT54J	Small signal Schottky diode - SOD-323
FB1, FB2, FB3, FB4	BLM18PG221SN1	Ferrite beads - Size 0603
J1	Strip 1x9	Strip connector 9 pos, 2.54 mm
J2, J6	N.M.	Strip connector 4 pos, 2.54 mm
J3, J4, J5	N.M.	Strip connector 3 pos, 2.54 mm
J8, J9	Strip 1x4	Strip connector 4 pos, 2.54 mm
J10	MORSV-350-6P_screw	Screw connector 6 poles, Pitch 3.5 mm
J11	MORSV-350-3P_screw	Screw connector 3 poles, Pitch 3.5 mm
Q1, Q2	SGT120R65AL	650 V e-mode GaN transistor - PowerFLAT 5x6 mm HV
Q3, Q4	BC847B	NPN general purpose transistor - SOT-23
R1, R8, R9, R11, R49, R50	47 Ω	SMT resistor - Size-0603
R2, R10	47 Ω	SMT resistor - Size-0603
R3, R12	1 Ω	SMT resistor - Size-0603
R4, R6, R14, R31, R41, R42, R44, R46, R48	N.M.	SMT resistor - Size-0603
R5, R13, R26, R27	10 kΩ	SMT resistor - Size-0603
R7, R28, R29	0 Ω	SMT resistor - Size-0603
R15, R16, R17, R18	0 Ω	SMT resistor - Size-0805
R30	240 Ω	SMT resistor - Size-0603
R34, R35	N.M.	SMT resistor - Size-0603

Reference	Part Value	Part Description
R43, R47	10 kΩ	SMT resistor - Size-0603
R45	100 kΩ	SMT resistor - Size-0603
R51, R52, R53, R54	0 Ω	SMT resistor - Size-1206
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15	Test point for probe	Metallized hole, 0.8 mm diameter
TR1, TR2	1 kΩ - 3266W	Trimming potentiometer
U1, U2	STGAP2GS	Galvanically isolated single gate driver for e-mode GaN FETs - SO-8W
U4, U5	MGJ2D051509SC	5.2 kV Isolated DC-DC converter Murata
U6, U7	74LVC1G86QW5	2-input EX-OR gate - SOT23-5L
U8, U9	74LVC1G17W5	Single Schmitt-trigger buffer - SOT23-5L

3 Layout and component placements

Figure 4. Layout - component placement top

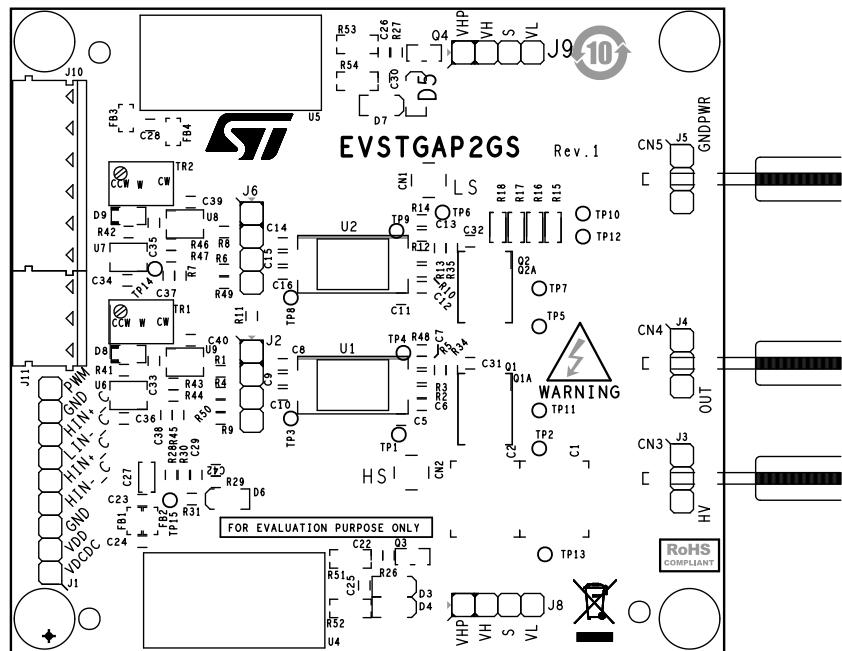


Figure 5. Layout - component placement bottom

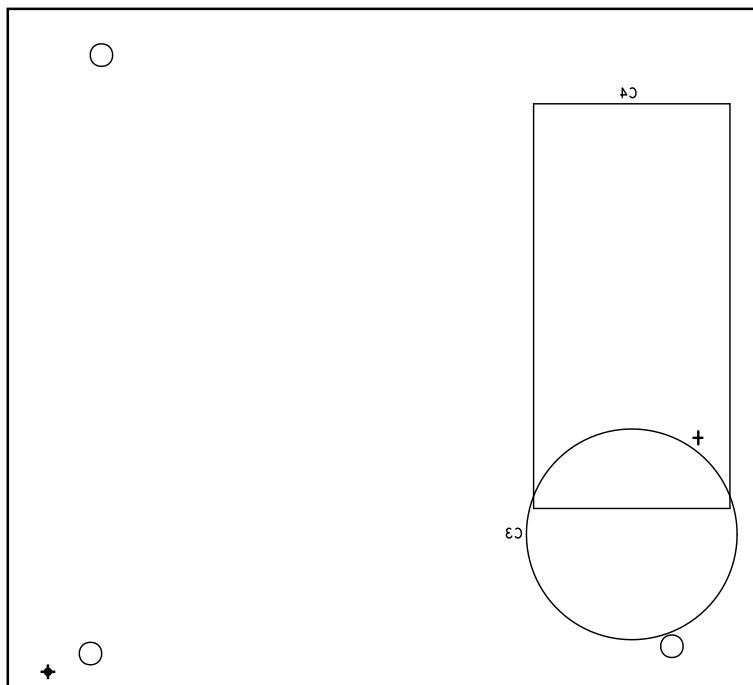


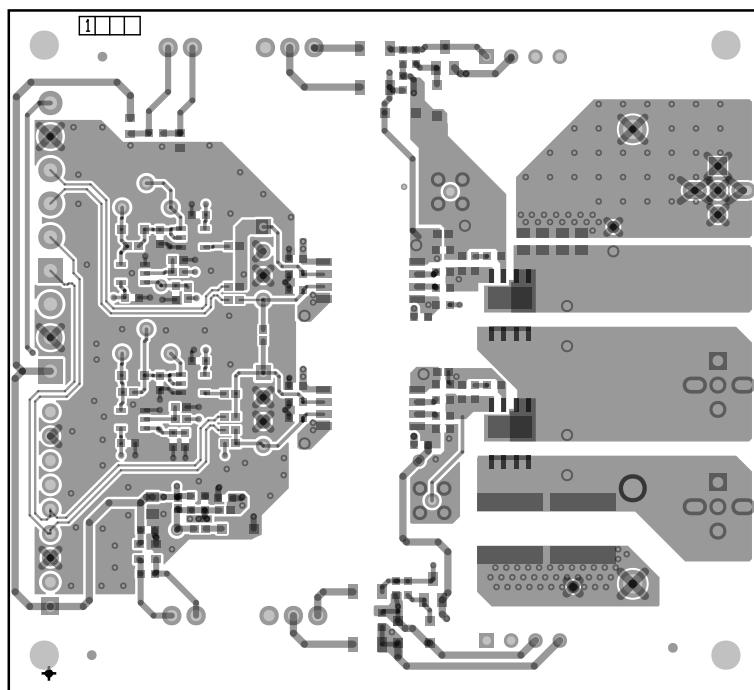
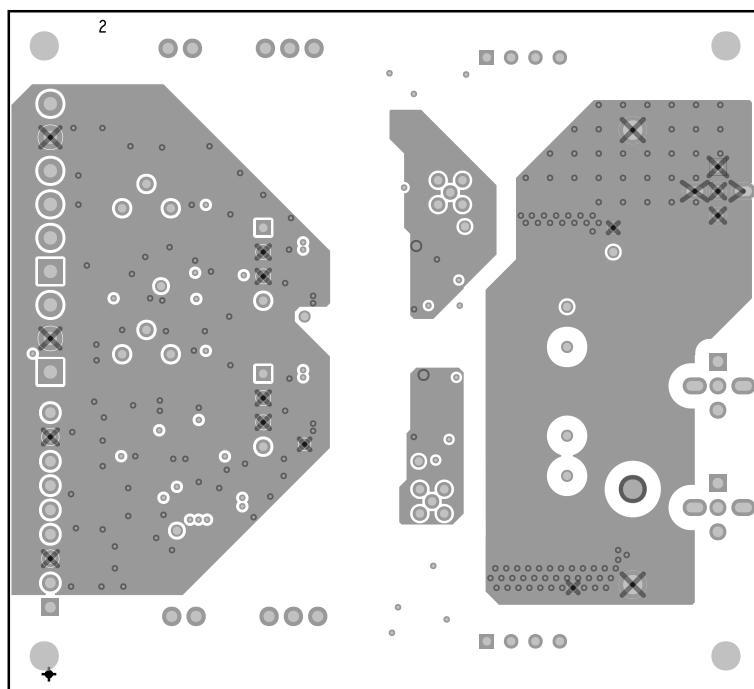
Figure 6. Layout - top layer**Figure 7. Layout - inner 2 layer**

Figure 8. Layout - inner 3 layer

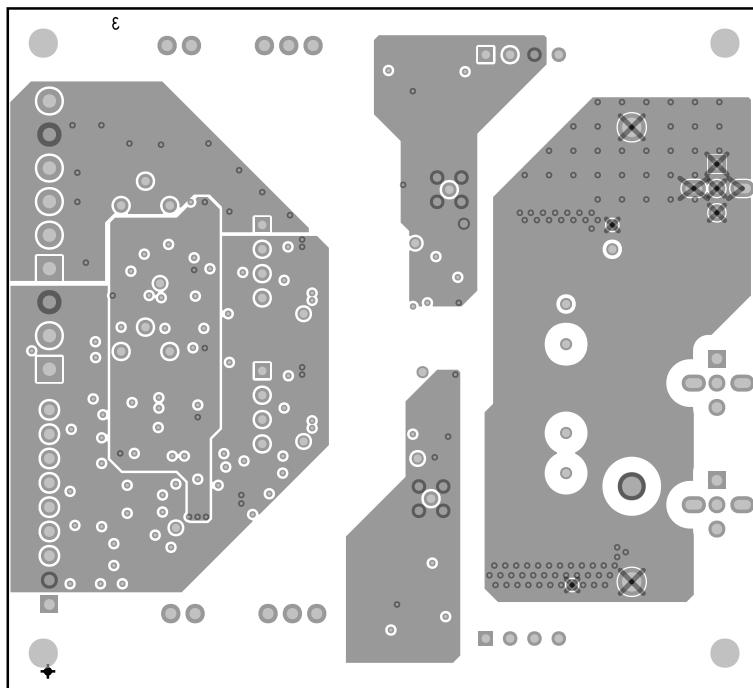
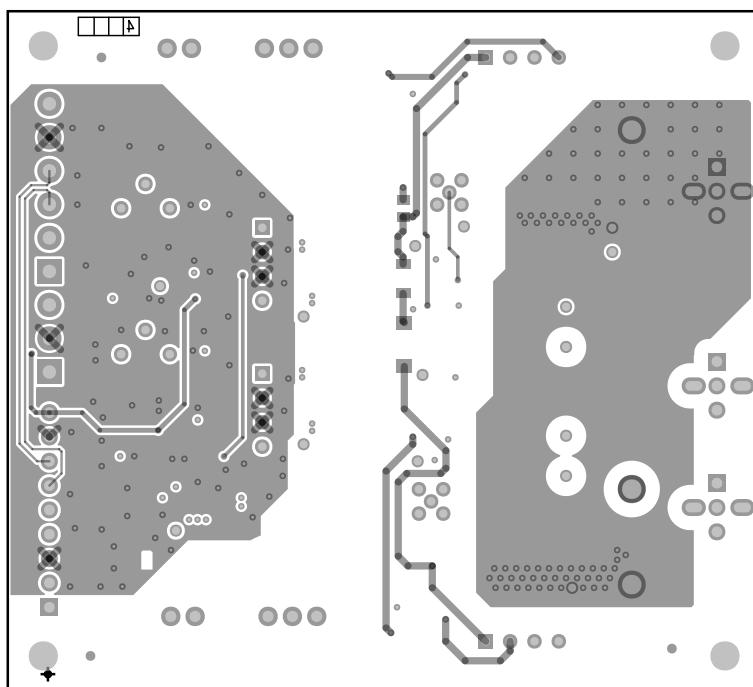


Figure 9. Layout - bottom layer



Revision history

Table 2. Document revision history

Date	Version	Changes
26-May-2023	1	Initial release.

Contents

1	Schematic diagrams	2
2	Bill of material	4
3	Layout and component placements	6
	Revision history	9
	List of tables	11
	List of figures.....	12

List of tables

Table 1.	Bill of material	4
Table 2.	Document revision history	9

List of figures

Figure 1.	Circuit schematic – gate drivers and connectors	2
Figure 2.	Circuit schematic – supply	2
Figure 3.	Circuit schematic – Dead time generation	3
Figure 4.	Layout - component placement top	6
Figure 5.	Layout - component placement bottom	6
Figure 6.	Layout - top layer	7
Figure 7.	Layout - inner 2 layer	7
Figure 8.	Layout - inner 3 layer	8
Figure 9.	Layout - bottom layer	8

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