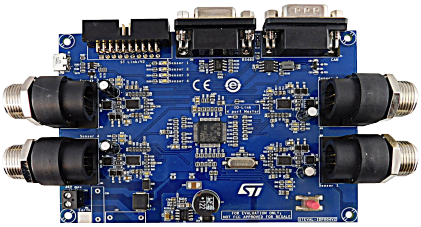
STEVAL-IPD004V2

Data brief

IO-Link master multi-port evaluation board based on L6360



Product summary	
IO-Link master multi-port evaluation board based on L6360	STEVAL-IDP004V2
High-performance ARM Cortex-M3 MCU with 128 Kbytes Flash, 120 MHz CPU, ART Accelerator	STM32F205RB
IO-Link communication master transceiver IC	L6360

Features

- Master IO-Link stack embedded with read out protection
- Limitation of time of use (10000 minutes)
- Fully compatible with all IO-Link devices
- Main supply voltage 32 V maximum
- 4 L6360 IO-Link master transceiver ICs
- RS-485 serial interface
- CAN serial interface
- USB interface
- DC-DC converter
- On-board reverse polarity protection
- Designed to meet IEC requirement for industrial standards
- RoHS and WEEE compliant

Description

The STEVAL-IDP004V2 evaluation board embeds the STM32F205RB microcontroller and four separate L6360 ICs.

Communication with the ICs is implemented via I²C in master mode and is managed by the STM32F205RB MCU; each L6360 has its own address and shares the bus with the other devices.

The STEVAL-IDP004V2 is developed to create a multi-port master based on serial asynchronous communication to support the IO-Link protocol.

Each node is equipped with an industrial M12 connector (as recommended by the standard) for connection with a single slave node using a cable (max. length 20 meters). The wire is a normal three-pole: one for the IO-Link bus, one for the L+ line (positive supply voltage pole) and one for the L- line (negative supply voltage pole).

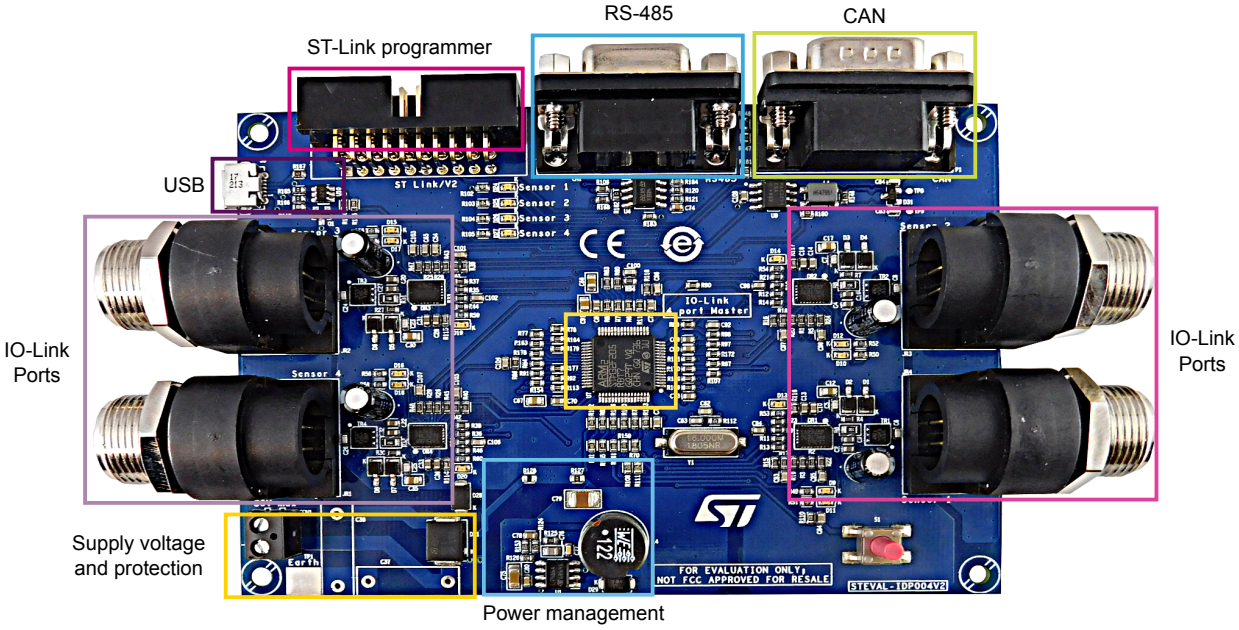
The STEVAL-IDP004V2 board also includes RS-485 bus, CAN bus and USB hardware interfaces.

The layout is designed to meet the requirements for IEC61000-4-2/4/5 for industrial segment.

Note: The protocol stack is provided by TEConcept GmbH and comes with some limitations. Be aware that the STSW-IO-LINK implements only the physical layer without stack. Programming it into the microcontroller you lose the full stack. This process is irreversible.

1 Board components

Figure 1. STEVAL-IDP004V2 components



2 Schematic diagrams

Figure 2. STEVAL-IDP004V2 circuit schematic (1 of 11)

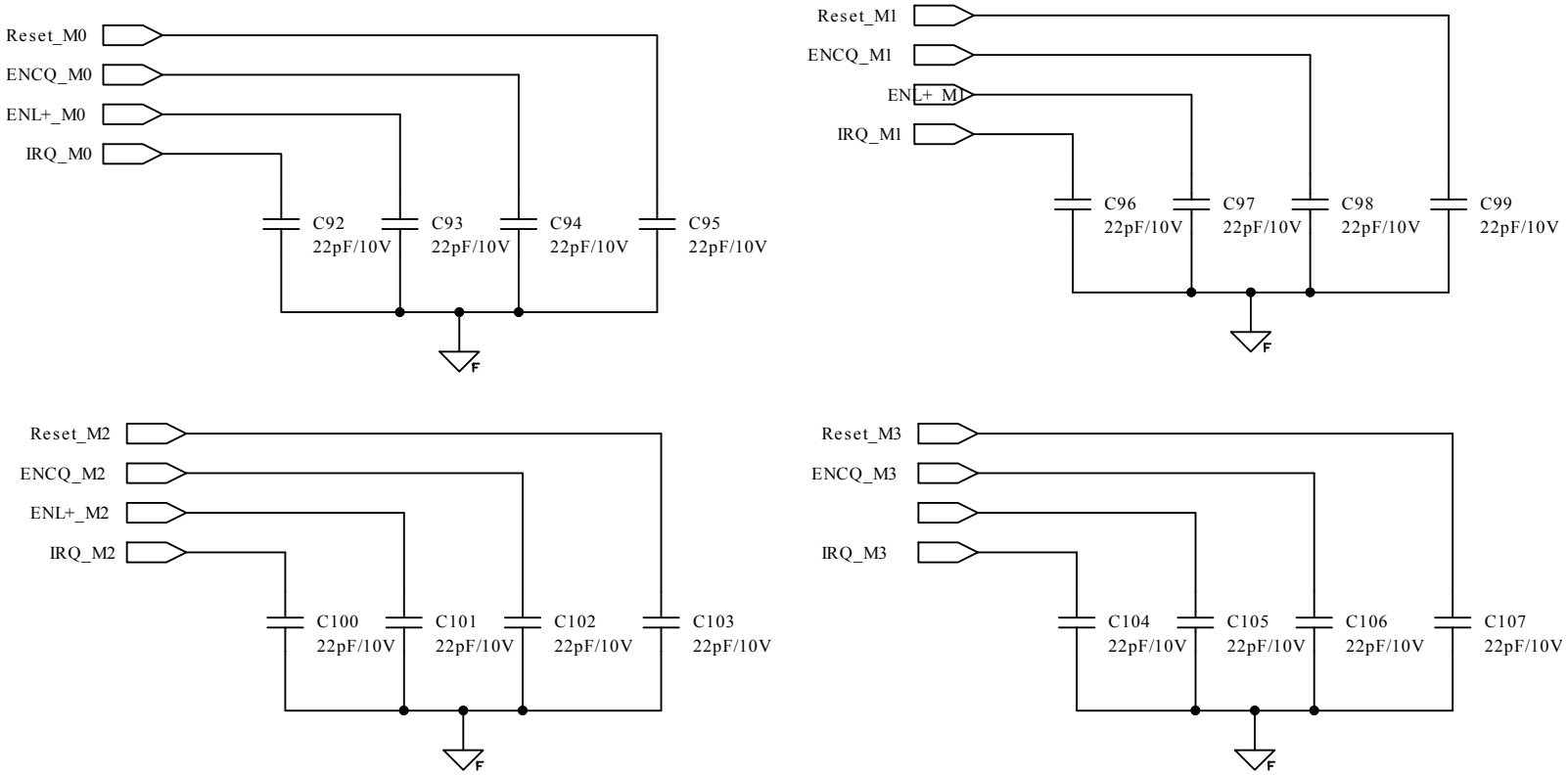


Figure 3. STEVAL-IDP004V2 circuit schematic (2 of 11)

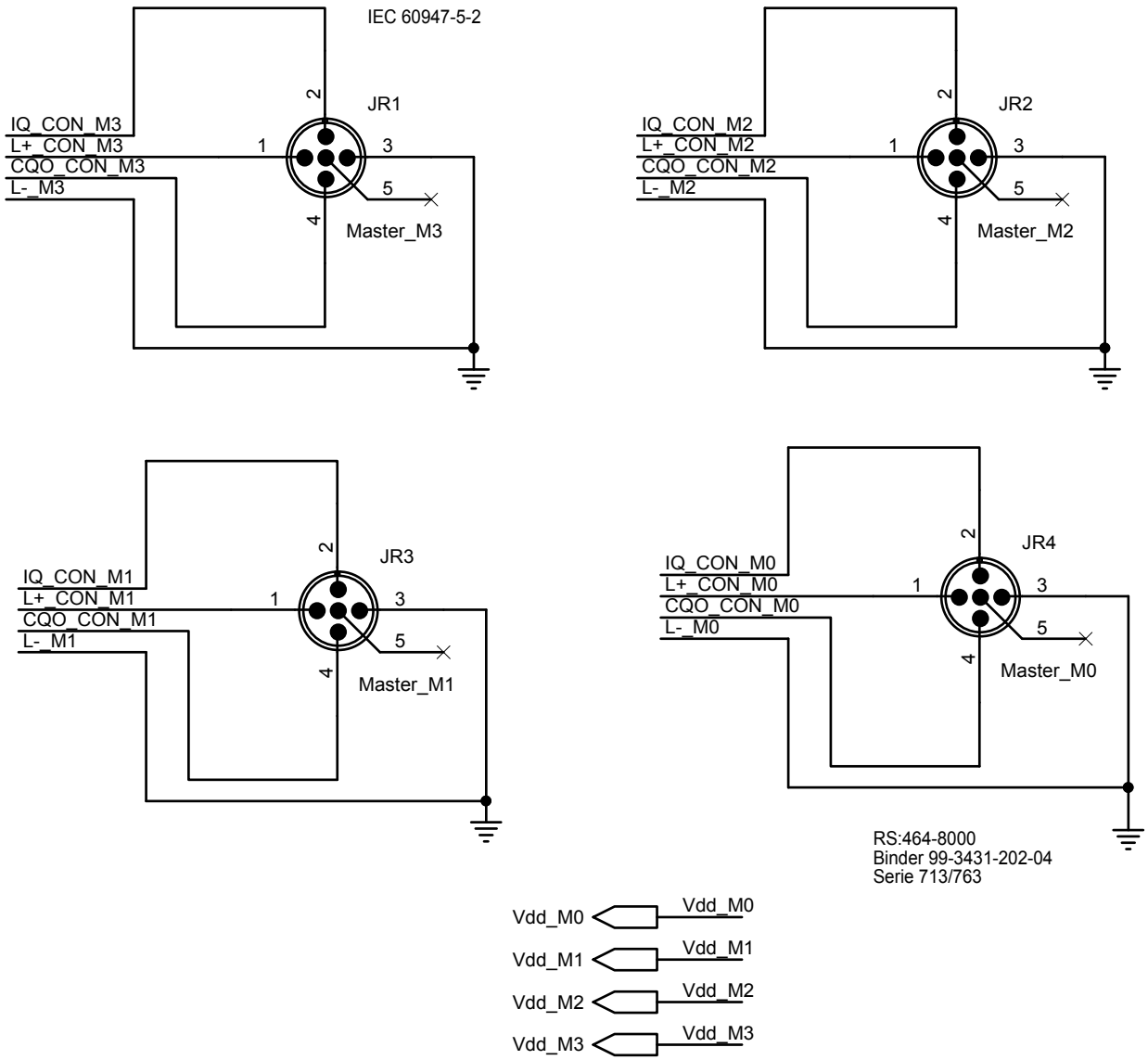


Figure 4. **STEVAL-IDP004V2 circuit schematic (3 of 11)**

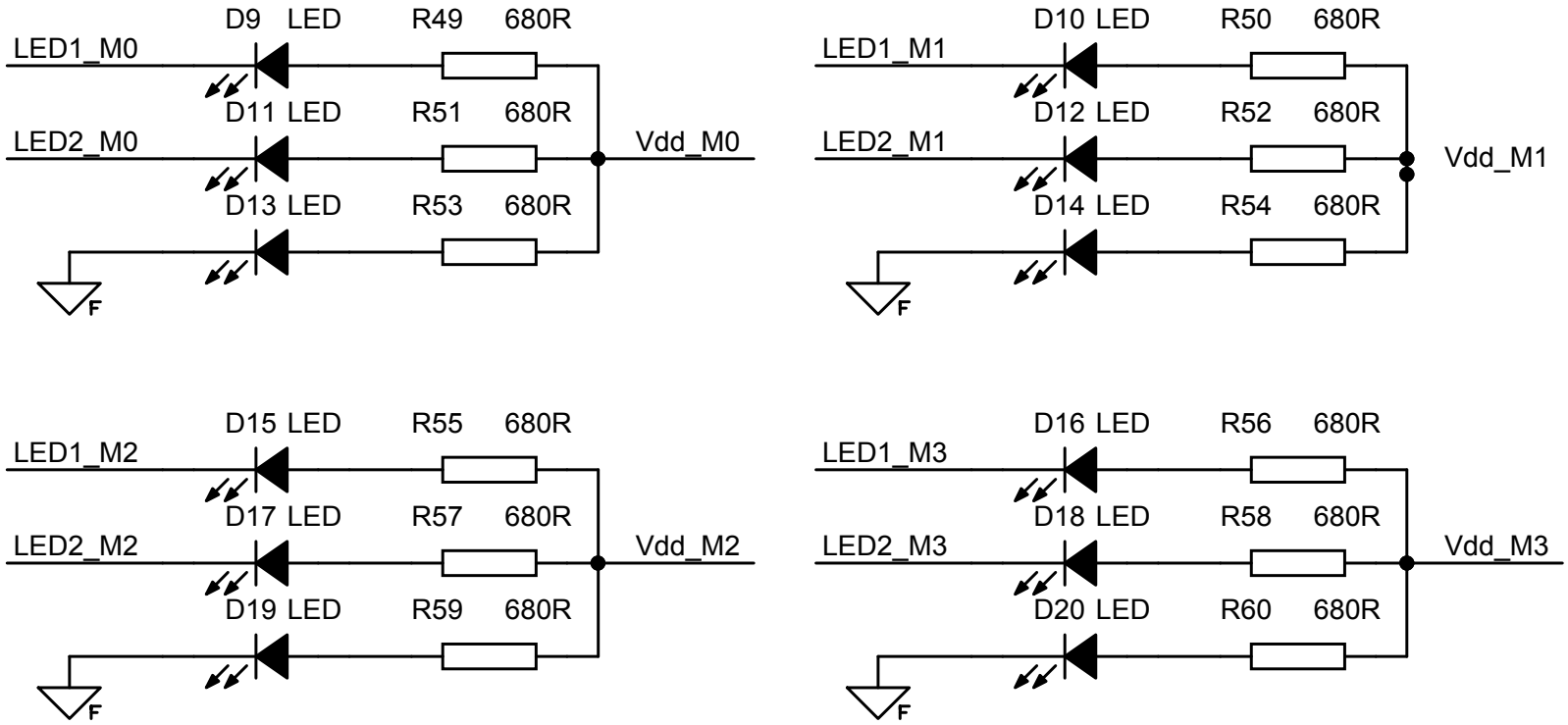


Figure 5. STEVAL-IDP004V2 circuit schematic (4 of 11)

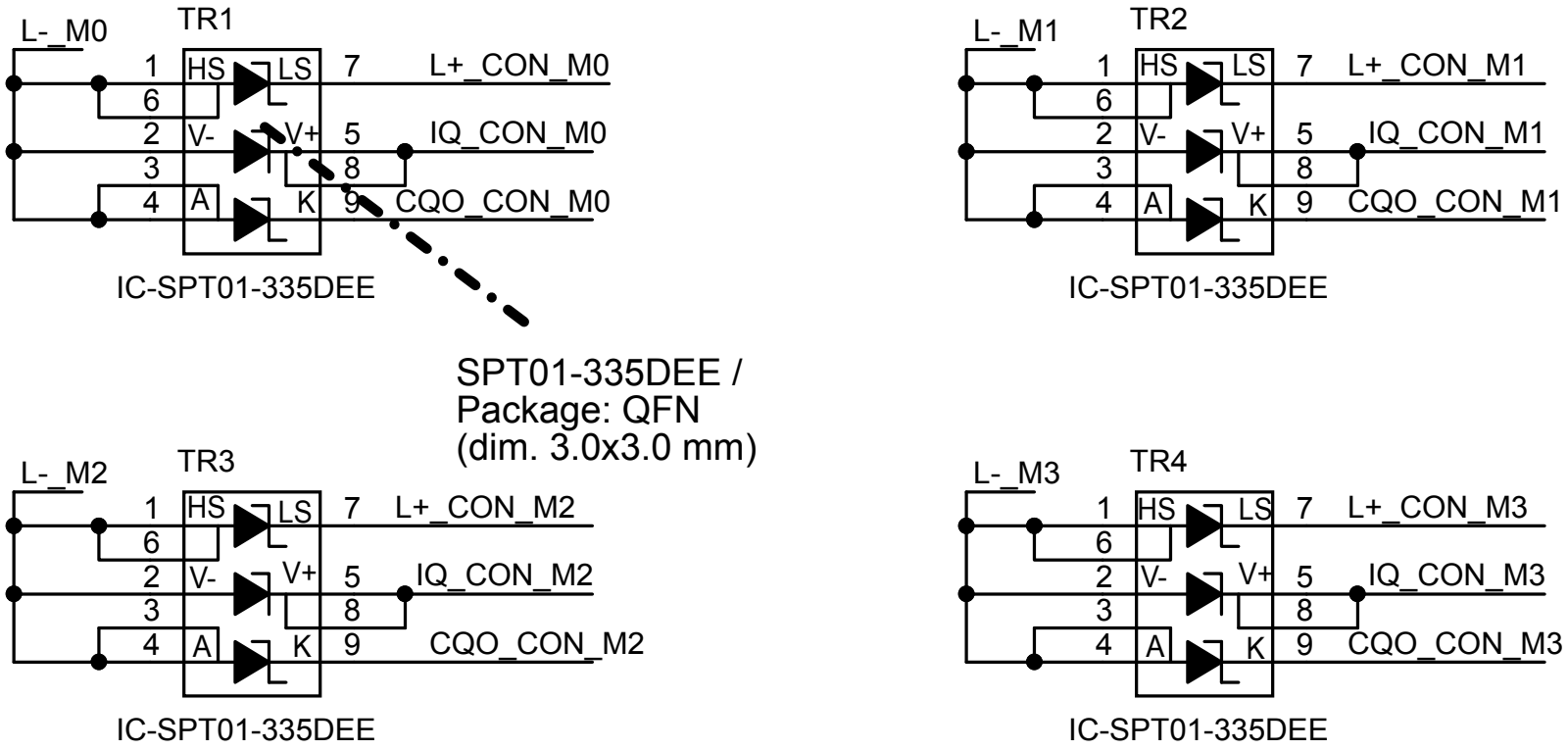


Figure 6. STEVAL-IDP004V2 circuit schematic (5 of 11)

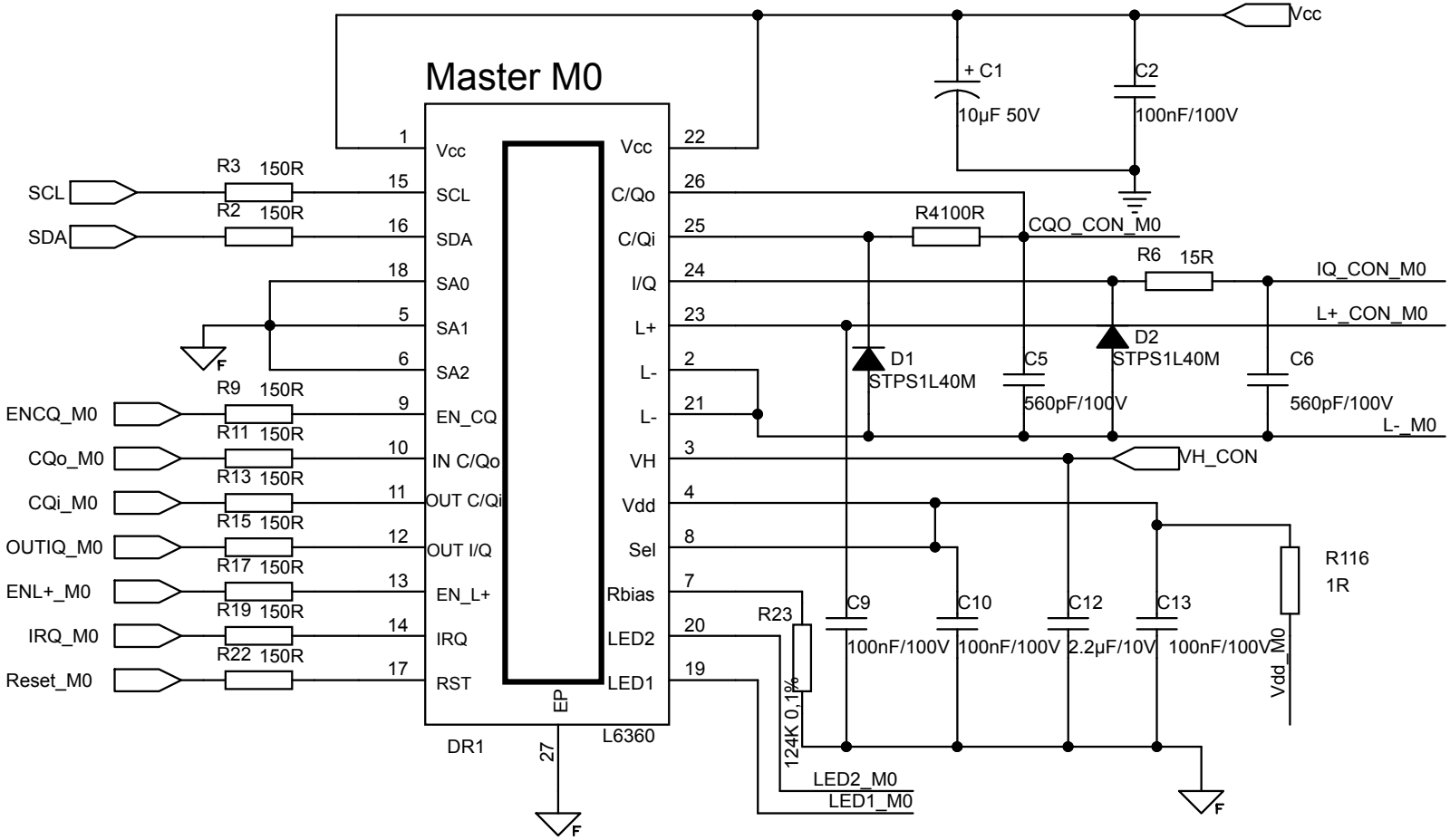


Figure 7. STEVAL-IDP004V2 circuit schematic (6 of 11)

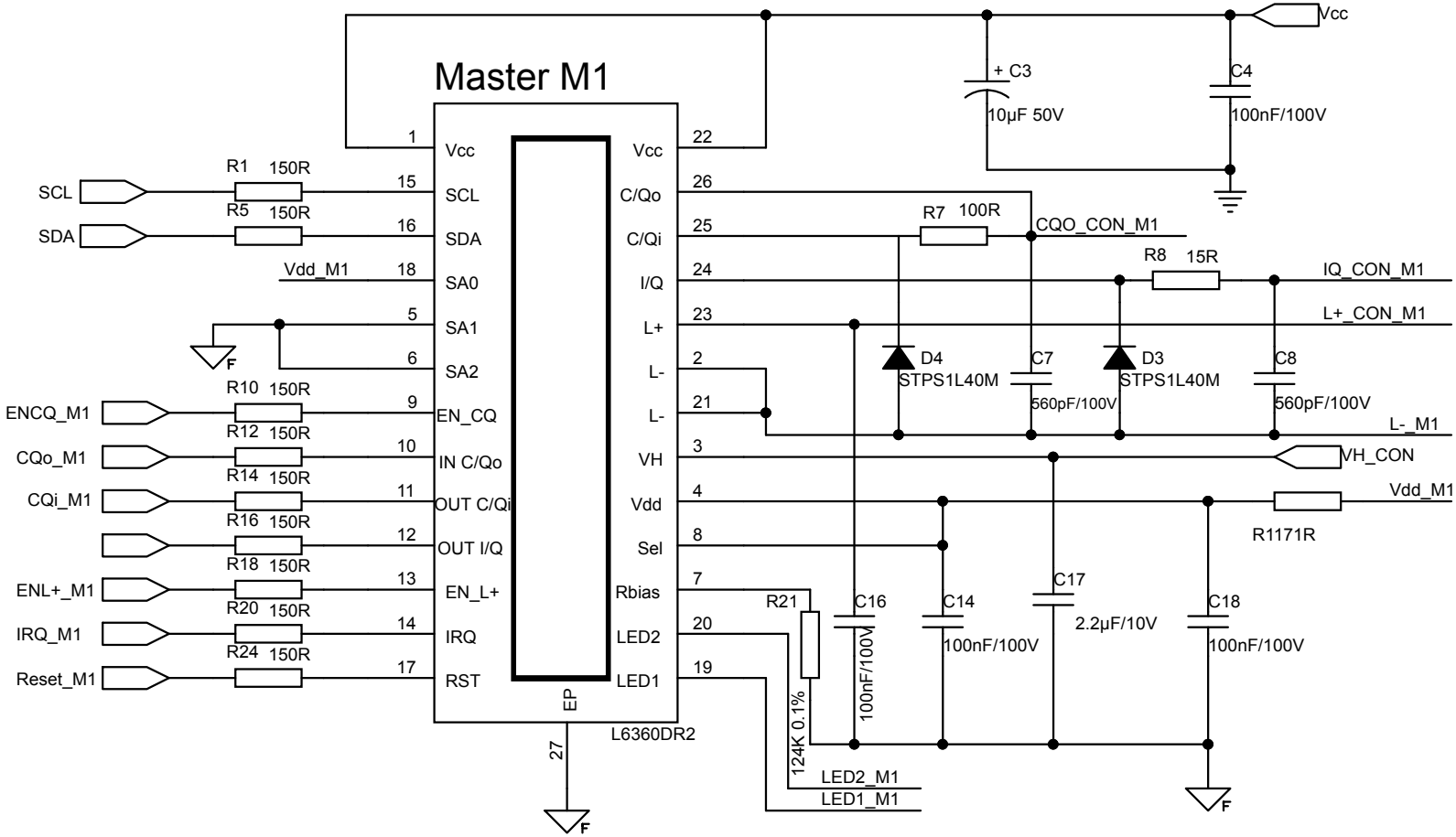


Figure 8. STEVAL-IDP004V2 circuit schematic (7 of 11)

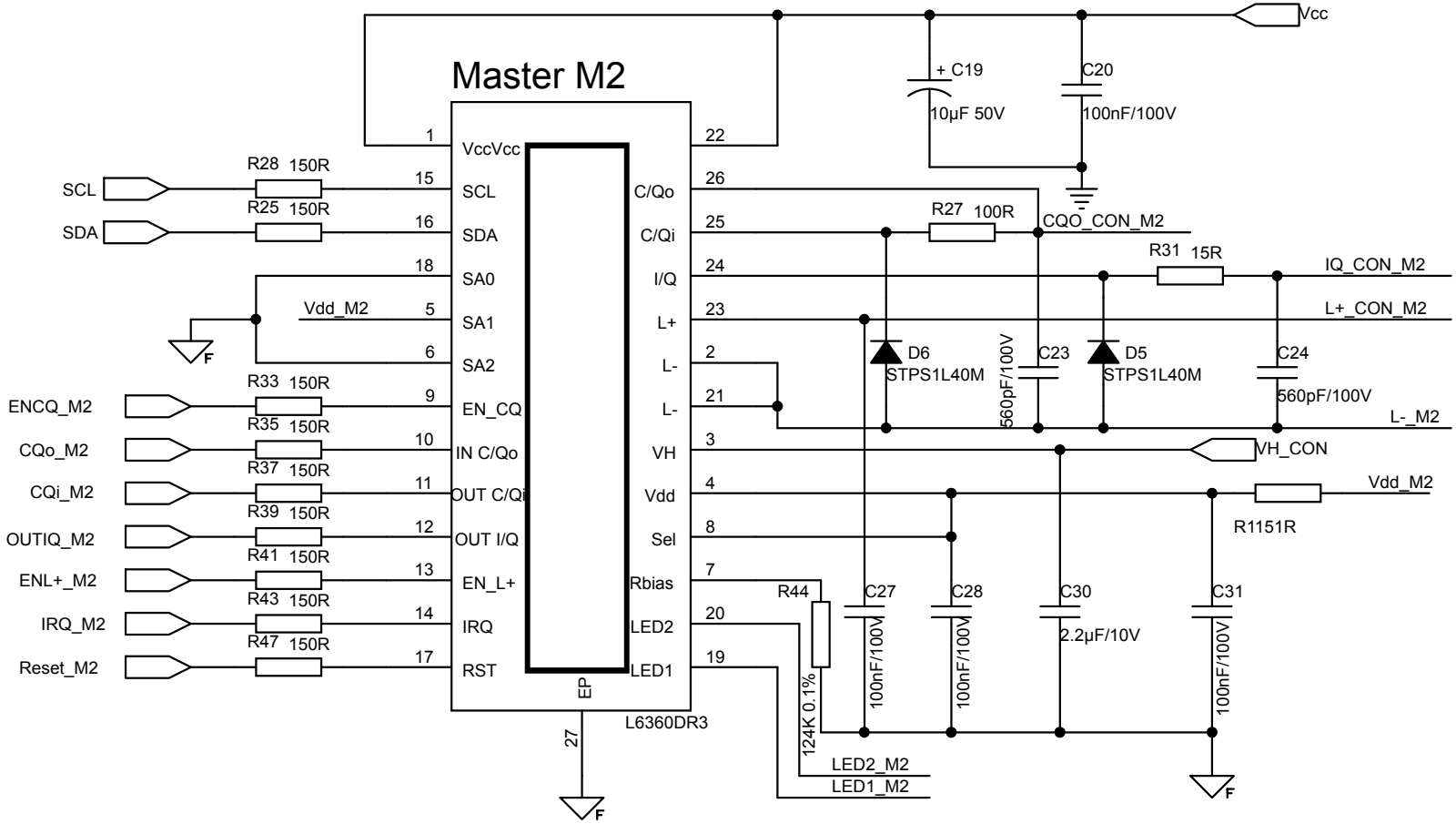


Figure 9. STEVAL-IDP004V2 circuit schematic (8 of 11)

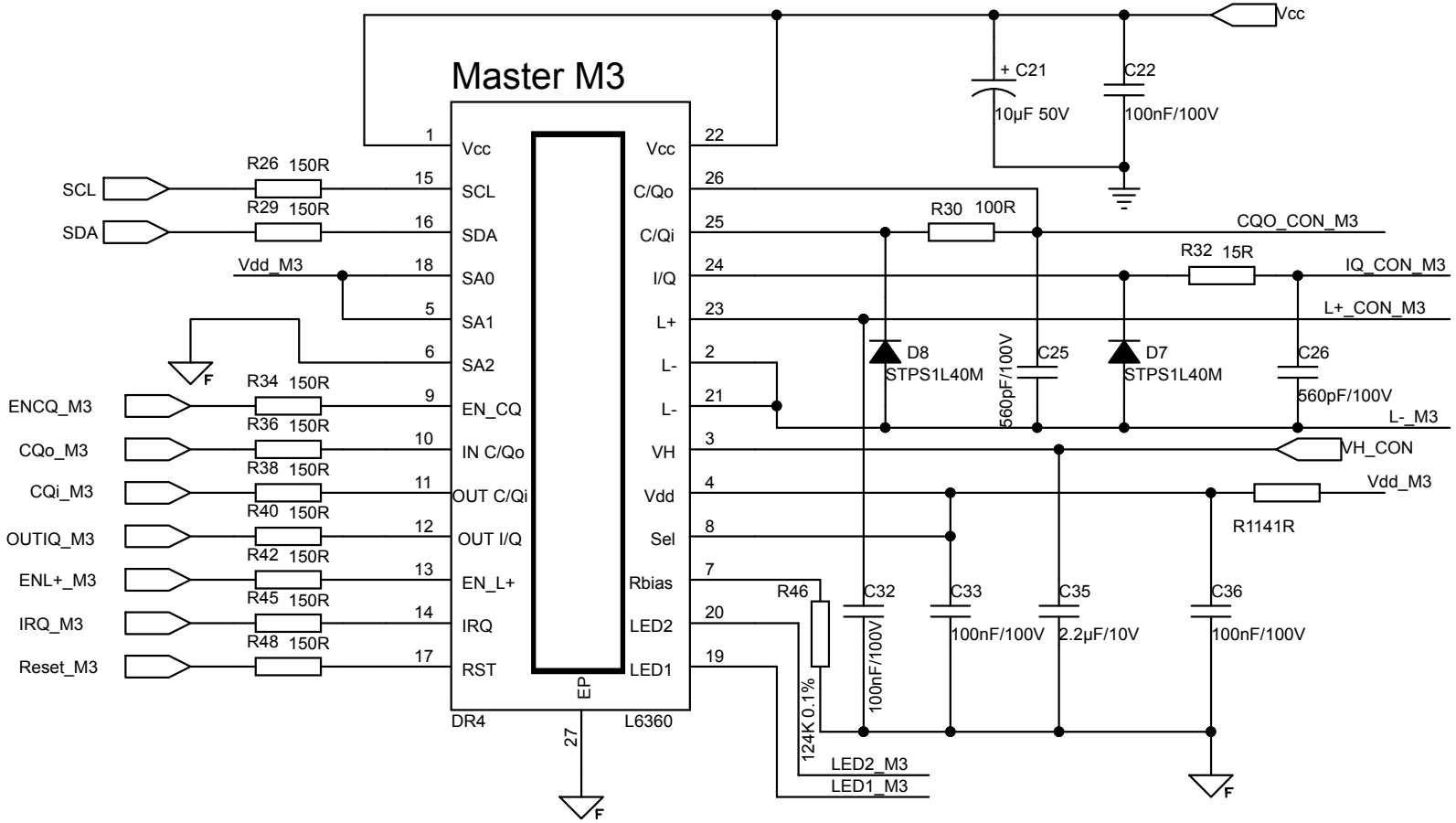


Figure 10. STEVAL-IDP004V2 circuit schematic (9 of 11)

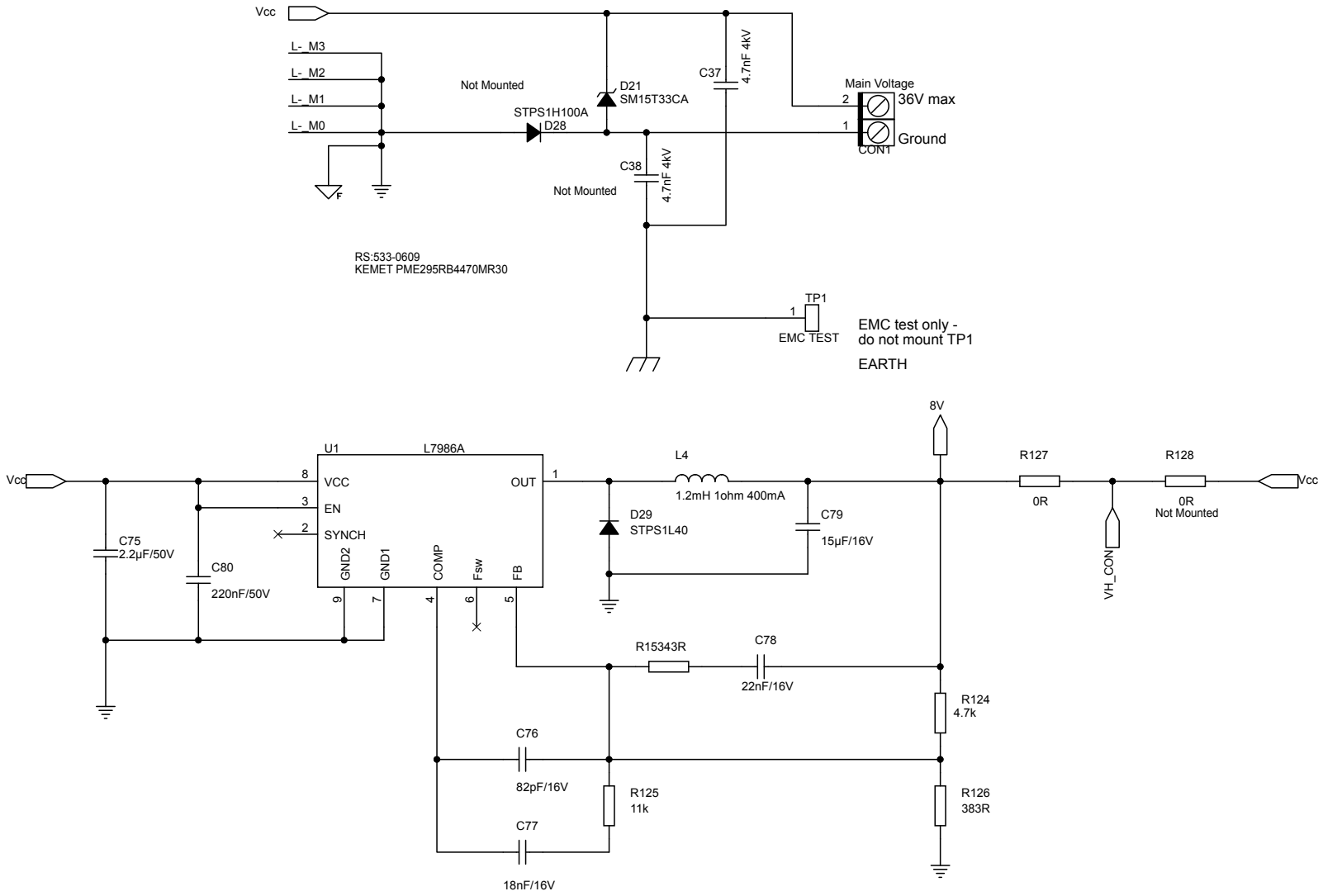


Figure 11. STEVAL-IDP004V2 circuit schematic (10 of 11)

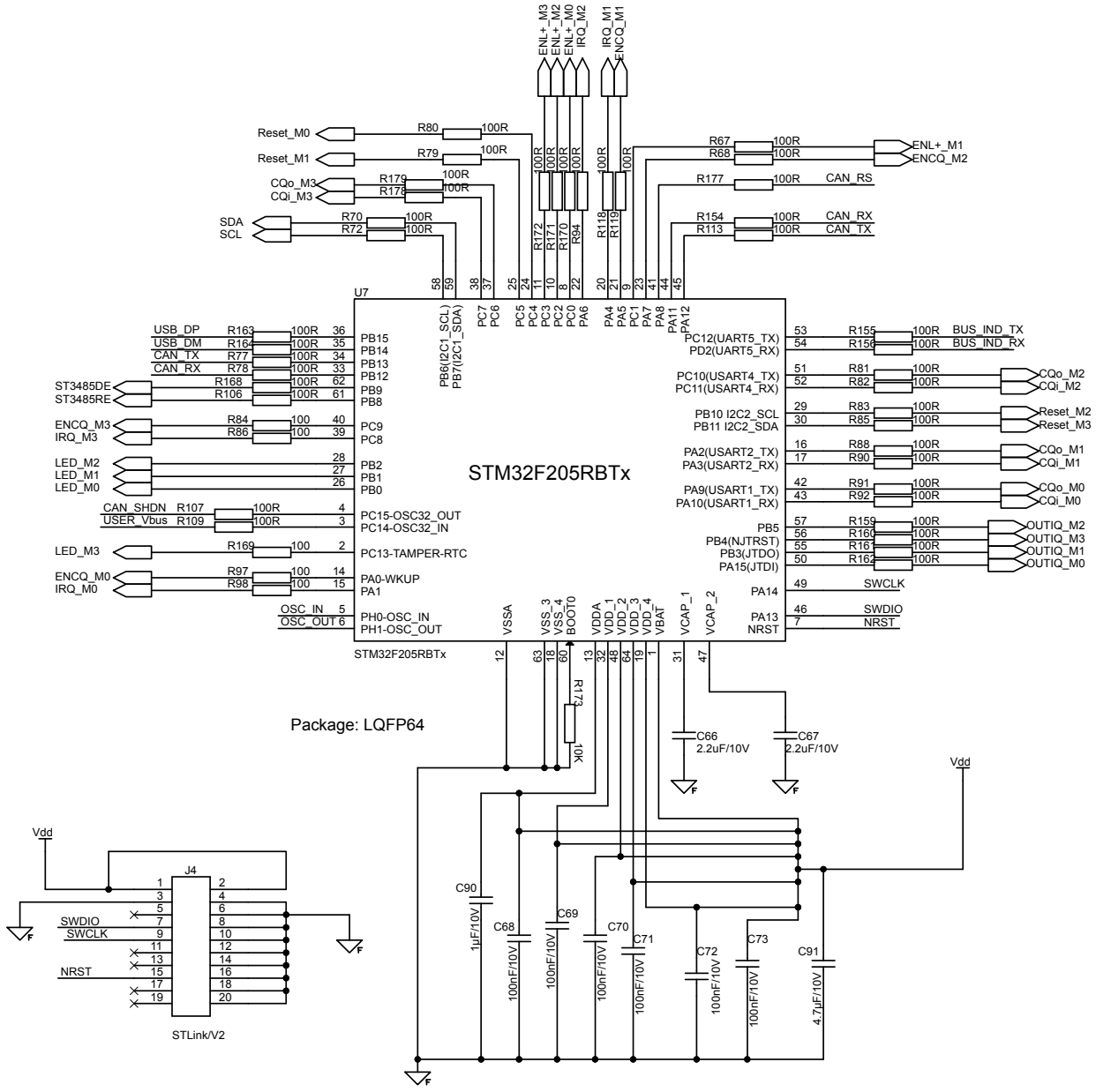
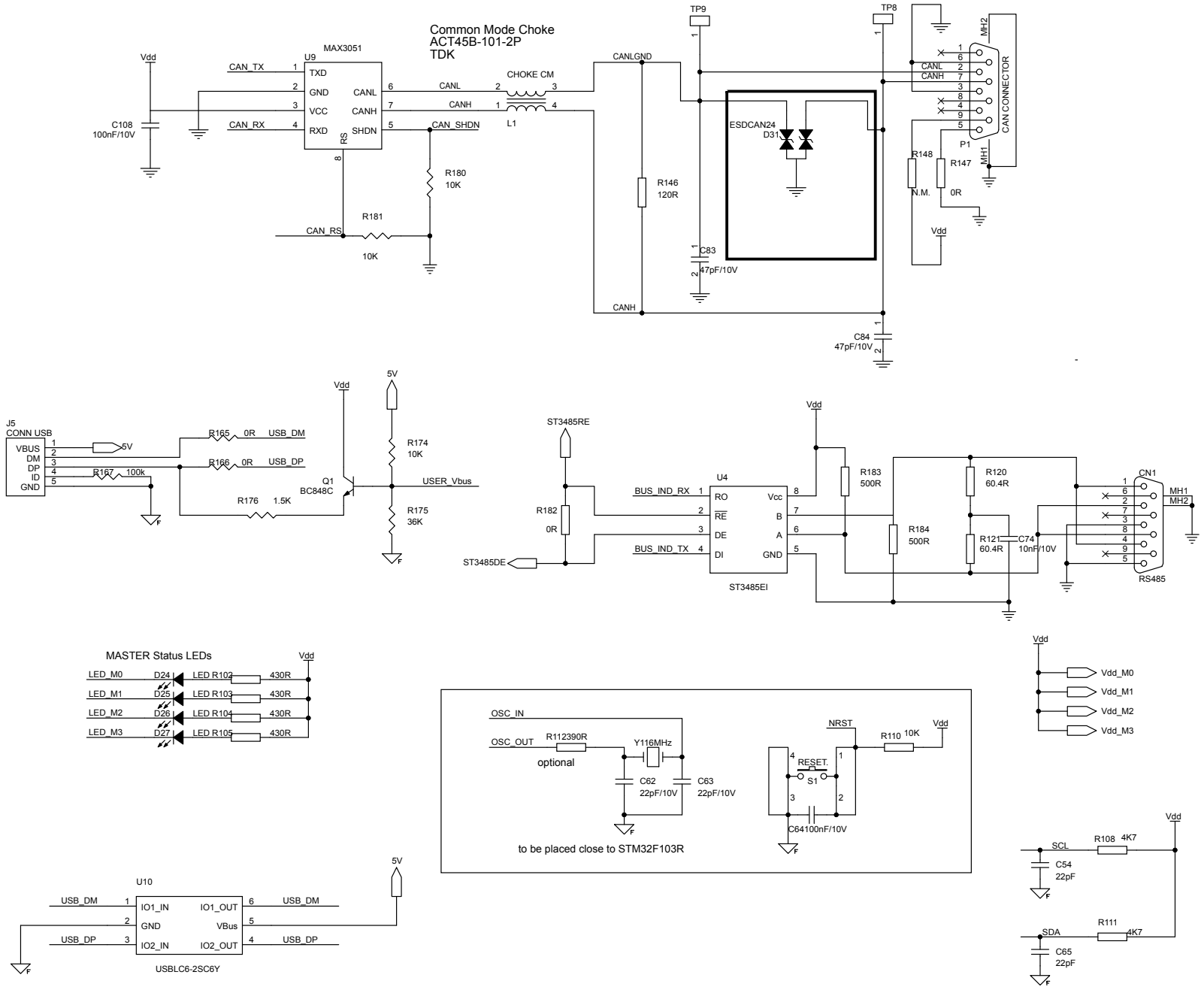


Figure 12. STEVAL-IDP004V2 circuit schematic (11 of 11)



Revision history

Table 1. Document revision history

Date	Version	Changes
16-Oct-2019	1	Initial release.
08-Apr-2025	2	Updated Description.

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