STW81200-EVB STSW-RFSOL002

Wideband RF synthesizer/VCO evaluation board and GUI

Data brief

Features

- PCB-mounted STW81200 ultra low noise RF fractional/integer IC synthesizer with integrated VCOs and LDOs.
- PC-compatible graphical user interface (GUI) giving:
  - Direct read/write access to device registers
  - Instant display of register field descriptions.

Description

The STW81200-EVB evaluation kit allows the user to program and operate the STW81200 RF fractional/integer synthesizer and its integrated VCOs and LDOs.

The kit includes PC-compatible software with a Graphical User Interface (STSW-RFSOL002) allowing the user to write and read all device registers. This gives direct control of circuit functions such as: operating frequency, reference frequency, input mode, charge pump current and low-power modes.

The user-oriented GUI aids understanding of the performance, features and characteristics of the STW81200 device under test in a laboratory environment. The GUI displays instant register descriptions when the user slides the mouse over the displayed areas, command buttons and fields.

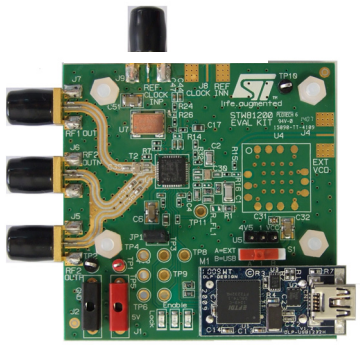

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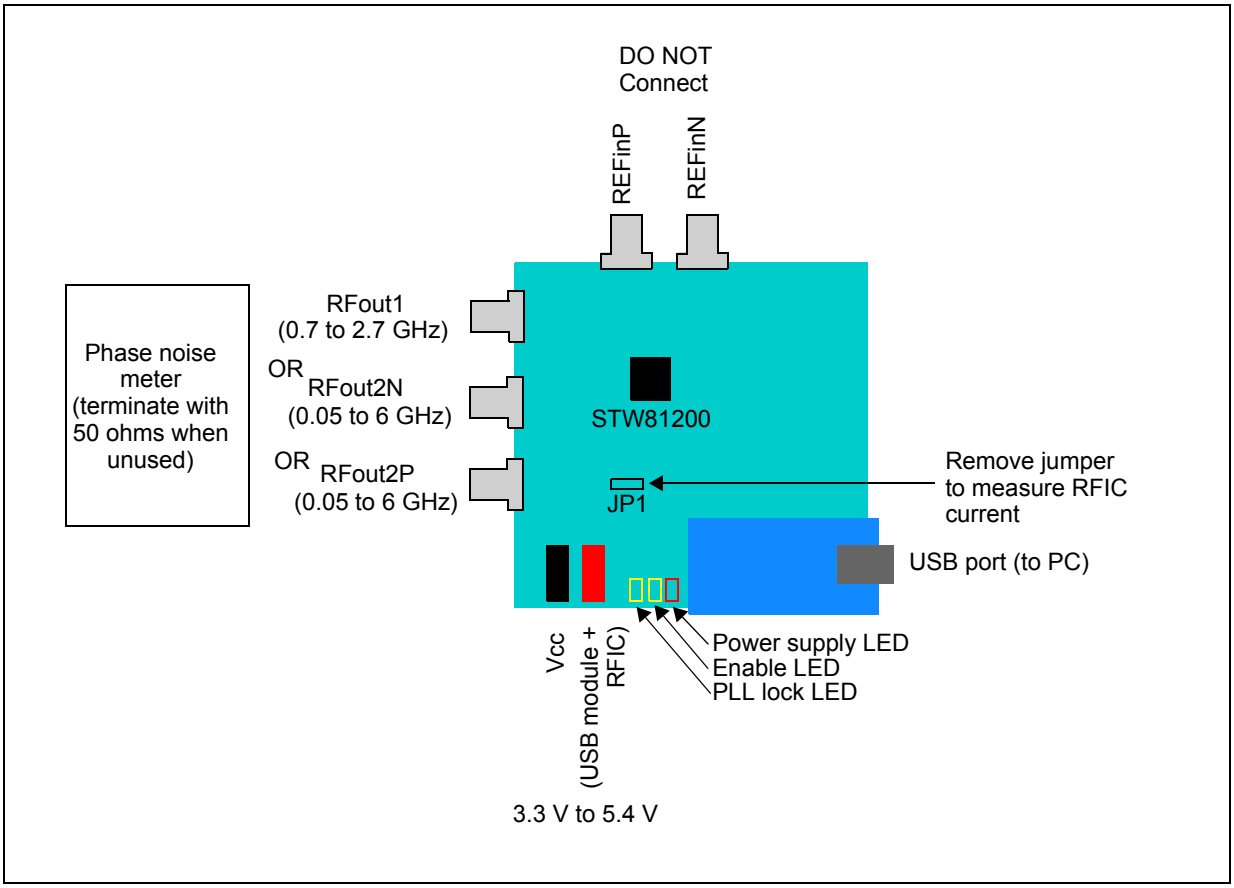
Figure 1. STW81200-EVB connections



1.1 RF outputs

For phase-noise meter connection (such as an Agilent E5052A/B or a spectrum analyzer):

- RFout1 is a differential output (limited by Balun bandwidth)
- RFout2P/N are single-ended outputs with full bandwidth available (50 MHz to 6 GHz). It is recommended to terminate unused ports with 50-ohm coaxial terminations.

1.2 Vcc

Power supply connection. USB power can be used instead of J1/J2 although this is not recommended. (Check the USB PC port current capability.)

1.3 USB (port B)

Provision for a USB cable connection to the PC running the STW81200-EVB GUI.

1.4 LEDs

These are active only if the STW81200-EVB GUI is running. From left to right:

- STW81200 is in LOCK state (green). The same information is available in the STW81200 EVAL GUI.
- STW81200 is ENABLED (green).
- An unregulated 5 V supply is applied from the power connectors or USB port (red).

1.5 EXT VCO

This is not used in the default setup, however it is included to support the use of an external VCO (the STW81200 has on-chip VCOs).

1.6 REFinP/N

This is not used in the default setup, however it is included to support the use of an external reference signal.

The STW81200-EVB incorporates a low-noise CMOS 100 MHz reference crystal oscillator (not temperature compensated) and a 50 MHz crystal which is not connected to the STW81200 in the delivered board configuration, but which can be connected with some simple soldering operations. (Some component configurations are not connected to the STW81200 in the delivered configuration.)

As the device supports different reference signal standards (CMOS, LVDS, LVECL) REFinP/N can be used to inject a reference signal from a low-noise synthesized signal generator. The REFin signal is critical for the phase noise and spur performance of the STW81200.

1.7 Enables/power down

Once connected to a supply, the STW81200, crystal oscillator, RF1/2 power-down control and status are available only through the STW81200 EVAL GUI.

No hardware switch needs to be set on the PCB (except for the optional on-board VCO selector).

2 Loop filter

Figure 2. Loop filter schematics

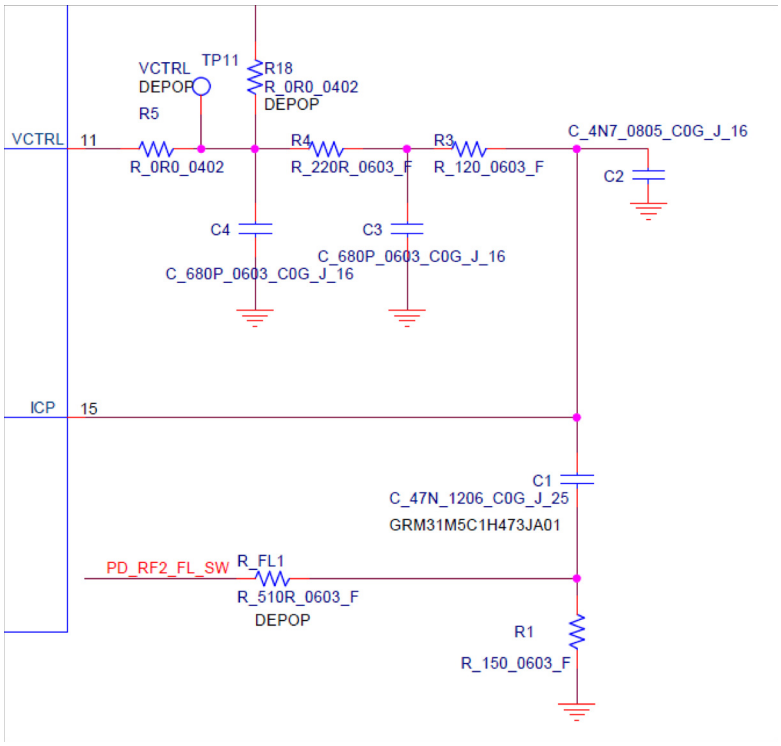


Table 1. Loop filter component choice

VCO freq	VCO gain	Charge pump	PFD freq	Loop BW	Phase margin
3000-4000MHz C2 = 4.7 nF	23-58MHz/V C1 = 47 nF	4.9mA R1 = 150 ohm	50 MHz R3 = 120 ohm	TBD C3/C4 = 680 pF	TBD R4 = 220 ohm
4000-5000MHz C2 = 4.7 nF	32-66MHz/V C1 = 47 nF	4.9mA R1 = 150 ohm	50 MHz R3 = 120 ohm	TBD C3/C4 = 680 pF	TBD R4 = 220 ohm
5000-6000MHz	43-78MHz/V	4.9mA	50 MHz	TBD	TBD
C2 = 4.7 nF	C1 = 47 nF	R1 = 150 ohm	R3 = 120 ohm	C3/C4 = 680 pF	R4 = 220 ohm

Note: The VCO gain varies appreciably. Although not demonstrated in these instructions, the charge-pump current is automatically adjusted to partially account for variation due to VCO gain with loop control voltage. It can also be manually tuned versus VCO frequency.

Typically the loop filter/charge pump gain used is a good compromise between spur rejection and integrated phase noise. Loop bandwidth is set to approximately to 50 kHz and loop phase margin is set to approximately 55°.

3 STW81200-EVB GUI setup

Before using the STW81200-EVB the FTDI drivers must be installed. The following quick setup and power-on sequence can then be performed:

1. Supply the STW81200-EVB through J1/2.
2. Connect a USB cable from the PC to the STW81200-EVB board.
3. Check that the USB device is properly recognized by the PC and that drivers are installed (CDM20814_Setup).
4. Start the GUI (STW81200GUI.exe). The window shown in *Figure 4: STW81200-EVB GUI window* should be displayed.
5. Check the GUI message list (USB Port is open, communication OK).
6. Configure all user settings (default or load previously defined configuration).
7. Click the WRITE button of the GUI to upload settings to the STW81200 registers.

The USB communication is automatically established between the GUI and the STW81200 when the GUI is started (see point 4 of GUI setup above). This ensures that if the STW81200 is disconnected or its power supply is removed, the GUI detects this and gives a warning. The user must close the GUI, restore hardware connections and re-open the GUI to re-establish the communication before being able to WRITE to the registers again.

The GUI frequently uses the message list window to inform the user of any action being performed on the device, and to give a real-time aid-to-understanding of what is happening inside the STW81200. We strongly suggest reading these messages.

For each of the objects present inside the GUI a brief description is available for a few seconds when the user passes the mouse cursor over the object. In this way the GUI passes detailed information to the user, minimizing the need for separate documentation.

Notes about RFIC current consumption measurement in the STW81200-EVB

The STW81200-EVB has 3 on-board active parts:

- USB module
- crystal oscillator
- STW81200

All the electronics is supplied through J1/J2 banana connectors (3.6 V/5.4 V) or through a USB cable (see schematic, s1). Using a USB cable is not recommended for laboratory measurements, but it can be useful if the user wants to exploit different configurations in an office environment. The following should be noted:

- The USB module and STW81200 are supplied directly from J1/J2
- The crystal oscillator is supplied through internal low voltage regulator of STW81200.

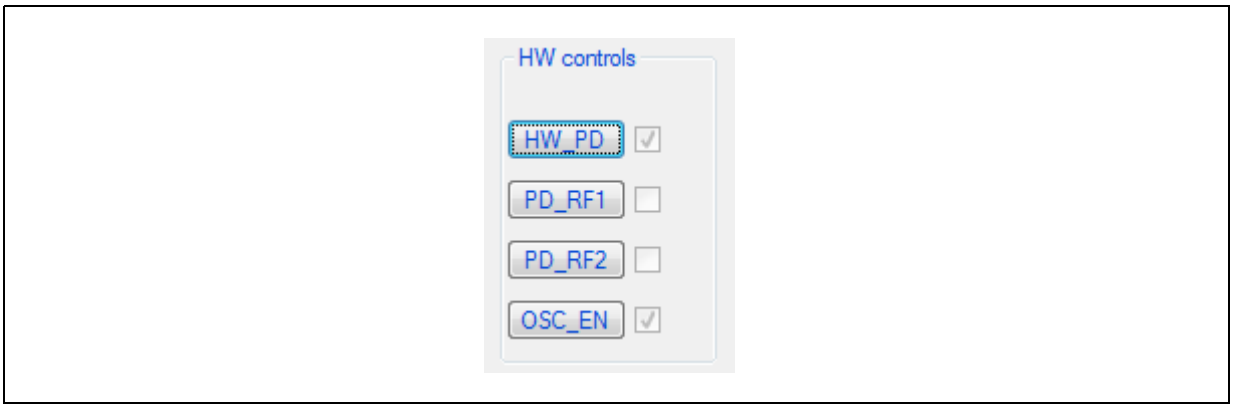
Typical currents measured through J1/J2 are the sum of the USB module (~80 mA), STW81200 and crystal oscillator (~10 mA).

To do accurate measurements of STW81200 and crystal oscillator, current jumper JP1 can be used.

The correct procedure for accurate measurements of the RFIC current is as follows:

1. Insert an ammeter in the JP1 power line. Check that the voltage drop through JP1 is negligible.
2. Select STW81200 HW_PD and OSC_EN (*Figure 3*). Current consumption is approximately 15 mA (5 mA STW81200 + 10 mA crystal oscillator).
3. Disable OSC_EN and calculate the consumption of the crystal oscillator (IccOSC)
4. Program the STW81200 in the required configuration and/or operating mode.
5. Measure current through JP1 (IccOperating).
6. Calculate IccSTW = IccOperating - IccOSC.

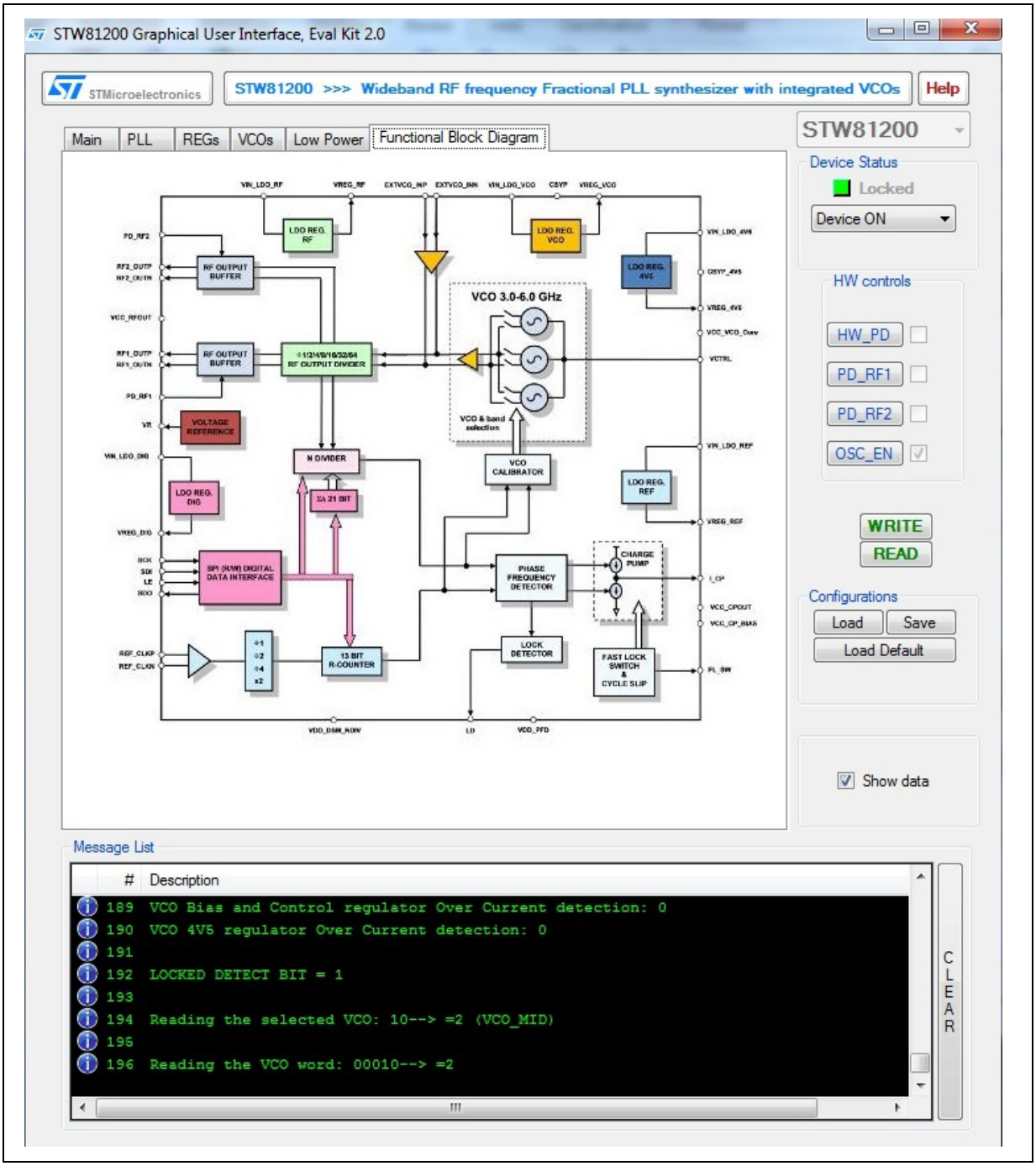
Figure 3. Hardware control buttons



4 STW81200-EVB GUI overview

The STW81200-EVB GUI provides different tabs to set all available STW81200 features as detailed in this section. The device status control can be used as an alternative to HW_PD to set the STW81200 to ON or **power down** mode. If ON, a green/red LED indicates if it is in locked/ unlocked state.

Figure 4. STW81200-EVB GUI window



Four hardware controls are available:

- **HW_PD** sets the STW81200 to power-down or active mode
- **PD_RF1**/2 enables the RF outputs
- **OSC_EN** acts on the on-board oscillator standby pin.

These controls are effective immediately (there is no need to perform a WRITE command).

Two buttons are available to **WRITE** or **READ** all STW81200 registers.

GUI configurations can be saved or loaded through the following buttons:

- **Load**: loads previously saved configuration from file
- **Save**: saves current configuration to a file
- **Load Default**: restores the default configuration.

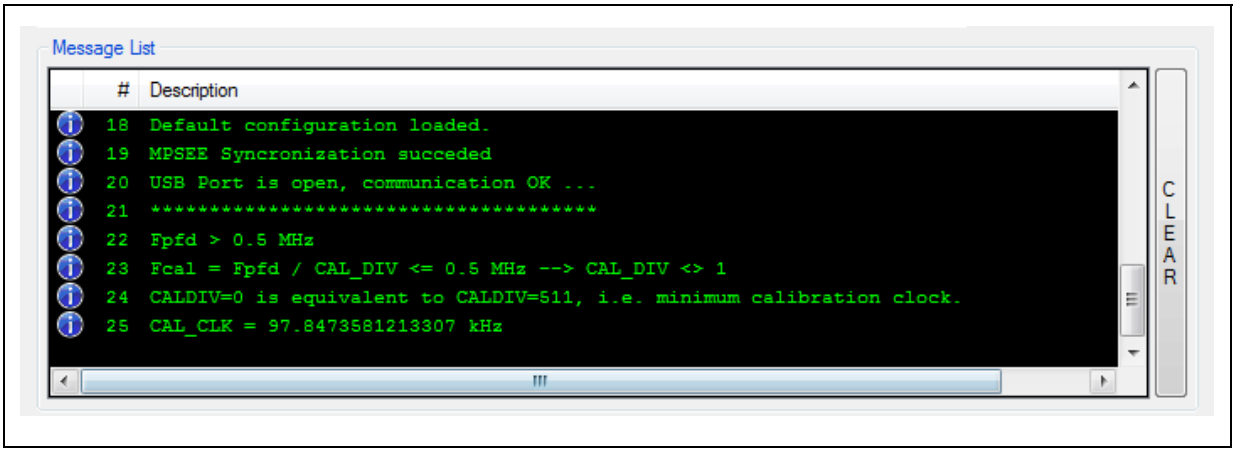
The user can show/hide register content (after a WRITE/READ command) in the Message List window using the Show Data check button.

The **message list** is a powerful instrument that supports the user during normal operation of the GUI. It gives useful information about:

- FTDI communication information
- STW81200 ID
- Registers R/W
- Lock detection
- VCO/Word selected by calibrator or user
- Regulators ready/over current detection.

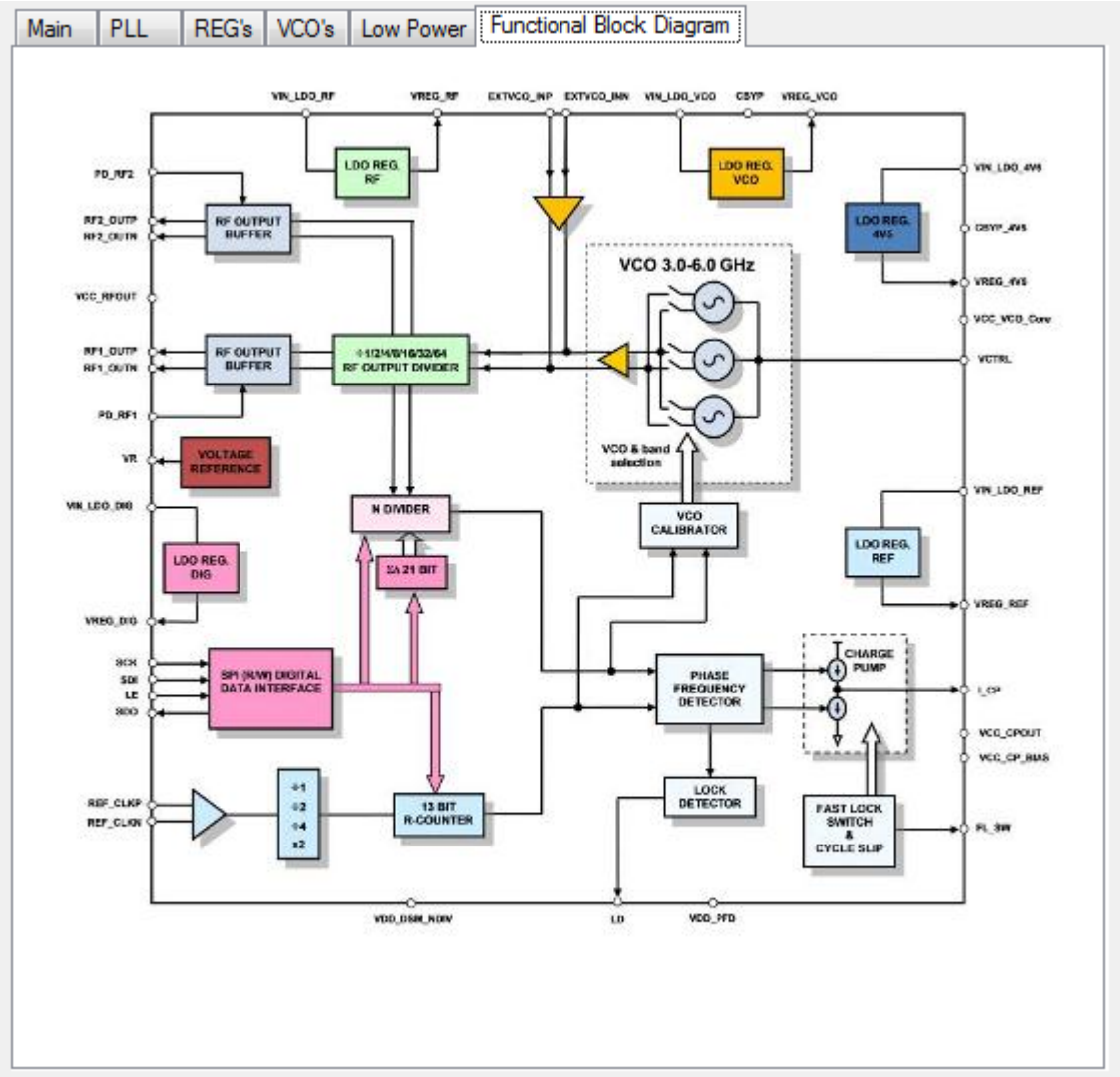
The GUI always checks (poll time = 1s) the SWT81200 lock and ID. This feature is provided so that any unintentional USB cable disconnect or other incorrect user intervention is reported so that the user can correct the issue.

Figure 5. Message output example



For quick reference the circuit block diagram is given in *Figure 6*. Reading the data sheet is recommended for a detailed understanding of all circuit features, blocks and registers.

Figure 6. STW81200-EVB functional block diagram



5 STW81200-EVB GUI programming tabs

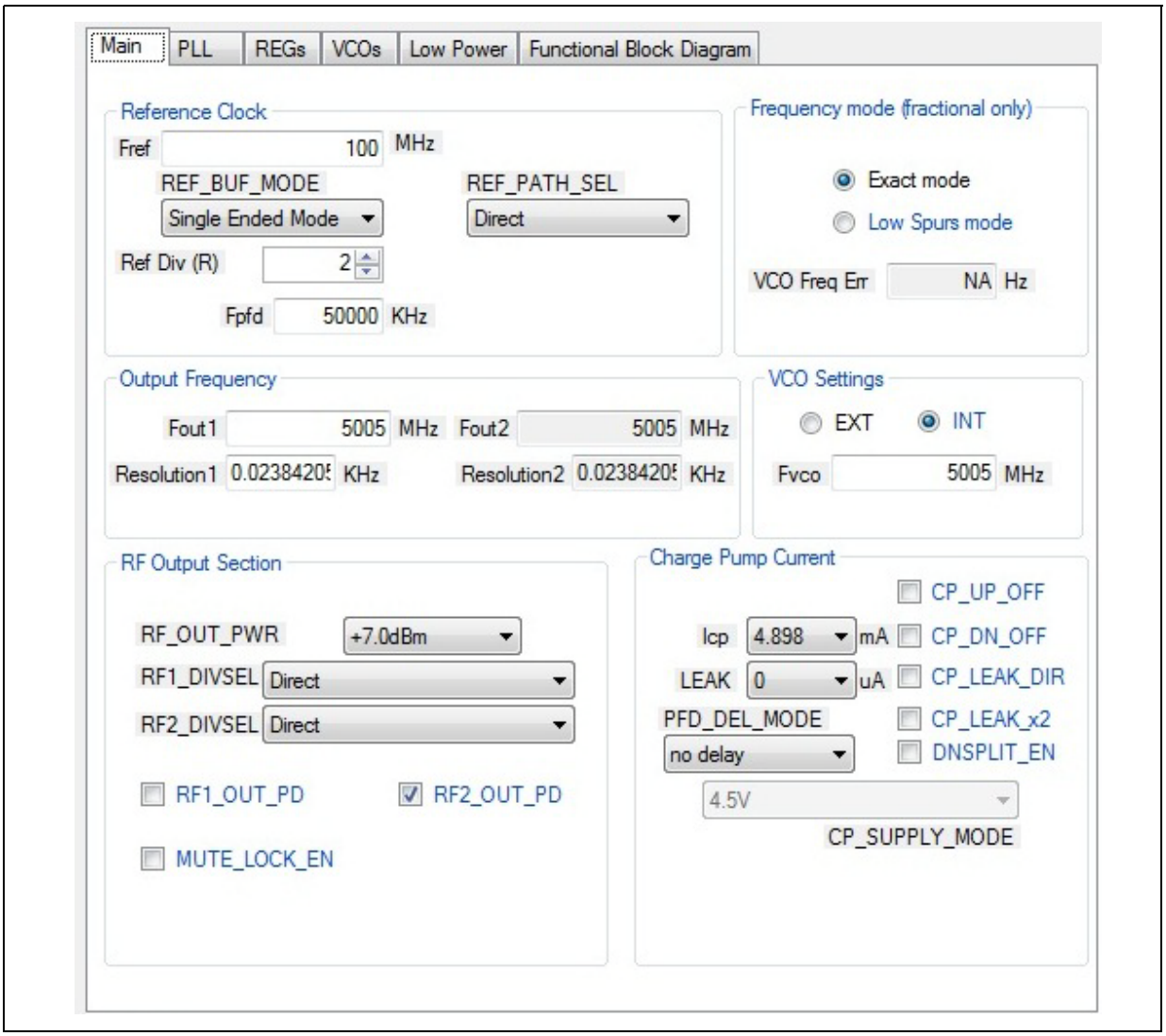
Five tabs are available to control the different parts and user modes of the STW81200.

- *Section 5.1: Main tab*
- *Section 5.2: PLL programming tab*
- *Section 5.3: Regulator programming tab*
- *Section 5.4: VCO programming tab*
- *Section 5.5: Low-power programming tab*.

5.1 Main tab

The **Main** tab (*Figure 7*) groups all the commonly used controls and resulting information required for basic use of the STW81200.

Figure 7. STW81200 EVAL main tab



The Main tab is divided in six main sections detailed below.

5.1.1 Frequency mode (fractional only)

The user can select between two synthesizer operating modes. Although in most of the configurations the differences are negligible, in some cases mode selection can be useful:

Frequency modes (exact or low spur) are enabled only if the fractional divider is used (NINT < 508).

- **Exact mode**: due to the flexible architecture of the delta sigma modulator embedded in STW81200, the synthesized frequency is **exactly** the frequency requested by user.
- **Low Spur mode**: in this mode there is an improvement on spur signals at the expense of a slight frequency error. The error is less than half resolution and it is indicated in the Freq Err value. Under typical operating conditions the error is < 0.01 ppm.

5.1.2 Reference Clock

The user must enter the reference frequency (both from an external source or crystal oscillator), reference divider ratio or PFD frequency.

The relationship Fref=R*Fpfd is always guaranteed by the GUI.

5.1.3 Output frequency

Output frequency indication of RF1 and RF2 (the available resolution is shown based on exact or low spur mode).

The user can enter the RF1 output frequency and VCO frequency directly. The RF2 output frequency is calculated according to the RF1/2_DIVSEL value.

Resolution1/2 is a read-only field. It calculates the current frequency step obtained by increasing FRAC. It is controlled by MOD (a higher MOD value gives lower frequency resolution. (See *Figure 8: STW81200 EVAL PLL programming tab*.)

5.1.4 VCO settings

The user must choose whether to enable the internal VCO or an external one (if mounted on STW81200-EVB or connected through J4). The desired VCO frequency and EXTERNAL VCO (Fvco) are set here.

Note: VCO oscillator frequency values of 3000 MHz to 6000 MHz are allowed if using the internal VCO.

The user can enter VCO frequency and the RF1, RF2 output frequency is calculated according to the RF1/2_DIVSEL value.

5.1.5 RF output section

This section sets the RF1/2 output power, RF1/2 dividers and RF1/2 power down parameters.

The user can modify RF1/2_DIVSEL, VCO, RF1, RF2 and the output frequency is calculated accordingly.

5.1.6 Charge pump current

The nominal charge pump current (Icp) can be set to control loop parameters (bandwidth and phase margin).

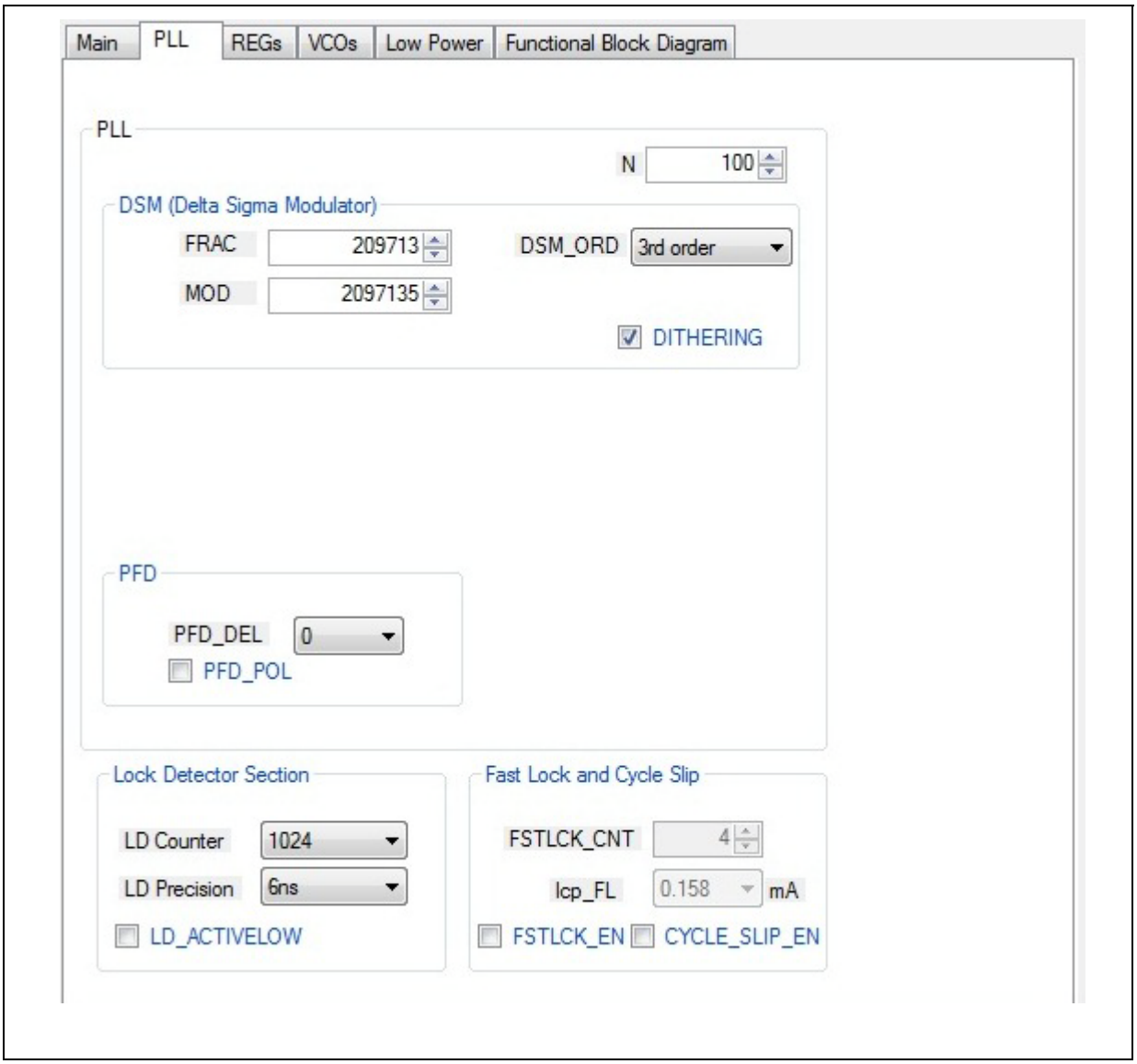
Different settings are used to mitigate the integer boundary spurs level. It is recommended to leave these settings unchanged.

Charge pump supply mode is set according to REGVCOHV_VOUT (see *Figure 9*) in the **regulator** tab. The user does not need to set this field in normal use.

5.2 PLL programming tab

This section details the **PLL settings** tab shown in (*Figure 8*).

Figure 8. STW81200 EVAL PLL programming tab



To exploit all of the advanced features of the STW81200, the **PLL settings** tab must be used.

All these settings are synchronized with affected parameters in the Main TAB. If, for example, the user modifies the frequency in the **Main** tab, the corresponding DSM settings are updated and vice versa, so all GUI information remains congruent.

It is recommended to act on these parameters taking into account data sheet information, in particular regarding the DSM settings, as this can affect the performance. The GUI automatically selects the best values for each frequency configuration based on an internal algorithm.

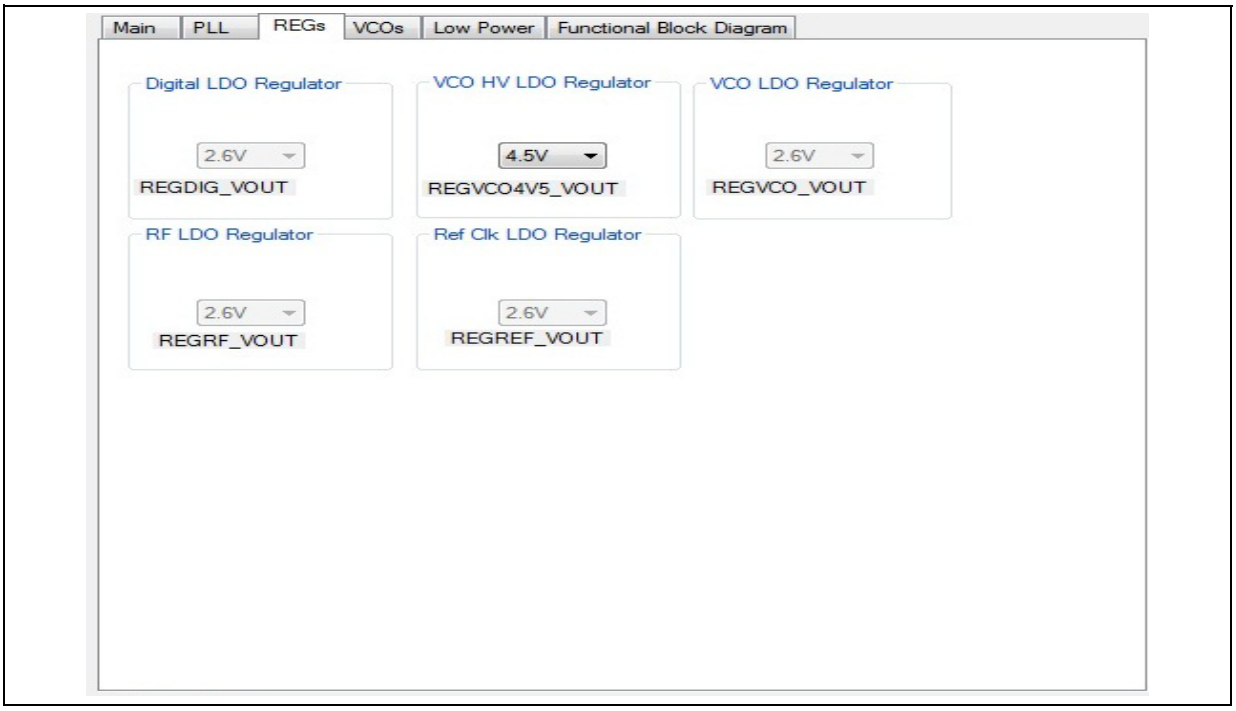
It is divided into three main sections

- **PLL**:
  - DSM: FVCO=FPFD*(N+FRAC/MOD+DITHERING/(2*MOD) where DITHERING=0 or 1
  - PFD_DEL: PFD anti-backlash delay
  - DSM_ORD: Delta sigma modulator order. Typically 3rd order is used.
- **Lock detector**: Sets the lock detector counter and precision to trim LOCK detector speed and accuracy under different PLL settings. This also allows changing the polarity of the LOCK detector PIN (LD_ACTIVELOW). The GUI and STW81200-EVB board LEDs are not affected by the polarity settings (they always show LOCK condition if met independently from LD_ACTIVELOW)
- **Fast lock and cycle slip**: Enable and set fast lock or cycle slip function, see the STW81200 data sheet *[1]* for details.

5.3 Regulator programming tab

This section details the linear regulator settings tab (**REGs)** shown in *Figure 9*.

Figure 9. Linear power regulators settings tab



The STW81200 embeds 5 LDOs for best supply noise rejection and block decoupling.

Digital, VCO, RF, and PLL regulator default values cannot be changed by the user (they are shown for information only). The VCO HV regulator must be set according to the external power supply (between 3 V and 5.4 V), assuming that a 300 to 400 mV drop has to be guaranteed between the unregulated and regulated voltage.

Typical configuration settings are:

- Unregulated voltage VIN, 5.3 V<VIN<5.4 V, REGVCOHV_VOUT=5.0 V. Limits are set taking into account that 5.6 V is the AMR for STW81200 and 5.3 V is the minimum voltage to guarantee 300 mV drop
- Unregulated voltage VIN, 4.8V<VIN<5.4V, REGOUTHV_VOUT=4.5V. This is the most commonly used setting in infrastructure applications as a 5.0 V line is available. It is the GUI default value.
- Unregulated voltage VIN, 3.6 V<VIN<5.4 V, REGOUTHV_VOUT=3.3 V. This is commonly used in low-power infrastructure applications.
- Unregulated voltage VIN, 2.9 V<VIN<5.4 V, REGOUTHV_VOUT=2.6 V. This is commonly used in ultra low-power infrastructure applications.

Acting on regulator voltage, the GUI modifies also the CP_SUPPLY_MODE, VCO_Ampl and RF_OUT_PWR so that appropriate settings are always used. (An exception is made for RF_OUT_PWR when restoring a higher regulator voltage)

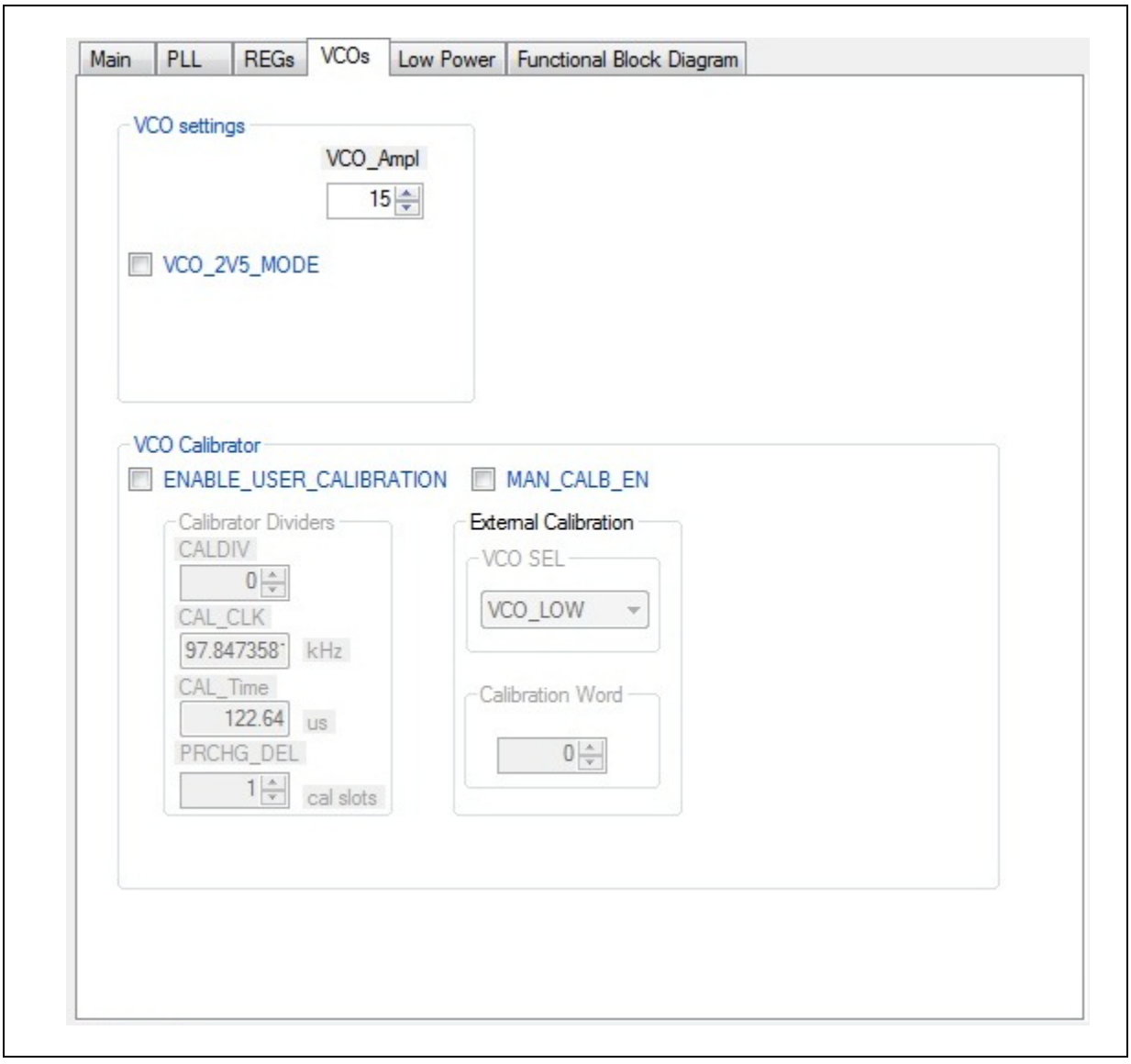
These settings can be used together with low-power options. There is always a balance between STW81200 dissipated power and performance. It is recommended that the user

tests the wanted configuration to check, in the application, the power dissipation against desired performance.

5.4 VCO programming tab

This section details the VCO settings tab shown in *Figure 10*.

Figure 10. VCO settings tab



The tab is divided in two main sections:

- **VCO settings**: VCO_Ampl allows the user to balance VCO noise and current consumption. A higher value corresponds to higher current consumption and to better VCO phase noise performance. It is set according to REGVCOHV_VOUT in the Regulator tab. The user does not need to modify this field.
- **VCO Calibrator**
  Enable_user_calibration: activates parameters associated with clock-frequency calibration (derived by dividing PFD clock by CALDIV). Pre-charge delay can be used to obtain more accurate results. Overall calibration time is also calculated. The STW81200 has 3 integrated VCOs with 32 bands (VCO_WORD) identified in a specific register.
  There are 2 main operating modes:
  - **Automatic calibration** (default). The user inserts the required frequency and WRITEs the corresponding registers. The device runs an internal calibration algorithm (calibration time is indicated in CAL_Time) that finds the most appropriate VCO/VCO_WORD value and synthesizes the frequency. The reference signal is needed to perform calibration.
  - **Manual VCO/VCO_WORD register set**. The calibration circuit is disabled and the VCO/VCO_WORD can be programmed immediately (there is no need to wait for CAL_Time to elapse). This feature is useful in fast frequency-hopping applications. The user is may run off-line calibration of a single or a multiple set of frequencies, read VCO/VCO_WORD values for each channel and store these registers, then reuse the previously-stored appropriate VCO/VCO_WORD.

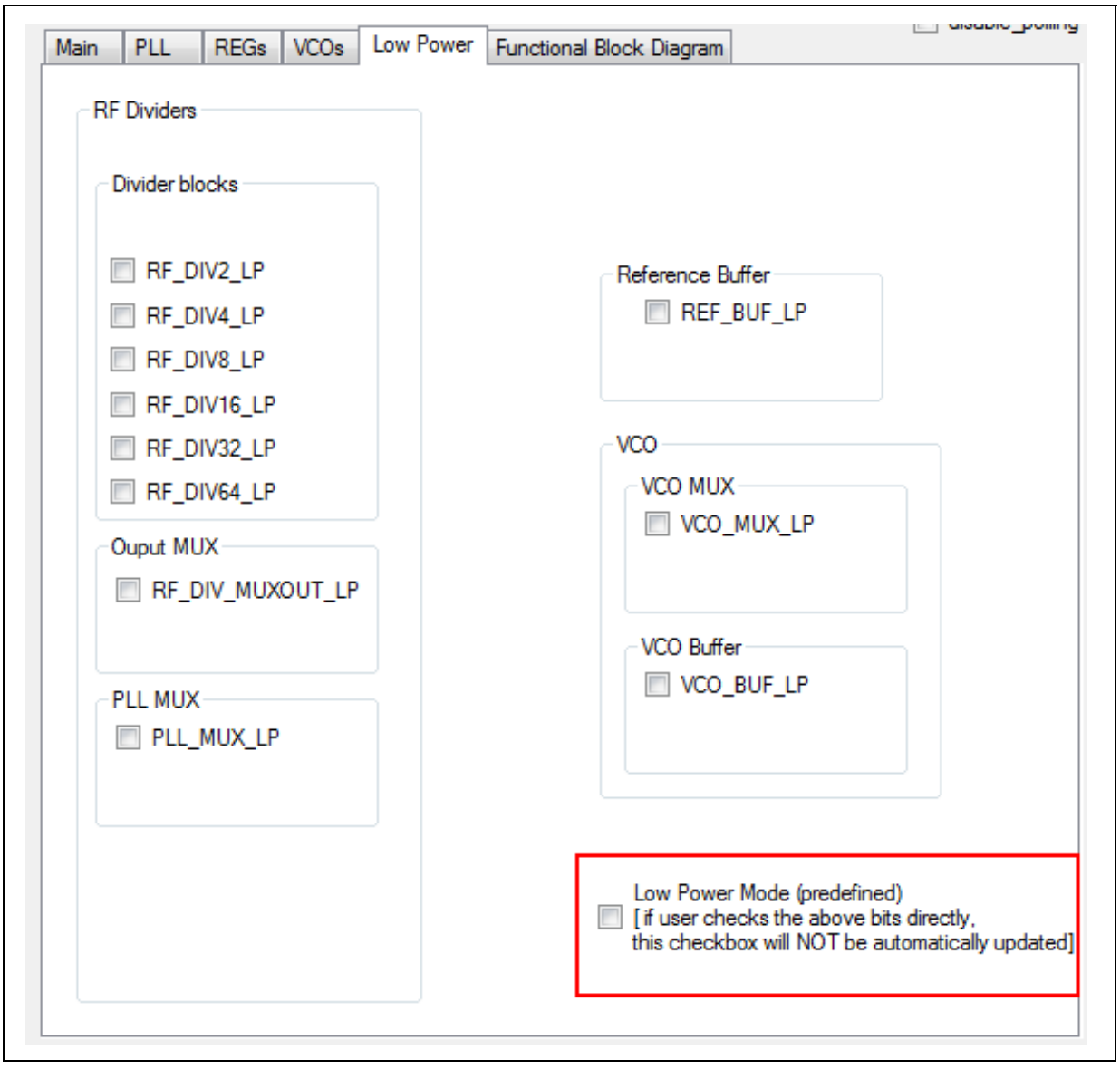
    As in fast frequency hopping applications, overall settling time has to be minimized, it is also possible to use double buffering for the registers the user needs to modify (see STW81200 datasheet *[1]* for details). The GUI enables the double-buffering feature by default.

    External calibration is enabled by CALBWORD_SET. This disables the internal calibration procedure, forcing VCO and WORD values. This is used if previous calibration data is to be reused. In this case the overall settling time for a frequency change is reduced as the STW81200 does not run the calibrator.

5.5 Low-power programming tab

This section details the low-power programming tab shown in *Figure 11*.

Figure 11. Low-power programming tab



Each of the sections contained in this TAB allow the user to apply low-power mode to respective circuit sections. It allows the user to balance overall current consumption against performance.

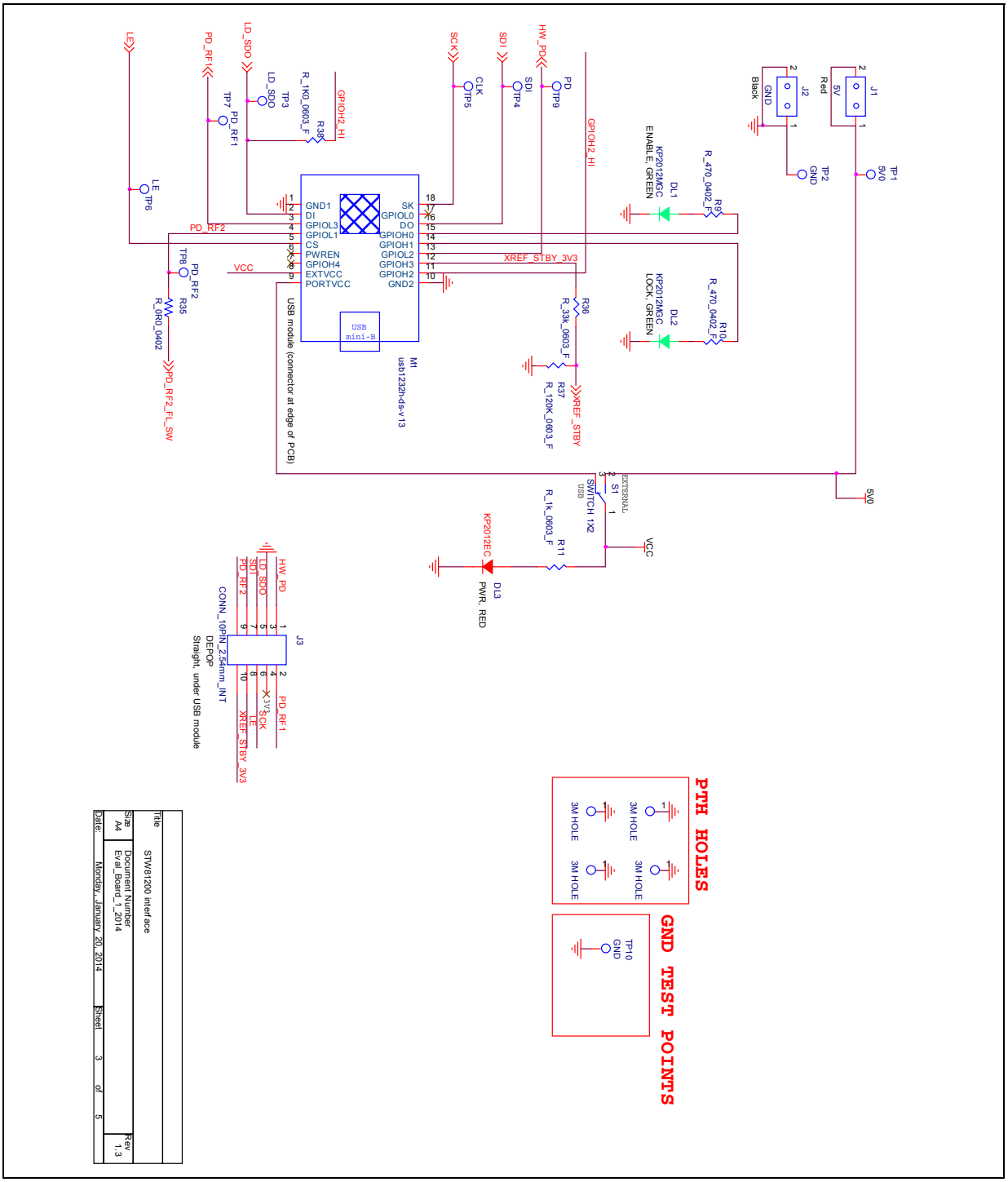
As many combinations of settings are possible, it is recommend to use the predefined configuration by checking the ‘Low power mode’ control shown in *Figure 11*.

Note: For low-power consumption configurations, please use the 3 config files provided.

Not all circuit parts are always on (for example if Fout = 2700 MHz only DIV2 is on and RF_DIV4/8/16/32/64_LP have no effect).

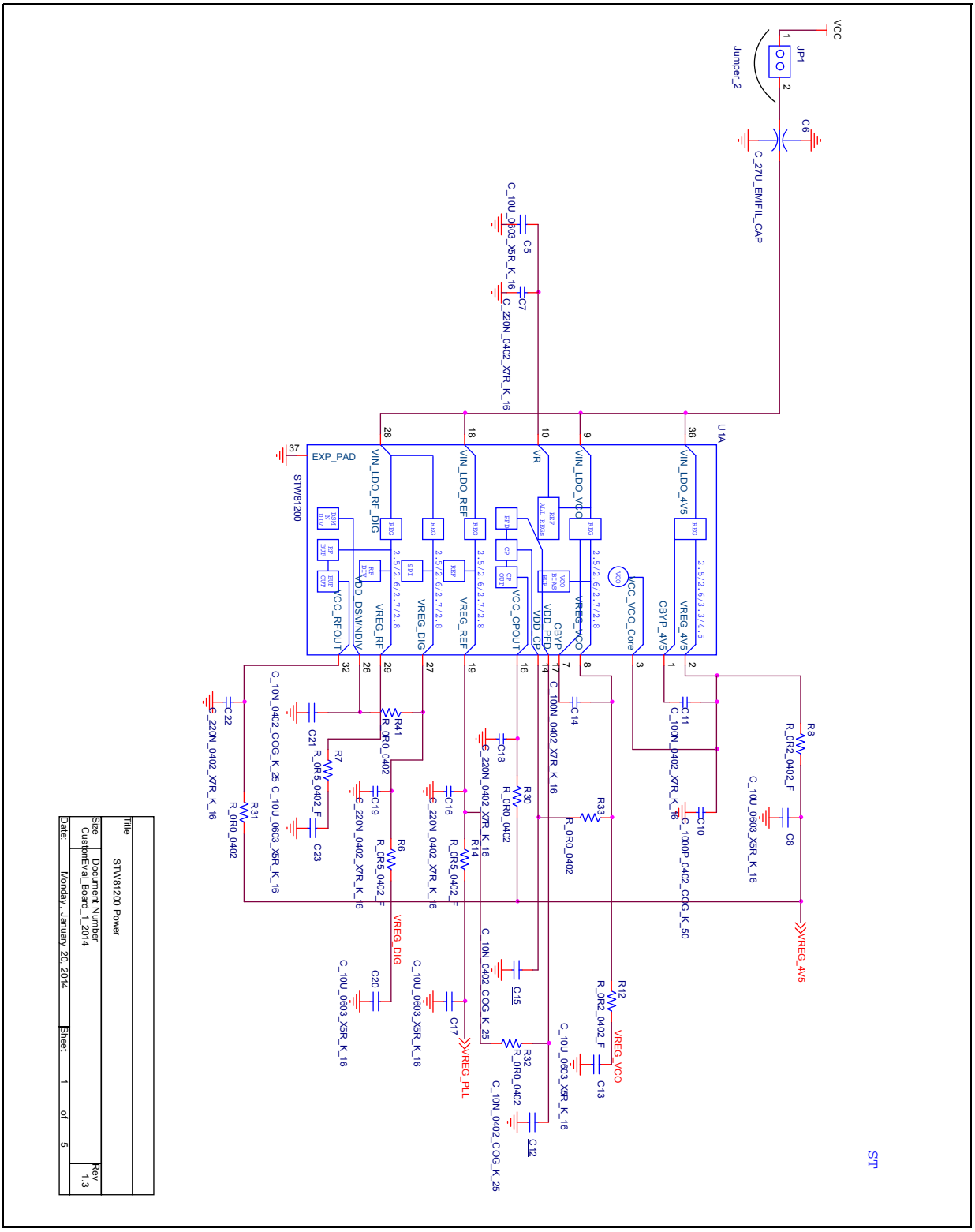
6 STW81200-EVB schematics

Figure 12. STW81200-EVB interfaces schematic



Note: Updated part values and part numbers are given in Section 7: STW81200-EVB BOM.

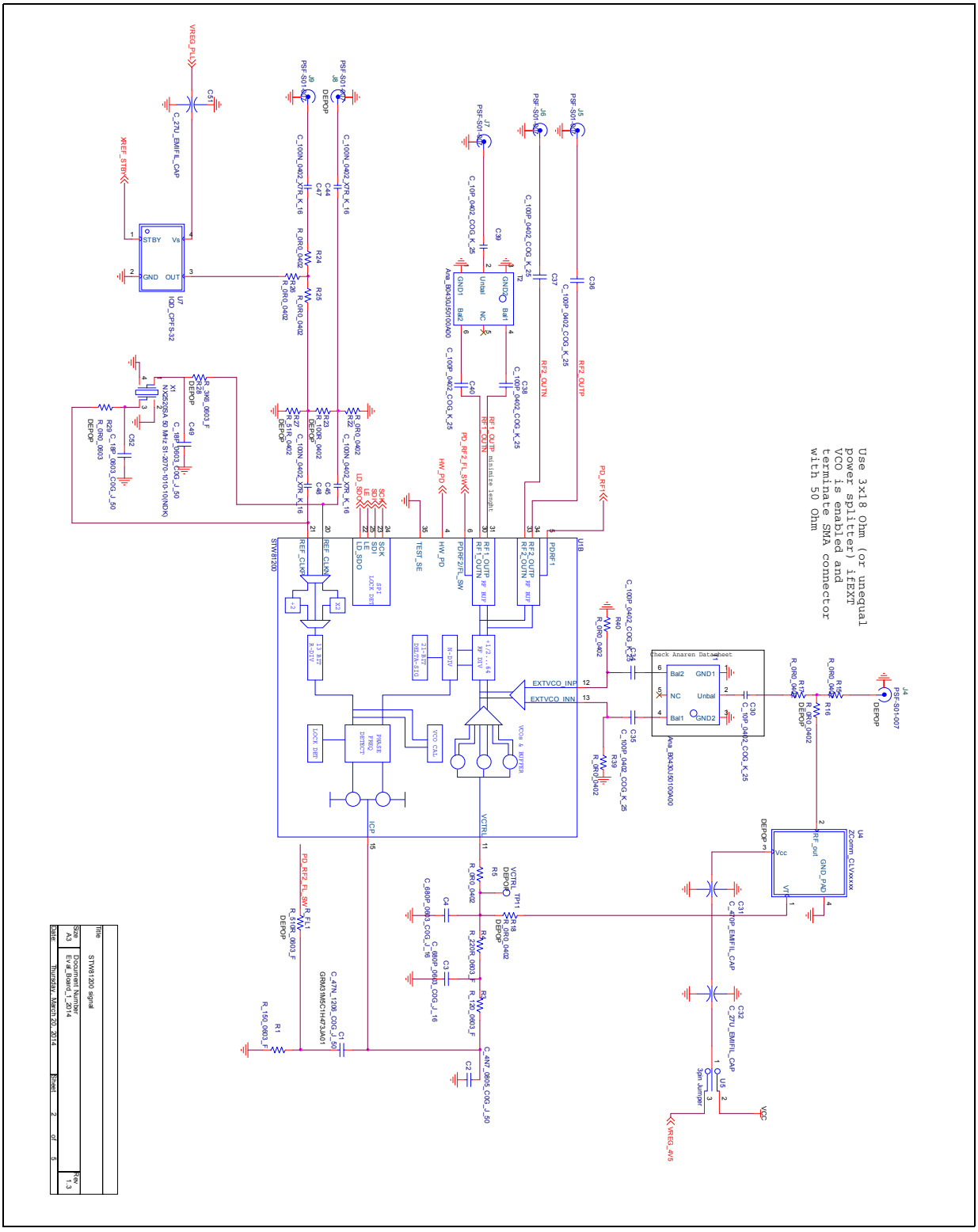
Figure 13. STW81200-EVB power supply schematic



Title	STW81200 Power		
Size	Document Number		Rev
Custom	Eval_Board_1_2014		1.3
Date:	Monday, January 20, 2014	Sheet 1 of 5	

Note: Updated part values and part numbers are given in Section 7: STW81200-EVB BOM.

Figure 14. STW81200-EVB Schematic – analog /RF signals



Note: Updated part values and part numbers are given in Section 7: STW81200-EVB BOM.

7 STW81200-EVB BOM

Table 2. STW81200-EVB BOM

Reference	Part	Manufacturer	Part Number	Populated
C1	C_47N_1206_C0G_J_50	Murata	GRM31M5C1H473JA01	Y
C2	C_4N7_0805_C0G_J_50	Murata	GRM2165C1H472JA01	Y
C3,C4	C_680P_0603_C0G_J_16	Murata	GRM1885C1E681JA01	Y
C5,C8,C13,C17,C20, C23	C_10U_0603_X5R_K_16	Murata	GRM188R61C106MA73	Y
C6	C_27U_EMIFIL_CAP	Murata	NFM31PC276B0J3	Y
C7,C16,C18,C19,C22	C_220N_0402_X7R_K_16	Murata	GRM155R71C224KA12	Y
C10	C_1000P_0402_COG_K_50	Murata	GRM1555C1H102JA01	Y
C11,C14,C44,C45,C47, C48	C_100N_0402_X7R_K_16	Murata	GRM155R71C104KA88	Y
C12,C15,C21	C_10N_0402_COG_K_25	Murata	GRM155R71E103KA01	Y
C30,C39	C_10P_0402_COG_K_25	Murata	GRM1555C1H100JA01	Y
C31	C_470P_EMIFIL_CAP	Murata	NFM18CC471R1C3	Y
C32,C51	C_27U_EMIFIL_CAP	Murata	NFM31PC276B0J3	Y
C34,C35,C36,C37,C38, C40	C_100P_0402_COG_K_25	Murata	GRM1555C1E101JA01	Y
C49,C52	C_18P_0603_C0G_J_50	Murata	GRM1885C1H180JA01	Y
DL1	KP2012MGC	Kingbright	KP2012MGC	Y
DL2	KP2012MGC	Kingbright	KP2012MGC	Y
DL3	KP2012EC	Kingbright	KP2012EC	Y
JP1	Jumper_2	Samtec	HTSW-102-07-G-S	Y
J1	5 V	Emerson Network Power Connectivity Solutions	105-0752-001	Y
J2	GND	Emerson Network Power Connectivity Solutions	105-0753-001	Y
J3	CONN_10PIN_2.54mm_INT	TE Connectivity	2-176 1603-3	DEPOP
J4,J8	PSF-S01-007	Gigalane	PSF-S01-007	DEPOP
J5,J6,J7,J9	PSF-S01-007	Gigalane	PSF-S01-007	Y
MF1,MF2,MF3,MF4	3M HOLE	Keystone	25510	Y
M1	usb1232h-ds-v13	DLP design	USB1232H-ds-v13	Y

Table 2. STW81200-EVB BOM

Reference	Part	Manufacturer	Part Number	Populated
R_FL1	R_510R_0603_F	Yageo	RC0603FR-07510RL	DEPOP
R1	R_150_0603_F	Yageo	RC0603FR-07150RL	Y
R3	R_120_0603_F	Yageo	RC0603FR-07120RL	Y
R4	R_220R_0603_F	Yageo	RC0603FR-07220RL	Y
R5,R15,R17,R22,R24, R25,R26,R30,R31,R32, R33,R35,R39,R40,R41	R_0R0_0402	Panasonic	ERJ-2GE0R00X	Y
R6,R7,R14	R_0R5_0402_F	Yageo	RL0402FR-070R5L	Y
R8,R12	R_0R2_0402_F	Yageo	RL0402FR-070R2L	Y
R9,R10	R_470_0402_F	Yageo	RC0402FR-07470RL	Y
R11	R_1k_0603_F	Yageo	RC0603FR-071KL	Y
R16,R18	R_0R0_0402	Panasonic	ERJ-2GE0R00X	DEPOP
R23	R_100R_0402	Panasonic		DEPOP
R27	R_51R_0402	Panasonic		DEPOP
R28	R_3K6_0603_F	Yageo	RC0603FR-073K6L	DEPOP
R29	R_0R0_0603	Panasonic		DEPOP
R36	R_33k_0603_F	Yageo	RC0603FR-0733KL	Y
R37	R_120K_0603_F	Yageo	RC0603FR-07120KL	Y
R38	R_1K0_0603_F	Yageo	RC0603FR-071KL	Y
S1	SWITCH 1X2	EOZ	09.03201.02	Y
TP1	5V0	Keystone	5005	Y
TP2,TP10	GND	Keystone	5006	Y
TP3	LD_SDO	Keystone	5005	DEPOP
TP4	SDI	Keystone	5005	DEPOP
TP5	CLK	Keystone	5005	DEPOP
TP6	LE	Keystone	5005	DEPOP
TP7	PD_RF1	Keystone	5005	DEPOP
TP8	PD_RF2	Keystone	5005	DEPOP
TP9	PD	Keystone	5005	DEPOP
TP11	VCTRL	Keystone	5005	DEPOP
T1,T2	Ana_B0430J50100A00	Anaren	B0430J50100A00	Y
U1	STW81200			Y
U4	ZComm_CLVxxxxx	ZComm	N.A.	DEPOP
U5	3pin Jumper	Samtec	PHT-103-01-L-S	Y

Table 2. STW81200-EVB BOM

Reference	Part	Manufacturer	Part Number	Populated
U7	IQD_CPFS-32	IQD	LFSPXO056090	Y
X1	NX2520SA 50 MHz S1-2070-1010-10(NDK)	NDK	NX2520SA	Y

Note: DEPOP stands for not populated

8 Reference documents

Table 3. Reference documents

Reference	Revision	Title
[1]	Latest version	STW81200 Wideband RF fractional/integer frequency synthesizer with integrated VCOs Preliminary Data sheet, Document ID025943

9 Revision history

Table 4. Document revision history

Date	Revision	Changes
10-Jun-2015	1	Initial release.
09-Jul-2015	2	Added RPN ‘STSW-RFSOL002’ to cover page and headers. Removed redundant content from *Table 2: STW81200-EVB BOM*.