# 50 and 25 MHz Digital I/O Boards for PCI Express

# NI PCIe-6537, NI PCIe-6536 NEW!

- 50 MHz maximum clock rate
- Data streaming up to 200 MB/s (NI PCle-6537) or 100 MB/s (NI PCle-6536)<sup>1</sup>
- Selectable voltage levels of 2.5 and 3.3 V (5.0 V compatible)
- 32 channels with per-channel directional control
- x1 PCI Express interface with dedicated throughput to and from host processor
- Synchronous and asynchronous (handshaking) timing modes
- Software compatible with NI 6533 and NI 6534 NI-DAQmx applications

<sup>1</sup>Data rates vary depending on PC chipset, RAM or hard disk data streaming, and data direction.

#### **Operating Systems**

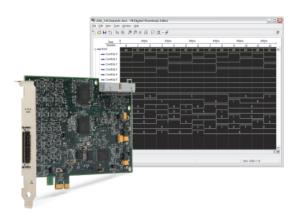
Windows 2000/XP

#### **Recommended Software**

- LabVIEW
- LabWindows/CVI
- SignalExpress
- Digital Waveform Editor

#### **Driver Software (included)**

- NI-DAQmx
- LabVIEW Express VIs



Product	Platform	Channels	Maximum Clock Rate (MHz)	Voltage Levels (V)	Maximum Throughput (MB/s)
NI 6537	PCI Express	32	50	2.5, 3.3, and 5.0 TTL	200
NI 6536	PCI Express	32	25	2.5, 3.3, and 5.0 TTL	100

Table 1. NI PCle-653x Specifications Overview

## **Overview**

Applications		
Semiconductor		
Interfacing to digital electronics		
Asynchronous digital transfers		
Consumer Electronics		
Digital display tests		
CCD imaging sensors		
Communications		
Digital I/O streaming		
Handshaking I/O		

The National Instruments PCIe-6537 and PCIe-6536 boards are 32-bit, digital I/O interfaces built on PCI Express — the next-generation PC I/O bus. These boards have maximum clock rates of 50 and 25 MHz, respectively. The 32 channels are fully software-configurable, providing the flexibility to communicate with a variety

of digital systems. You can set the direction of the 32 channels on a per-channel basis. These boards offer selectable voltage levels compatible with 2.5, 3.3, and 5.0 V TTL logic, with both synchronous and asynchronous timing modes for applications such as pattern I/O, handshaking, and change detection.

# Benefits of PCI Express for Digital I/O

PCI Express is the next-generation PC bus technology, delivering high, sustainable throughput to each module connected to the bus in a PC. With the increased bandwidth in the system bus, you can generate and acquire digital waveforms much larger than were previously possible with PCI-based digital I/O devices.

The ability to transfer large amounts of data at high rates over the system bus removes the need for expensive memory on board, lowering the cost of the digital device. Through PCI Express, the NI PCIe-6537 and PCIe-6536 boards can continuously stream digital data from PC memory at 200 MB/s and 100 MB/s respectively. High-throughput bus technology opens the

door for PC-based digital devices to service new areas such as testing image sensors and display panels while maintaining the ability to emulate communications protocols and interface to memory devices.

# NI 6533 and NI 6534 Compatibility

- Software compatible with existing NI 6533 and NI 6534 NI-DAQmx applications
- Interface to existing NI 6533 and NI 6534 fixtures and terminal blocks with the NI 653x cable adapter
- Compatible with most NI 6533 and NI 6534 timing modes pattern I/O, handshaking, change detection, and burst

# Timing Modes

- Pattern I/O or sample clock (synchronous) transfer patterns using an internal or external clock signal
- Burst handshaking (synchronous) NI 653x device and the peripheral device handshake before and during the synchronous transfer to maximize the transfer rate
- Handshaking I/O (asynchronous) transfer patterns when both the NI 653x device and the peripheral device are ready
- On-demand (unstrobed or static I/O) acquire or generate data through software-timed commands
- Change detection acquire data whenever a change occurs on one or more digital lines

For more information, visit ni.com/hsdio.



# **Specifications**

These specifications are valid for 0 to 45 °C, unless otherwise noted.

# **Channel Characteristics**

# **Generation Signal Characteristics (data, PFI channels)**

#### **Generation Voltage Levels**

	Low Voltage Levels (V)		High Voltage Levels (V)		
Family Settings (V)	Typical	Max	Min	Typical	
2.5	0	0.1	2.4	2.5	
3.3	0	0.1	3.2	3.3	
5.0	0	0.1	3.2	3.3	

#### **Acquisition Signal Characteristics (data, PFI channels)**

Acquisition voltage families (V)........... 2.5, 3.3 logic families (5.0 V compatible)

## **Acquisition Voltage Levels**

Family	Low Voltage Thresholds (V)	High Voltage Thresholds (V)	
Settings (V)	Max	Min	
2.5	0.75	1.75	
3.3	1.0	2.3	
5.0	1.0	2.3	

# Timing Characteristics Sample Clock

Sample Glock		
Sources	Onboard clock (internal OSC with divider) PFI<4:5> RTSI<7>	
Onboard clock frequency range		
NI 6536	48 Hz to 25 MHz, settable to 200 MHz/N; $8 \le N \le 4,194,304$ 48 Hz to 50 MHz, settable to 200 MHz/N; $4 \le N \le 4,194,304$	
Imported sample clock frequency range		
NI 6536	0 Hz to 25 MHz	
NI 6537	0 Hz to 50 MHz	
Exported sample clock destinations	PFI<4:5>	

RTSI<7>

## **Generation Signal Characteristics (data, PFI channels)**

Maximum data channel toggle rate NI 6536 NI 6537 Data position modes	12.5 MHz 25 MHz Active edge, inactive edge (data channels only)	
Handshaking		
Asynchronous handshaking modes Synchronous handshaking modes	Handshaking sample timing Burst sample timing Pipelined sample clock timing	

Active low

#### **Change Detection**

Change detection resolution	Sample clock period
Sources for change detection	Data channels 0 to 31
Valid sample position	Active edge, inactive edge
Valid changes	Rising, falling, both

# **Waveform Characteristics**

Control line polarity ...... Active high

Transfer types	DMA	
	Programmed I/O (static only)	

## **Trigger Inputs**

Trigger types	Start trigger (pipelined or sample clock timing) Pause trigger (pipelined or burst timing) Reference trigger (pipelined or sample clock timing) Handshake trigger (handshaking timing)
Sources	PFI <0:5> (DDC connector) RTSI <0:7> (RTSI bus) Pattern match (acquisition only) Disabled (do not wait for a trigger)
Trigger detection	Start trigger (edge detection: rising or falling; pattern match: match or don't match) Pause trigger (level detection: high or low; pattern match: match or don't match) Reference trigger (edge detection: rising or falling; pattern match: match or don't match) Handshaking trigger (interlocked: high or low)
Destinations	PFI <0:5> (DDC connector) RTSI <0:7> (RTSI bus)

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#### **Events (outputs from NI PCIe-653x)**

## **Miscellaneous**

# **Physical**

#### **Power Requirements**

Typical ...... 5.1 W Maximum ..... 6.1 W

#### Software

Driver and application software ....... NI-DAQmx

#### **Environment**

(meets IEC-60068-2-56)

#### Compliance

#### Safety

The NI PCIe-653x boards meet the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 3111-1, UL 61010-1
- CSA 61010-1

**Note:** For full EMC compliance, you must operate this device with shielded cabling. In addition, all covers and filler panels must be installed. Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information.

For access to certifications, marks, and DoCs, visit ni.com/certification.

# Ordering Information

NI PCIe-6537	779673-01
NI PCIe-6536	779672-01
Includes NI-DAQmx software.	
Software	
NI Digital Waveform Editor	778724-03
Cables	
SHC68-C68-D2 (shielded 1 m cable)	188142-01
C68-C68-D4 (unshielded 1 m cable)	195949-01
SHC68-H1X38 (flying-lead cable)	192681-1R5
Accessories	
CB-2162	778592-01
SMB-2163	778747-01

# **BUY NOW!**

For complete product specifications, pricing, and accessory information, call 800 813 3693 (U.S. only) or go to ni.com/hsdio.

NI 653x cable adapter ......195846-01

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