TS200L Series

NANOPOWER MICRO DC-DC BUCK CONVERTER WITH BUILT-IN INDUCTOR

TS200L-DS-R005

1. GENERAL DESCRIPTION

The TS200L series is a nano-power step-down micro DC-DC converter built with integrated inductor in one tiny package (2.0 mm x 2.5 mm, h=1.0 mm). The micro DC-DC converter features very low ripple and EMI noise emission due to its close to zero interconnection length between the controller IC and inductor.

The PFM operation consumes 100 nA or less in stand-by mode and 500 nA quiescent current (typ @ Vout = 1.8V) during operation while delivers high conversion efficiency throughout the full range of load. The combination of these features enables up to 95% power conversion efficiency from a battery and significantly boosts battery life in product light-load operating hours.

The series is compatible with low ESR ceramic capacitors.

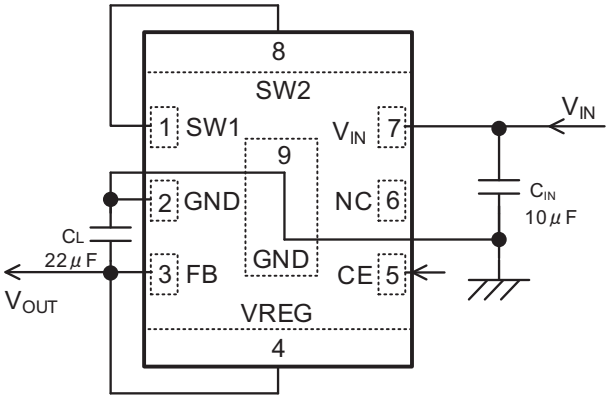
APPLICATIONS

- Wearable Devices
- Energy Harvest Devices
- Digital Cameras
- Internet-of-Thing (IoT)
- Wireless Connectivities Devices
- Digital Audio Equipment
- Reference Voltage Sources
- Multi-function Power Supplies

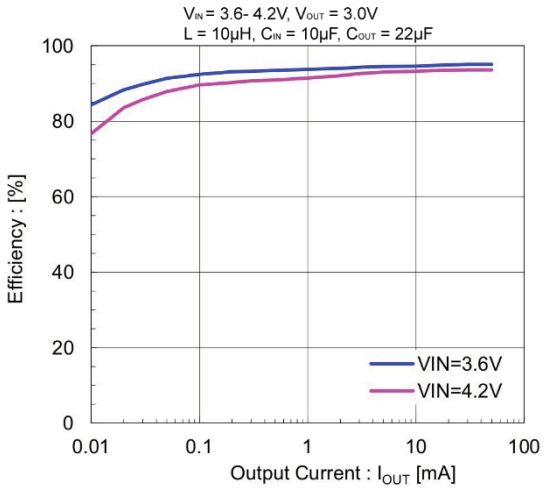
FEATURES

- Output Voltage : 1.0 ~ 4.0 V (0.05V increments)
- Input Voltage : 2.0 ~ 6.0 V
- Quiescent Current : 500nA typ.
- High Efficiency : 93% (V_{IN}=3.6V,V_{OUT}=3.0V/100µA)
- Output Current : 200mA / 50mA
- Total Solution Size : < 7 mm^2
- Optional Discharge Function on V_{OUT}
- Low Output Ripple Voltage
- Protection Circuits : current limit and short circuit
- Operating Temperature : -40°C to +85°C
- Environmental Friendly : EU RoHS Compliant, Pb-free, Halogen-free

TYPICAL APPLICATION CIRCUIT



TYPICAL PERFORMANCE CHARACTERISTICS



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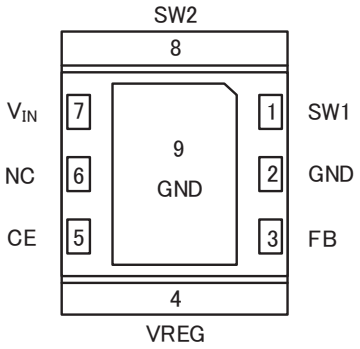
2. PIN CONFIGURATION



(BOTTOM VIEW)

Table 1

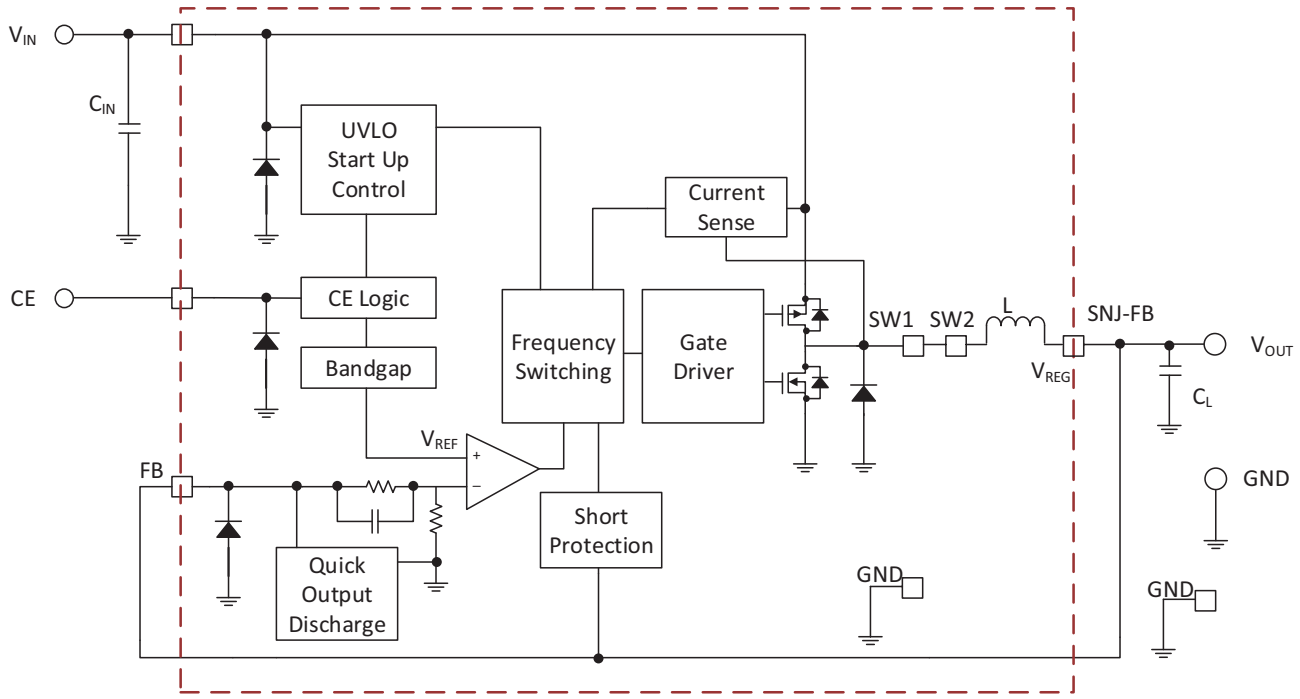
Pin No.	Symbol	Description
1	SW1	Switching Node 1
2	GND	Ground
3	FB	Feedback
4	VREG	Regulated Output Voltage
5	CE	Chip Enable
6	NC	No Connection
7	VIN	Input Voltage
8	SW2	Switching Node 2
9	GND	Ground

3. ORDERING PART NUMBERS

Table 2

TS200L PN TS200L -①②③④⑤⑥⑦	FEATURE	SYMBOL	DESCRIPTION
①	Quick Output Discharge	E / D	E = Enabled, D = Disabled
②	Output Current (I_{OUT})	5 / 2	5 = 50 mA, 2 = 200 mA
③④⑤	Output Voltage (V_{OUT})	0 - 9	Range: 1.00V ~ 4.00V (0.05V step) e.g. Vout = 1.80V → ③④⑤ = 180
⑥⑦	Fixed Part Number	EL	EL = IIP-2025 (w/ integrated inductor) (3,000 pcs/Reel)
e.g. TS200L-E5180EL = Quick Output Discharge/50mA/1.8V/integrated inductor/IIP-2025 2.0 x 2.5 x 1.0 mm e.g. TS200L-D2180EL = No Quick Output Discharge/200mA/1.8V/integrated inductor/IIP-2025 2.0 x 2.5 x 1.0 mm			

4. BLOCK DIAGRAM



5. ABSOLUTE MAXIMUM RATINGS

Table 3

Parameter	Rating
V_{IN} to GND	-0.3 V to +7 V
SW1 to GND	-0.3V to V_{IN}+0.3 V or +7V *
SW2 to GND	-0.3V to V_{IN}+0.3 V or +7V *
FB to GND	-0.3V to V_{IN}+0.3 V or +7V *
CE to GND	-0.3 V to +7 V
V_{REG} to GND	-0.3V to V_{IN}+0.3 V or +7V *
Storage Temperature Range	-55°C to +125°C
Operational Ambient Temperature	-40°C to +85°C

* The maximum value is the lower of either V_{IN} + 0.3V or +7V

6. ELECTRICAL CHARACTERISTICS

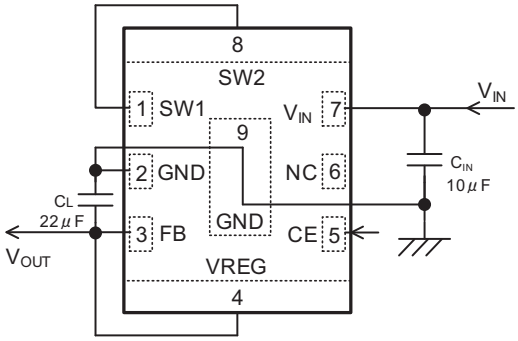
Table 4

TS200L-_ _ _ _ _ EL Ta = 25°C

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Input Supply Voltage Range	V_{IN}	2.0		6.0	V	
Output Voltage Range	V_{OUT}	1.00		4.00	V	Factory Programmable (0.05V step)
Output Current V_{OUT} Range: 1.00V ~ 4.00V	I_{OUT}			50 200	mA	Selectable 50 mA Max / 200 mA Max
Output Voltage Tolerance	V_{OUT_Tol}	-2%		+2%	%	
Standby Current	I_{STBY}		0.1	1	µA	V_{IN} = 5V, V_{CE} = V_{OUT} = 0V
Quiescent Current	I_q		500	900	nA	$V_{OUT(typ)}$ = 1.0 V ~ 1.95 V, V_{IN} = V_{CE} = $V_{OUT(typ)}$ + 0.5 V
Input Supply Bypass	V_{INBY}		V_{IN} = V_{OUT}		V	Bypass until UVLO is reached
Undervoltage Lockout (UVLO)	V_{UVLO}	1.65	1.8	1.95	V	
UVLO Hysteresis	V_{UVLO_H}	0.1	0.15	0.2	V	
Switching Frequency	F_{SW}	40	200	600	kHz	Pulsed I_{OUT} 30 mA / 50 µA
CE Pin Input Voltage Threshold High Low Input Leakage Current	 V_{CEH} V_{CEL} I_{CE_Leak}	 1.2 GND		 6.0 0.3 100	 V V nA	
Current Limit 50 mA Type 200 mA Type	 I_{LIMIT} I_{LIMIT}	 115 260	 180 330	 250 400	 mA mA	 V_{IN} = V_{CE} = V_{OUT} + 2V, I_{OUT} = 10 mA V_{IN} = V_{CE} = V_{OUT} + 2V, I_{OUT} = 10 mA
Efficiency 50 mA Type 50 mA Type 50 mA Type 50 mA Type 200 mA Type 200 mA Type 200 mA Type	 E_{ff} 	 	 95 95 89 85 93 93 87	 	 % % % % % % %	 V_{IN}=V_{CE}=5V, V_{OUT}=4V, I_{OUT}=30 mA V_{IN}=V_{CE}=3.6V, V_{OUT}=3.3V, I_{OUT}=30 mA V_{IN}=V_{CE}=3.6V, V_{OUT}=1.8V, I_{OUT}=30 mA V_{IN}=V_{CE}=3.6V, V_{OUT}=0.7V, I_{OUT}=30 mA V_{IN}=V_{CE}=5V, V_{OUT}=4V, I_{OUT}=30 mA V_{IN}=V_{CE}=3.6V, V_{OUT}=3.3V, I_{OUT}=30 mA V_{IN}=V_{CE}=3.6V, V_{OUT}=1.8V, I_{OUT}=30 mA
SW Pin ON Resistance High-side Power FET Low-side Power FET	 R_{DS_H} R_{DS_L}	 	 0.4 0.4	 0.65 	 Ω Ω	
Quick Output Discharge Resistance	R_{DIS}	55	100	130	Ω	Varies with V_{IN}
Short Protection Threshold V_{OUT} Range: 1.00V ~ 4.00V	V_{SHORT}	0.4	0.5	0.6	V	V_{OUT} → 0V

ESD CAUTION	
	ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

7. TYPICAL APPLICATION CIRCUIT



Selecting the Input and Output Capacitor

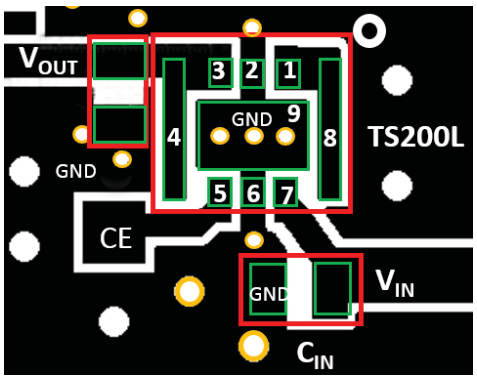
A low ESR X7R or X5R ceramic capacitor is required to minimize the input and output voltage ripple. Although a 10µF and 22µF respectively for input and output capacitor are generally sufficient for nearly all combinations of input current and output voltage, it is important to account for the loss of capacitance due to DC bias characteristics of the input capacitor. Early sanity testing helps to evaluate how much output voltage ripple suppression is sufficient. When small case sizes are used, 16V or higher rated voltage is recommended with a 10µF input capacitor or 10V rated voltage with a 22µF output capacitor. Do not use Y5V or Z5U capacitors due to their large variation in capacitance over temperature and DC bias.

The following table shows the recommended input and output capacitors.

Vendor	Model	Rated Voltage [V]	Capacitance (µF)	Case Size	Dimensions (mm)
Taiyo Yuden	LDK105EBJ226MV-F	10	22	0402	1.0 x 0.5 x 0.5
Taiyo Yuden	EMK107BBJ106MA-T	16	10	0603	1.6 x 0.8 x 0.8
Taiyo Yuden	LMK107BBJ226MA-T	10	22	0603	1.6 x 0.8 x 0.8
TDK	C1608X5R1C106M	16	10	0603	1.6 x 0.8 x 0.8
TDK	C1608X5R1A226M	10	22	0603	1.6 x 0.8 x 0.8
Taiyo Yuden	LMK212BBJ476MG-T	10	47	0805	2.0 x 1.25 x 1.25
TDK	C2012X5R1A476M	10	47	0805	2.0 x 1.25 x 1.25

Evaluation Board Layout

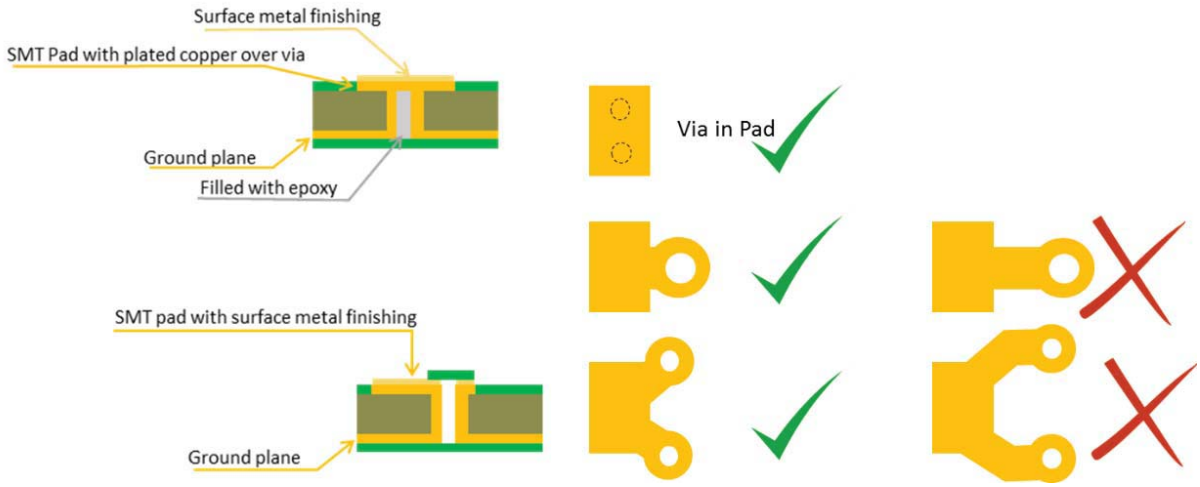
The 2-layer evaluation board (bottom layer is a ground plane) as illustrated below provides a general idea of how power rail, signal paths, ground plane and vias may be arranged. In compact designs such as wearable electronics, components are placed as close as possible by following the layout consideration given in the next section, wherein each of the ground terminals should be immediately connected to a ground plane underneath by ground vias in close proximity (or via-in-pad) - highlighted in orange color as follows:



8. LAYOUT CONSIDERATION

1. PCB layout is of utmost importance to avoid potential performance, stability and EMI problems. Key notes on ground vias are listed as follows:

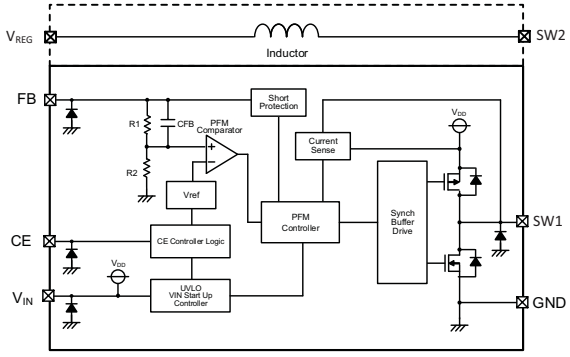
Placement of Ground Vias



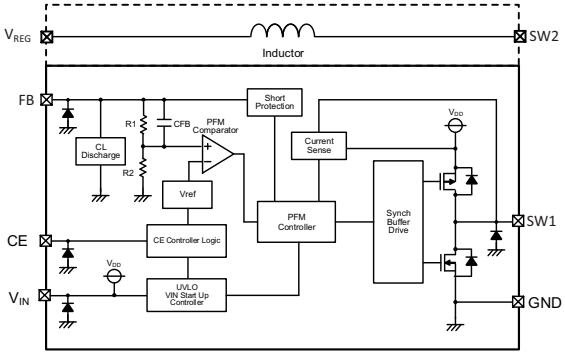
2. Place the TS200L, input and output capacitors in close proximity with traces as wide and as short as possible.
3. Connect ground terminal of the TS200L to a ground plane that should be as close as possible. Ground vias should be placed next to or on the ground terminals as shown in the pictures above. Do not use long trace and thermal reliefs on the ground vias. The ground plane should be directly connected to the ground terminal of a battery or power source using as wide and as short a connection as possible.
4. Ground planes between different layers should be interconnected with as many ground vias in close proximity as possible. Do not use a single via or vias with large separation to connect different layers of ground planes.
5. Keep the output voltage trace away from the input voltage trace.
6. Do not route traces under the TS200L.
7. In the event that layout requirements require more than a single layer to route the TS200L, input and output capacitors or these components must be placed on opposite sides of the board, traces running on adjacent layers coaxial to each other or overlapping should be separated by a ground plane to prevent cross-coupling and provide stable ground reference.

9. OPERATIONAL EXPLANATION

The TS200L series consists of a reference voltage supply, PFM comparator, Pch driver Tr, Nch synchronous rectification switch Tr, current sensing circuit, PFM control circuit, CE control circuit, and others. (Refer to the block diagram below.)



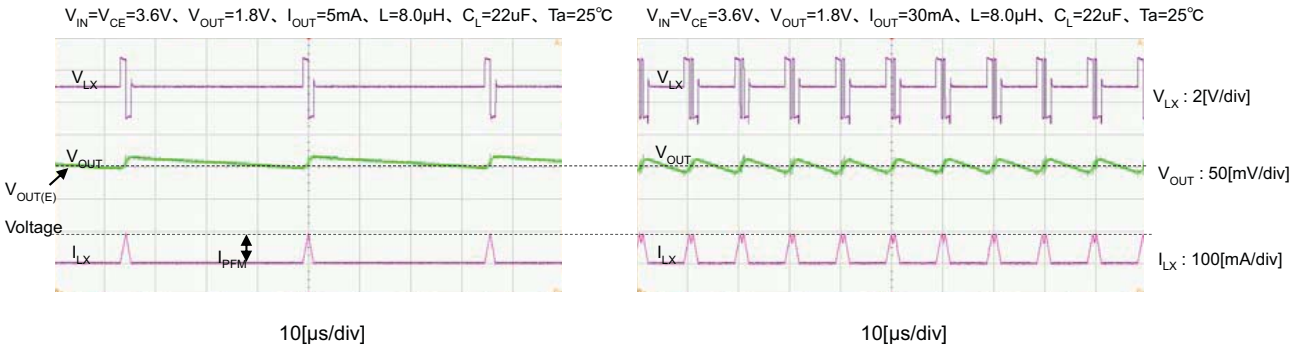
Without Quick Output Discharge



With Quick Output Discharge

An ultra-low quiescent current circuit and synchronous rectification enable a significant reduction of dissipation in the IC, and the IC operates with high efficiency at both light loads and heavy loads. Current limit PFM is used for the control method, and even when switching current superposition occurs, increases of output voltage ripple are suppressed, allowing use over a wide voltage and current range. The IC is compatible with low- capacitance ceramic capacitors, and a small, high-performance step-down DC-DC converter can be created.

The actual output voltage $V_{OUT(E)}$ in the electrical characteristics is the threshold voltage of the PFM comparator in the block diagram. Therefore the average output voltage of the step-down circuit, including peripheral components, depends on the ripple voltage. Before use, test fully using the actual device.



<Reference voltage supply (V_{REF})>

Reference voltage for stabilization of the output voltage of the IC.

<PFM control>

(1) The feedback voltage (FB voltage) is the voltage that results from dividing the output voltage with the IC internal dividing resistors R_{FB1} and R_{FB2}. The PFM comparator compares this FB voltage to V_{REF}. When the FB voltage is lower than V_{REF}, the PFM comparator sends a signal to the buffer driver through the PFM control circuit to turn on the Pch driver Tr. When the FB voltage is higher than V_{REF}, the PFM comparator sends a signal to prevent the Pch driver Tr from turning on.

(2) When the Pch driver Tr is on, the current sense circuit monitors the current that flows through the Pch driver Tr connected to the Lx pin. When the current reaches the set PFM switching current (I_{PFM}), the current sense circuit sends a signal to the buffer driver through the PFM control circuit. This signal turns off the Pch driver Tr and turns on the Nch synchronous rectification switch Tr.

(3) The on time (off time) of the Nch synchronous rectification switch Tr is dynamically optimized inside the IC. After the off time elapses and the PFM comparator detects that the V_{OUT} voltage is higher than the set voltage, the PFM comparator sends a signal to the PFM control circuit that prevents the Pch driver Tr from turning on. However, if the V_{OUT} voltage is lower than the set voltage, the PFM comparator starts Pch driver Tr on.

9. OPERATIONAL EXPLANATION (Continued)

By continuously adjusting the interval of the linked operation of (1), (2) and (3) above in response to the load current, the output voltage is stabilized with high efficiency from light loads to heavy loads.

<PFM Switching Current >

The PFM switching current monitors the current that flows through the Pch driver Tr, and is a value that limits the Pch driver Tr current.

The Pch driver Tr remains on until the coil current reaches the PFM switching current (I_{PFM}). An approximate value for this on-time t_{ON} can be calculated using the following equation:

$$t_{ON} = L \times I_{PFM} / (V_{IN} - V_{OUT})$$

<Maximum on-time function>

To avoid excessive ripple voltage in the event that the coil current does not reach the PFM switching current within a certain interval even though the Pch driver Tr has turned on and the FB voltage is above V_{REF}, the Pch driver Tr can be turned off at any timing using the maximum on-time function of the PFM control circuit. If the Pch driver Tr turns off by the maximum on-time function instead of the current sense circuit, the Nch synchronous rectification switch Tr will not turn on and the coil current will flow to the V_{OUT} pin by means of the parasite diode of the Nch synchronous rectification switch Tr.

<Through mode>

When the V_{IN} voltage is lower than the output voltage, through mode automatically activates and the Pch driver Tr stays on continuously.

(1) In through mode, when the load current is increased and the current that flows through the Pch driver Tr reaches a load current that is several tens of mA lower than the set PFM switching current (I_{PFM}), the current sense circuit sends a signal through the PFM control circuit to the buffer driver. This signal turns off the Pch driver Tr and turns on the Nch synchronous rectification switch Tr.

(2) After the on-time (off-time) of the Nch synchronous rectification switch Tr, the Pch driver Tr turns on until the current reaches the set PFM switching current (I_{PFM}) again.

If the load current is large as described above, operations (1) and (2) above are repeated. If the load current is several tens of mA lower than the PFM switching current (I_{PFM}), the Pch driver Tr stays on continuously.

<V_{IN} start mode>

When the V_{IN} voltage rises, V_{IN} start mode stops the short-circuit protection function during the interval until the FB voltage approaches V_{REF}. After the V_{IN} voltage rises and the FB voltage approaches V_{REF} by step-down operation, V_{IN} start mode is released. In order to prevent an excessive rush current while V_{IN} start mode is activated, the coil current flows to the V_{OUT} pin by means of the parasitic diode of the Nch synchronous rectification Tr. In V_{IN} start mode as well, the coil current is limited by the PFM switching current.

<Short-circuit protection function>

The short-circuit protection function monitors the V_{OUT} voltage. In the event that the V_{OUT} pin is accidentally shorted to GND or an excessive load current causes the V_{OUT} voltage to drop below the set short-circuit protection voltage, the short-circuit protection function activates, and turns off and latches the Pch driver Tr at any selected timing. Once in the latched state, the IC is turned off and then restarted from the CE pin, or operation is started by re-applying the V_{IN} voltage.

<UVLO function>

When the V_{IN} pin voltage drops below the UVLO detection voltage, the IC stops switching operation at any selected timing, turns off the Pch driver Tr and Nch synchronous rectification switch Tr (UVLO mode). When the V_{IN} pin voltage recovers and rises above the UVLO release voltage, the IC restarts operation.

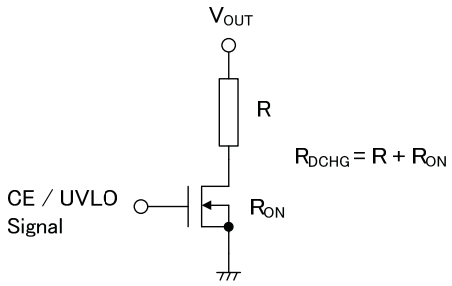
9. OPERATIONAL EXPLANATION (Continued)

<C_L discharge function>

On the TS200L series, a C_L discharge function is available as an option (TS200L-E/D) . This function enables quick discharging of the C_L load capacitance when "L" voltage is input into the CE pin by the Nch Tr connected between the V_{OUT}-GND pins, or in UVLO mode. This prevents malfunctioning of the application in the event that a charge remains on C_L when the IC is stopped. The discharge time is determined by C_L and the C_L discharge resistance R_{DCHG}, including the Nch Tr (refer to the diagram below). Using this time constant $\tau = C_L \times R_{DCHG}$, the discharge time of the output voltage is calculated by means of the equation below.

$V=V_{OUT} \times e^{-t/\tau}$, *or in terms of t,* $t = \tau In(V_{OUT}/V)$

V: Output voltage after discharge
V_{OUT} : Set output voltage
t: Discharge time
C_L: Value of load capacitance (C_L)
R_{DCHG} : Value of C_L discharge resistance Varies by power supply voltage.
τ: $C_L \times R_{DCHG}$



The C_L discharge function is not available on the TS200L-D.

10. APPLICATION NOTES

1. Be careful not to exceed the absolute maximum ratings for externally connected components and this IC.

2. The DC/DC converter characteristics greatly depend not only on the characteristics of this IC but also on those of externally connected components, so refer to the specifications of each component and be careful when selecting the components. Be especially careful of the characteristics of the capacitor used for the load capacity C_L and use a capacitor with B characteristics (JIS Standard) or an X7R/X5R (EIA Standard) ceramic capacitor.

3. Use a ground wire of sufficient strength. Ground potential fluctuation caused by the ground current during switching could cause the IC operation to become unstable, so reinforce the area around the GND pin of the IC in particular.

4. Mount the externally connected components in the vicinity of the IC. Also use short, thick wires to reduce the wire impedance.

5. When the voltage difference between V_{IN} and V_{OUT} is small, switching energy increases and there is a possibility that the ripple voltage will be too large. Before use, test fully using the actual device.

6. The CE pin does not have an internal pull-up or pull-down, etc. Apply the prescribed voltage to the CE pin.

7. If other than the recommended inductance and capacitance values are used, excessive ripple voltage or a drop in efficiency may result.

8. If other than the recommended inductance and capacitance values are used, a drop in output voltage when the load is excessive may cause the short-circuit protection function to activate. Before use, test fully using the actual device.

9. At high temperature, excessive ripple voltage may occur and cause a drop in output voltage and efficiency. Before using at high temperature, test fully using the actual device

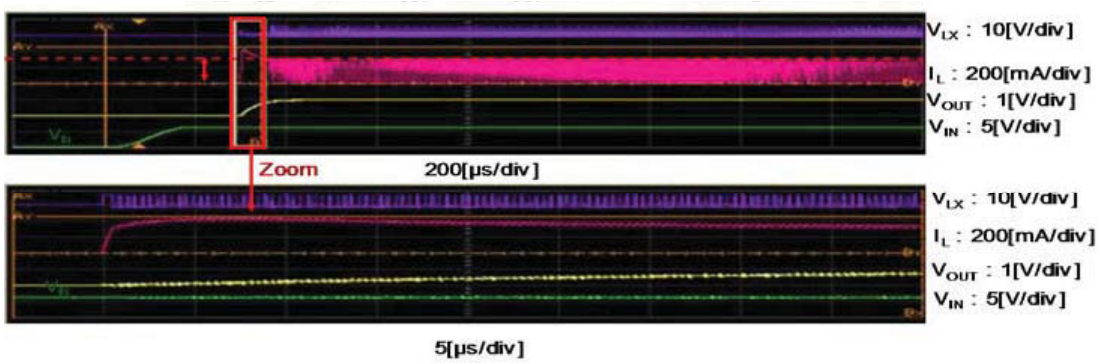
10. At light loads or when IC operation is stopped, leakage current from the Pch driver Tr may cause the output voltage to rise.

11. The average output voltage may vary due to the effects of output voltage ripple caused by the load current. Before use, test fully using the actual device.

12. If the C_L capacitance or load current is large, the output voltage rise time will lengthen when the IC is started, and coil current overlay may occur during the interval until the output voltage reaches the set voltage (refer to the diagram below).

10. APPLICATION NOTES (Continued)

TSL200L series $V_{IN}=V_{CE}=0\rightarrow6.0V$、$V_{OUT}=1.0V$、$I_{OUT}=200mA$、CL=22uF、Ta=25℃



13. When the IC is started, the short-circuit protection function does not operate during the interval until the VOUT voltage reaches a value near the set voltage.

14. If the IC is started at a VIN voltage that activates through mode, it is possible that the short-circuit protection function will not operate. Before use, test fully using the actual device.

If the load current is excessively large when the IC is started, it is possible that the VOUT voltage will not rise to the set voltage. Before use, test fully using the actual device.

16. In actual operation, the maximum on-time depends on the peripheral components, input voltage, and load current. Before use, test fully usingthe actual device.

17. When the VIN voltage is tudrned on and off continuously, excessive rush current may occur while the voltage is on. Before use, test fully using the actual device.

18. When the VIN voltage is high, the Pch driver may change from on to off before the coil current reaches the PFM switching current (IPFM), or before the maximum on-time elapses. Before use, test fully using the actual device.

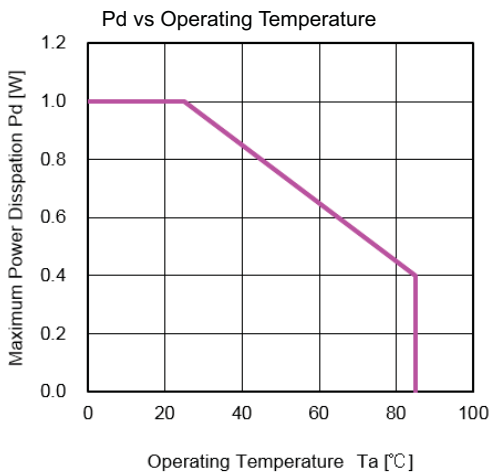
19. When the IC change to the Through Mode at light load, the supply current of this IC can increase in some cases.

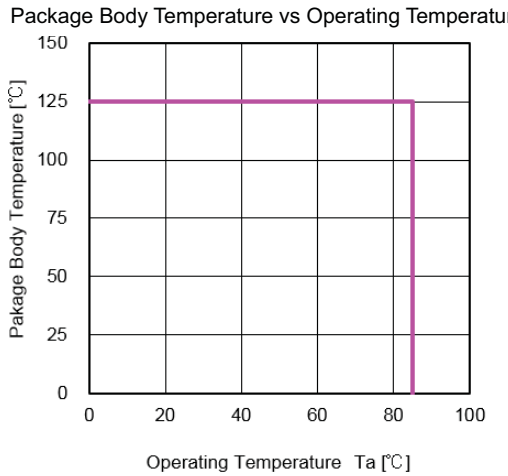
20. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.

21. TransSiP emphasizes on relentless improvement on our products and reliability.
We request users shall incorporate fail-safe designs and post-aging protection practice when using TransSiP products in their systems.

22. The UVLO function can be activated when the UVLO hysteresis width gets to about 0mV and after several tens ms elapses at light loads. Before use, test fully using the actual device.

23. Please use within the power dissipation range below. Please also note that the power dissipation may changed by test conditions, the power dissipation figure shown is PCB mounted.

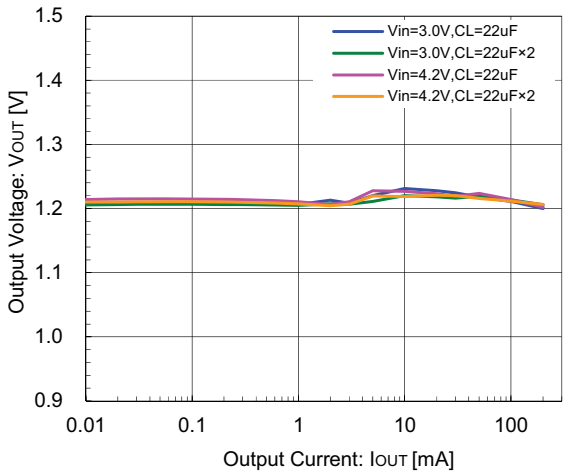




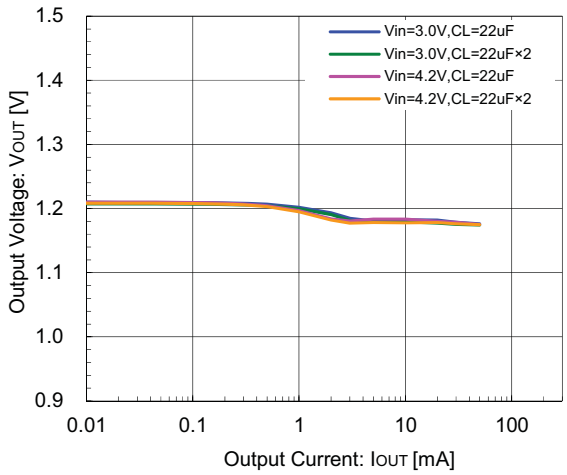
11. TYPICAL PERFORMANCE CHARACTERISTICS

1. Output Voltage vs. Output Current

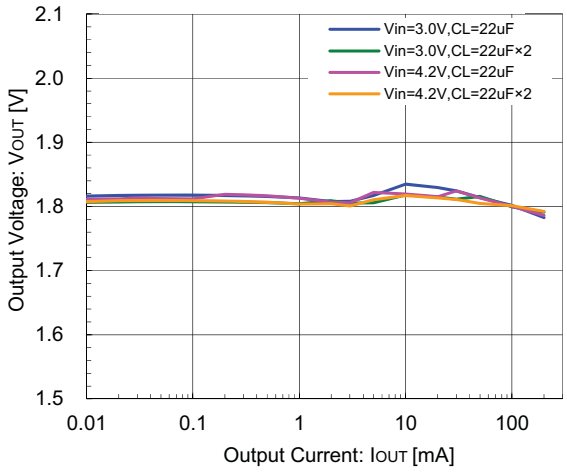
TS200L-D2120EL / TS200L-E2120EL



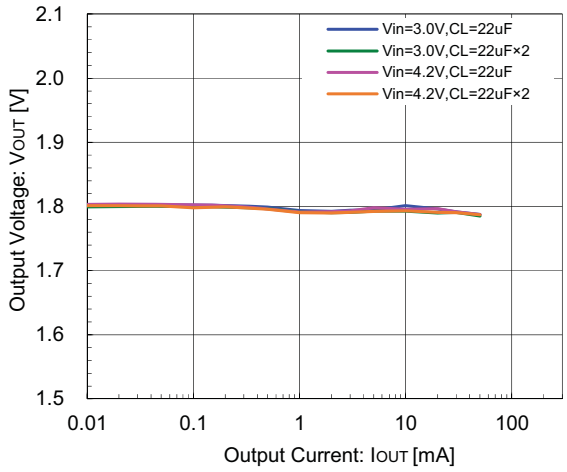
TS200L-D5120EL / TS200L-E5120EL



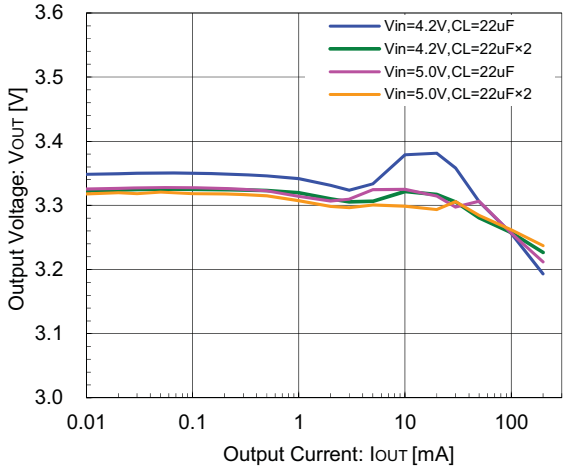
TS200L-D2180EL / TS200L-E2180EL



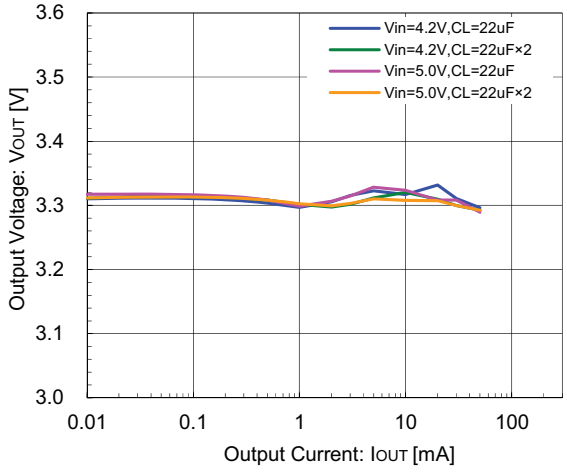
TS200L-D5180EL / TS200L-E5180EL



TS200L-D2330EL / TS200L-E2330EL



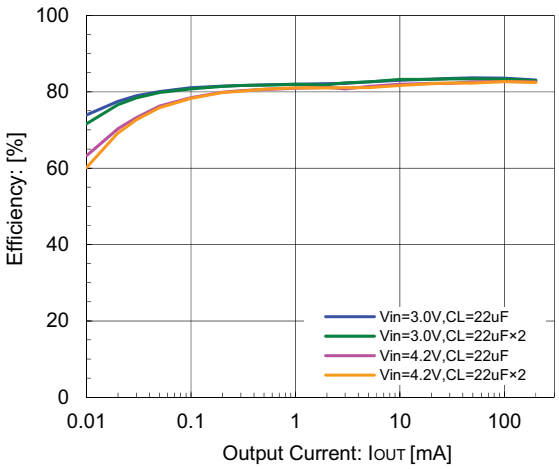
TS200L-D5330EL / TS200L-E5330EL



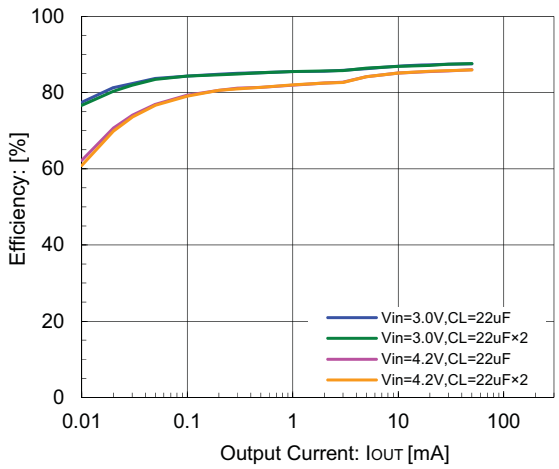
11. TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

2. Efficiency vs. Output Current

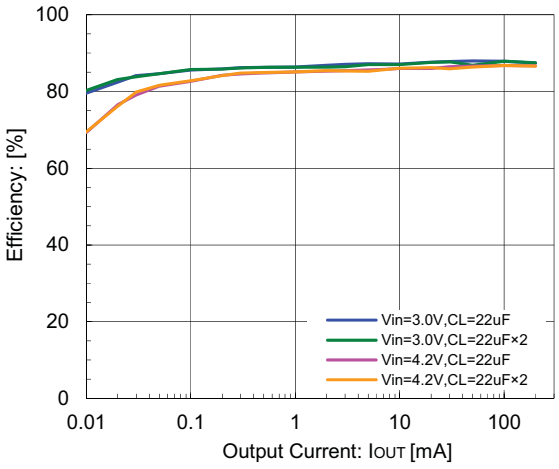
TS200L-D2120EL / TS200L-E2120EL



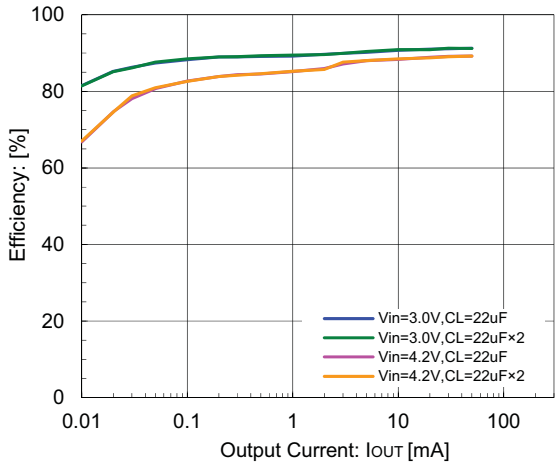
TS200L-D5120EL / TS200L-E5120EL



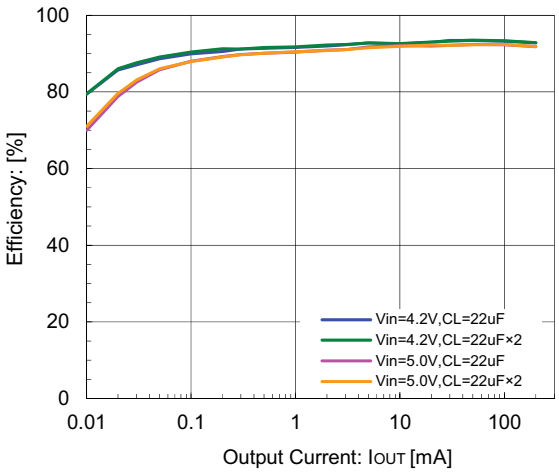
TS200L-D2180EL / TS200L-E2180EL



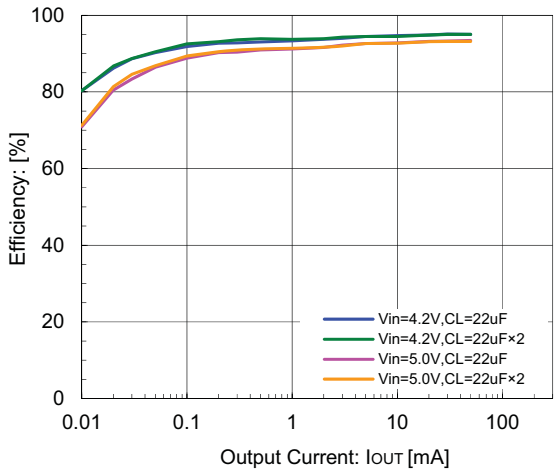
TS200L-D5180EL / TS200L-E5180EL



TS200L-D2330EL / TS200L-E2330EL



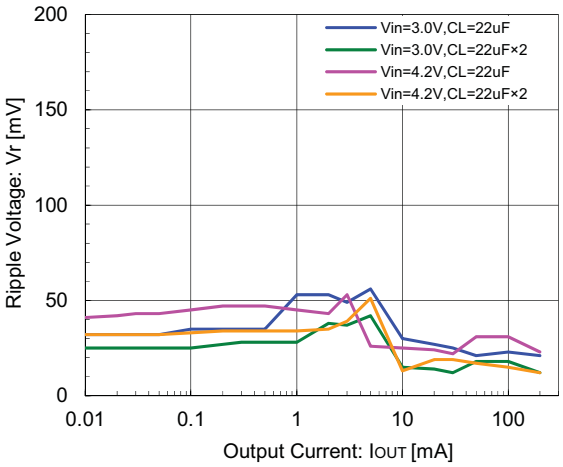
TS200L-D5330EL / TS200L-E5330EL



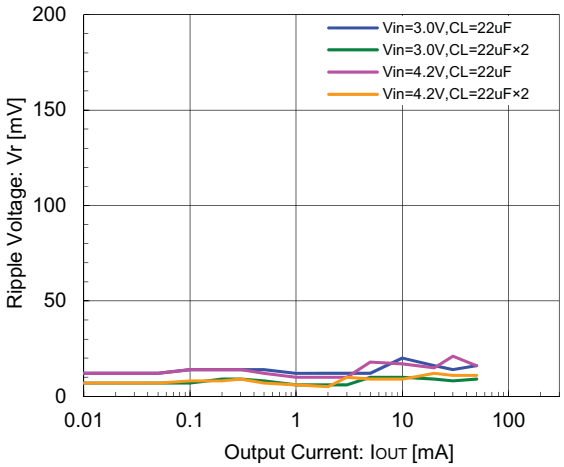
11. TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

3. Ripple Voltage vs. Output Current

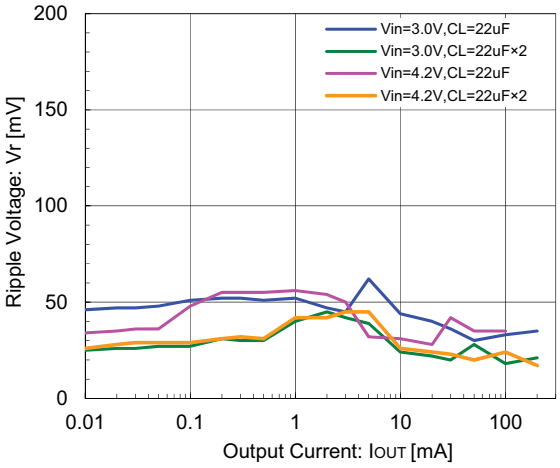
TS200L-D2120EL / TS200L-E2120EL



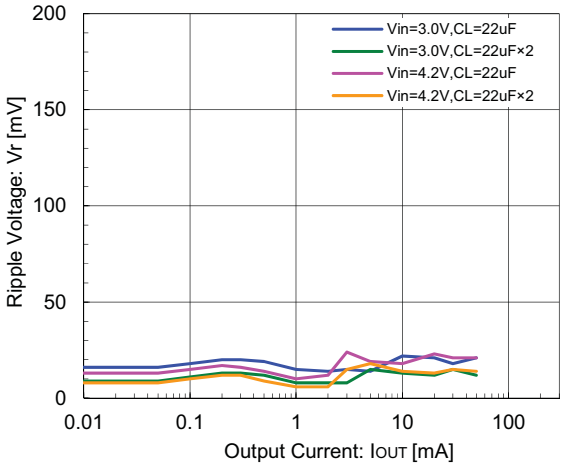
TS200L-D5120EL / TS200L-E5120EL



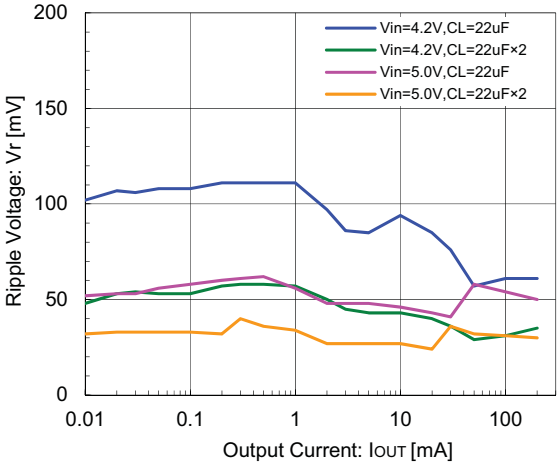
TS200L-D2180EL / TS200L-E2180EL



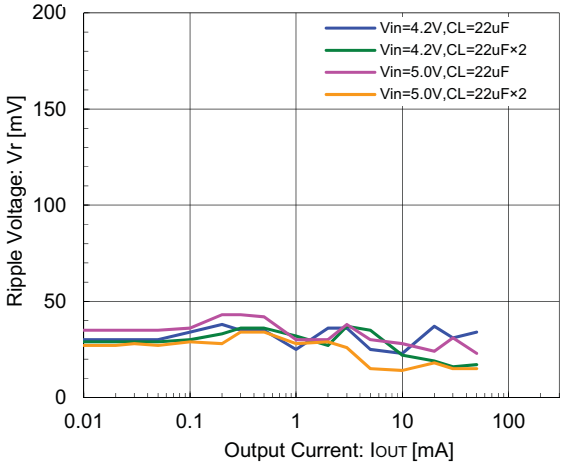
TS200L-D5180EL / TS200L-E5180EL



TS200L-D2330EL / TS200L-E2330EL



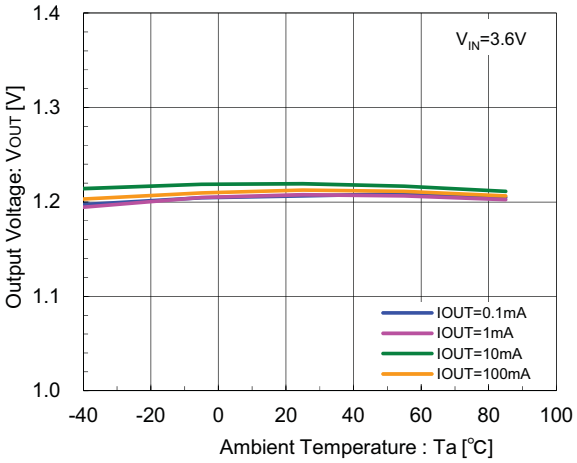
TS200L-D5330EL / TS200L-E5330EL



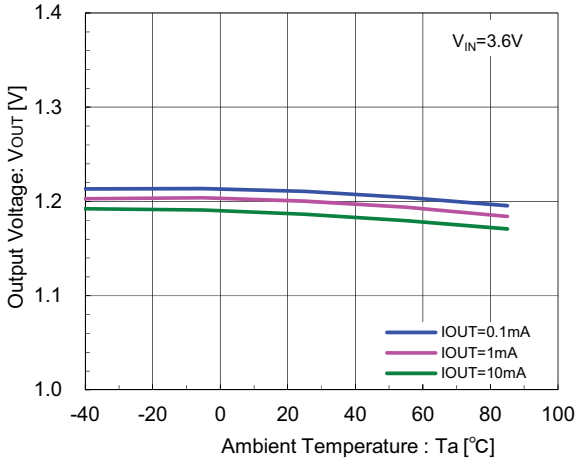
11. TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

4. Ambient Temperature vs. Output Voltage

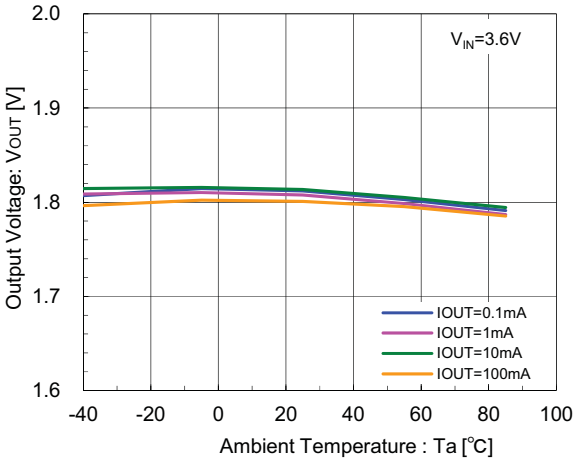
TS200L-D2120EL / TS200L-E2120EL



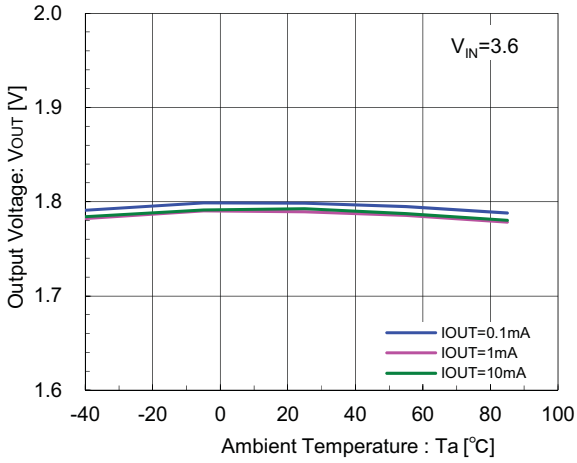
TS200L-D5120EL / TS200L-E5120EL



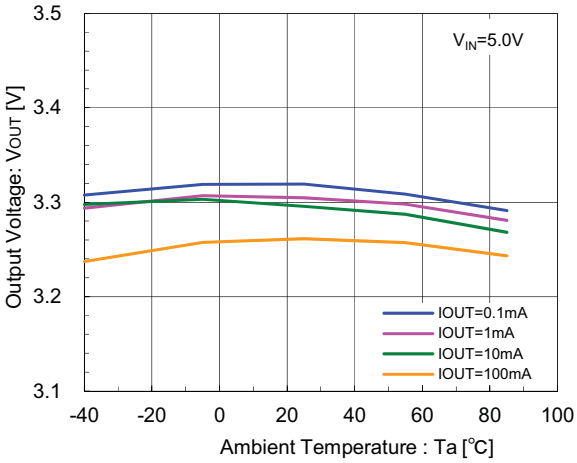
TS200L-D2180EL / TS200L-E2180EL



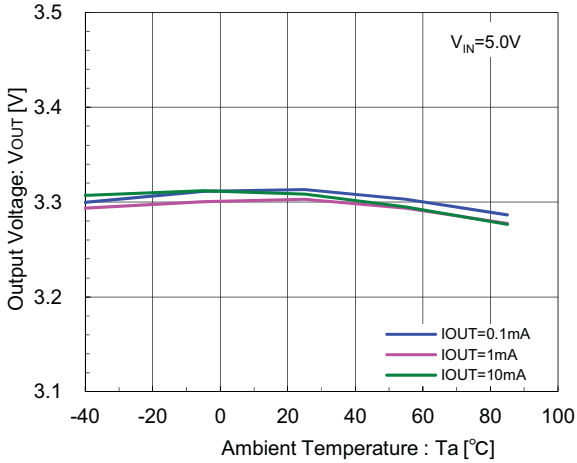
TS200L-D5180EL / TS200L-E5180EL



TS200L-D2330EL / TS200L-E2330EL



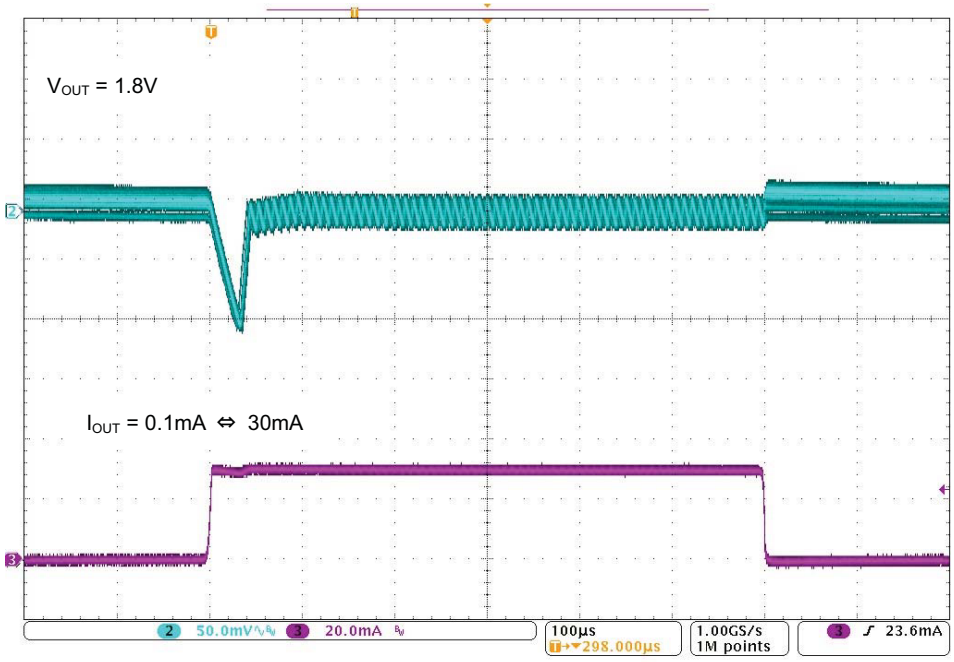
TS200L-D5330EL / TS200L-E5330EL



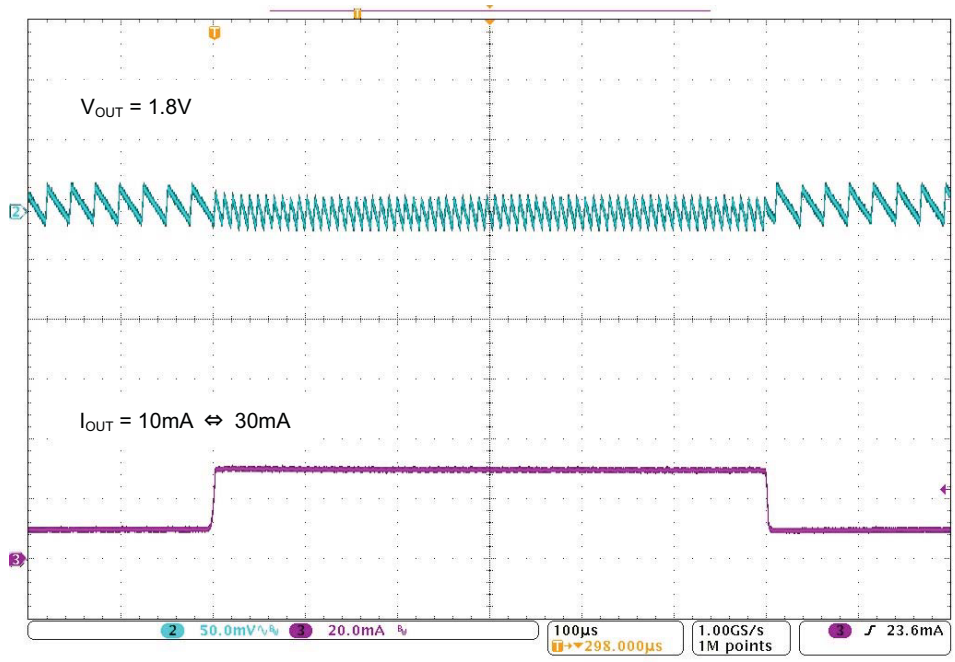
11. TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

5. Load Transient Response

1. TS200L-D5180EL V_{IN}=3.6V, V_{OUT}=1.8V / I_{OUT}=0.1mA ⇔30mA

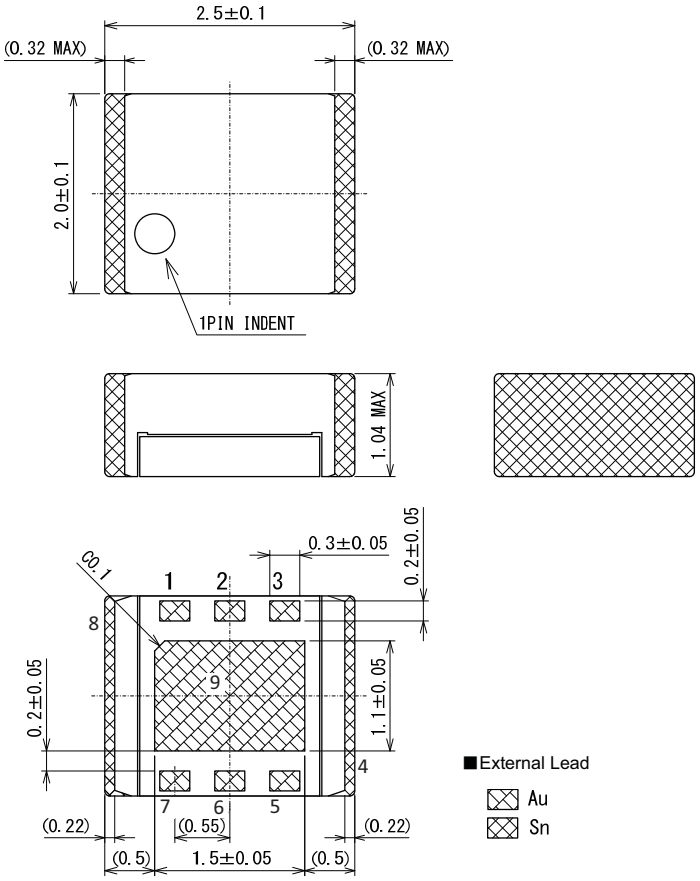


2. TS200L-D5180EL V_{IN}=3.6V, V_{OUT}=1.8V / I_{OUT}=0.1mA ⇔30mA

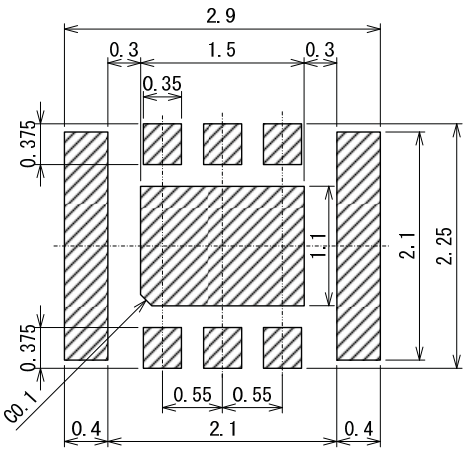


12. PACKAGING INFORMATION

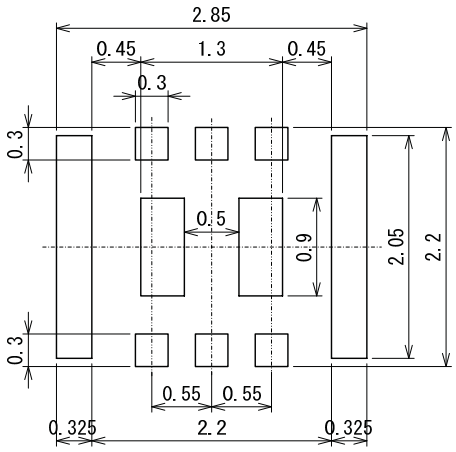
- **IIP-2025 (unit, mm)**



- Reference Pattern Layout (unit, mm)



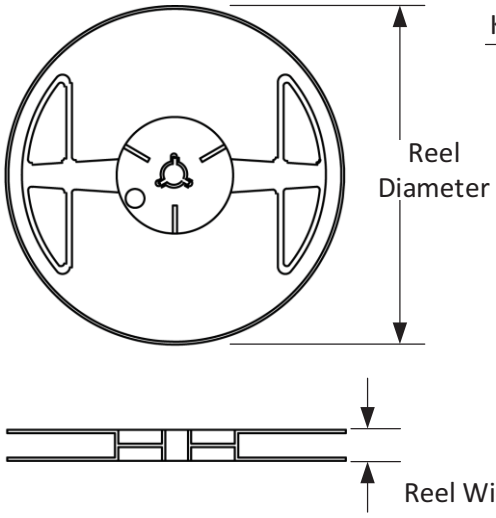
- Reference Metal Mask Design (unit, mm)



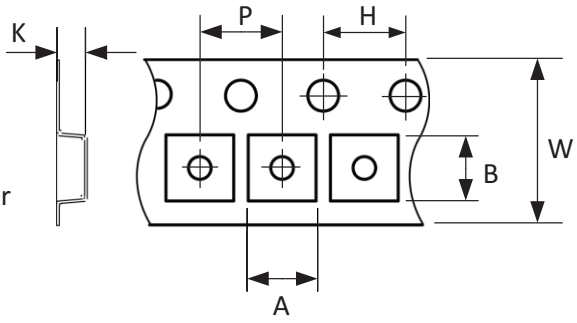
* Implementation of IIP-2025 is recommended within accuracy 0.05mm.

13. TAPE AND REEL INFORMATION

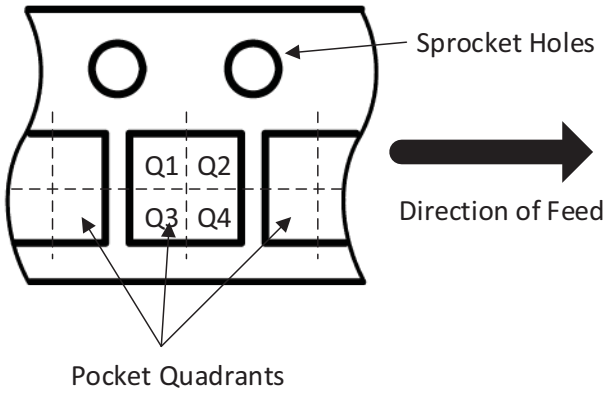
Reel Dimensions



Tape Dimensions



Quadrant Assignments for Pin 1 Orientation in Tape



Device	Package Type	Pins	Pin 1 Quadrant	Reel Diameter	Reel Width W1	A	B	K	P	H	W	Qty/ Reel
TS200L	IIP-2025	9	Q1	180	11.4	2.4	2.9	1.15	4.0	4.0	8.0	3000

14. HANDLING AND SOLDERING

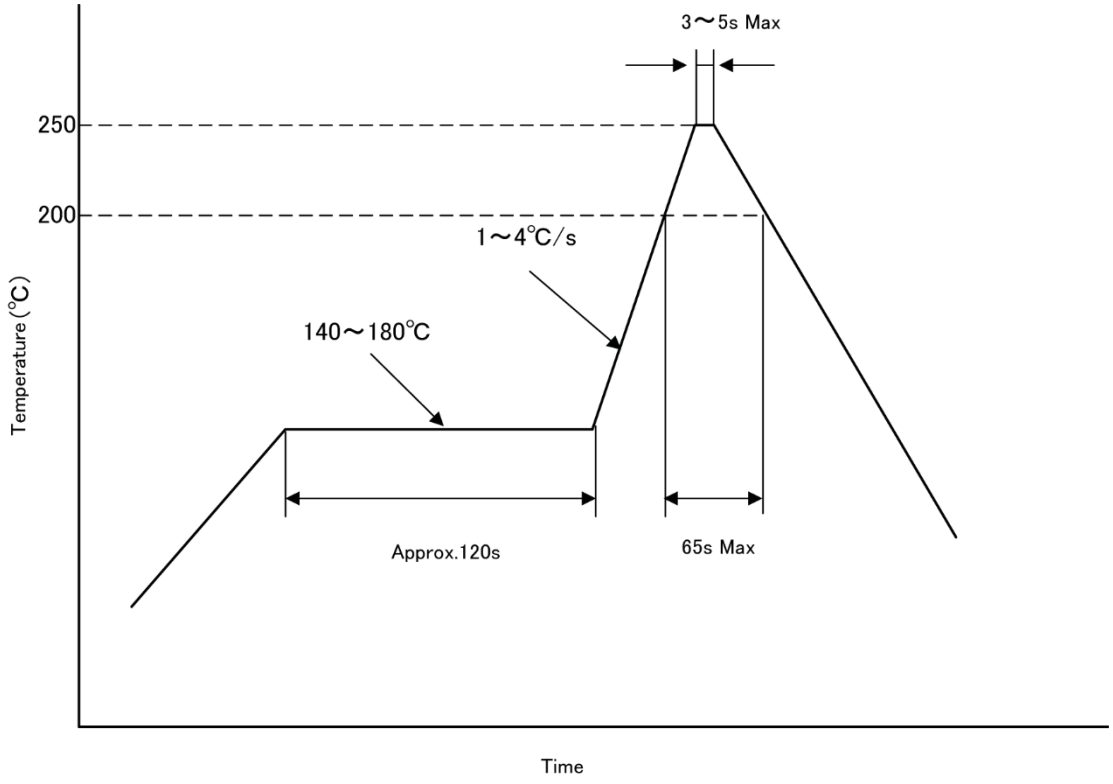
ESD

The TS200L is an electrostatic discharge sensitive device and should be handled in accordance with JESD625-A requirements for Handling Electrostatic Discharge Sensitive (ESDS) Devices. The expecting handling of the Symphony A2 PI chipset during assembly and test is identical to that of a semiconductor device.

Note: JEDEC standards are available for free from the JEDEC website http://www.jedec.org.

Reflow

The TS200L is compatible with lead free soldering processes as defined in IPC/JEDEC J-STD-020. The reflow profile must not exceed the profile given IPC/JEDEC J-STD-020 Table 5-2, “Classification Reflow Profiles”.



Note: JEDEC standards are available for free from the JEDEC website http://www.jedec.org.

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