54V, 135A DC/DC µModule Regulator with PMBus Interface

FEATURES

- **High Efficiency at High Frequency**
  - **Up to 89% Efficiency at 700kHz, $54V_{IN}$ to $0.75V_{OUT}$**
- **PMBus-Compliant I^2C Serial Interface**
  - **Monitor Voltage, Current, Temperature and Faults**
  - **Internal EEPROM Fault Log Record**
  - **Digitally Programmable Control Loop**
  - **Program Voltage, Current Limits, Soft-Start/Soft-Stop, Frequency Synchronization and Phasing, Power-Good, Warnings, and Faults**
- **Wide Input Voltage Range: 45V to 65V**
- **Output Voltage Range: 0.5V to 1.0V**
- **Optimized for 45V to $65V_{IN}$ to $0.75V_{OUT}$**
- **±0.5% Maximum DC Output Error with Differential Remote Voltage Sense**
- **±3% Current Readback Accuracy**
- Parallel and Current Share Multiple µModule ICs
- 22mm × 24mm × 6.7mm Surface-Mounted Package

APPLICATIONS

- High Current Distributed Power Systems
- Servers, Network, and Storage Equipment
- Intelligent Energy Efficient Power Regulation

DESCRIPTION

The LTP™8800-2 is a 135A step-down µModule® (micromodule) regulator that provides microprocessor core voltage from a 54V power distribution architecture. It features remote configurability and telemetry monitoring of power management parameters over PMBus, an open standard I^2C-based digital interface protocol.

The LTP8800-2 comprises a programmable digital control system with precision mixed-signal circuitry, EEPROM, power MOSFETs, planar transformer, inductors, and supporting components. Its high level of integration minimizes component count and design time and maximizes flexibility and power density.

The LTP8800-2 preserves high efficiency at high conversion ratios by utilizing a quasi-resonant architecture that reduces high voltage switching losses.

The LTP8800-2 is available in a 22mm × 24mm × 6.7mm surface-mounted open frame package.

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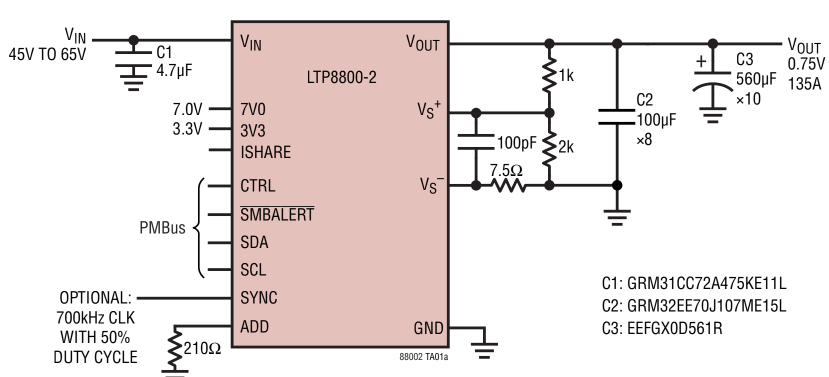
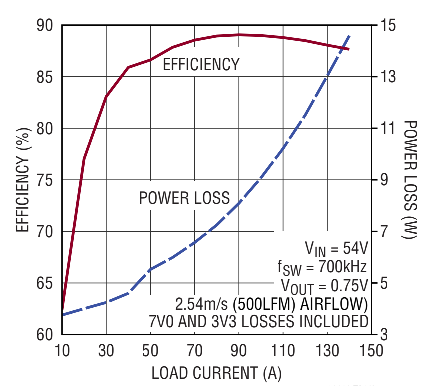
TYPICAL APPLICATION

0.75V, 135A Output DC/DC Module Regulator with PMBus Serial Interface



$0.75V_{OUT}$ Efficiency and Power Loss



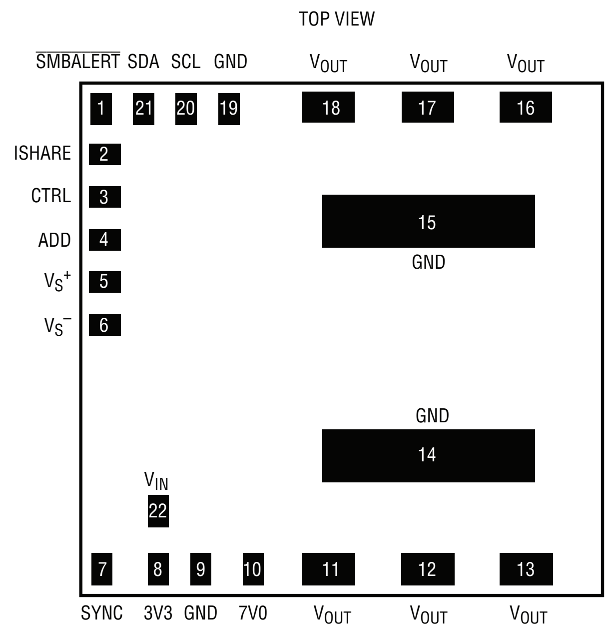
Rev A

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} .... –0.3V to 70V
7V0 .... –0.3V to 7.75V
3V3, SYNC, CTRL, $\overline{\text{SMBALERT}}$, SDA, SCL,
ISHARE, ADD .... –0.3V to 3.6V
V_{OUT}, V_S^+ .... –0.3V to 1.6V
V_S^- .... –0.3V to 0.3V
Operating Junction Temperature Range
LTP8800-2 (Notes 2 and 3) .... 0°C to 125°C
Storage Temperature Range (Note 2) ..... –40°C to 150°C
Peak Solder Reflow Body Temperature .... 245°C

PIN CONFIGURATION



OPEN FRAME PACKAGE
22-PIN (22mm × 24mm × 6.7mm)
WEIGHT = 9.5g

ORDER INFORMATION

LEAD FREE FINISH	PART MARKING	PACKAGE DESCRIPTION	MSL RATING	TEMPERATURE RANGE
LTP8800-2IPV#PBF	LTP8800-2	22-Pin (22mm × 24mm) Open Frame	3	0°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Supply							
V_{IN}	Input Operating Range		●	45		65	V
$V_{IN(UVLO)}$	Input Undervoltage	V_{IN} Rising		38	40	42	V
		V_{IN} Falling		36	38	40	V
$V_{IN(OVLO)}$	Input Overvoltage	V_{IN} Rising		67	70	73	V
		V_{IN} Falling		65	68	71	V
$I_{(VIN)}$	No-Load Input Current, f_{SW} = 700kHz	CTRL = 0V			0.1		mA
	Input Supply Current, f_{SW} = 700kHz	I_{OUT} = 0A, V_{IN} = 54V, V_{OUT} = 0.75V			41		mA
		I_{OUT} = 10A, V_{IN} = 54V, V_{OUT} = 0.75V			0.18		A
		I_{OUT} = 135A, V_{IN} = 54V, V_{OUT} = 0.75V			2.11		A

Rev A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
7V0 Supply							
7V0	7V0 Operating Range		●	6.5	7	7.5	V
$7V0_{(UVLO)}$	7V0 Undervoltage	7V0 Rising	●			4.5	V
		7V0 Falling	●	3.5			V
I_{7V0}	7V0 Input Current		●		0.26	0.40	A
3V3 Supply							
3V3	3V3 Operating Range		●	3.0	3.3	3.6	V
$3V3_{(UVLO)}$	3V3 Undervoltage	3V3 Rising	●			3	V
		3V3 Falling	●	2.75			V
I_{3V3}	3V3 Input Current		●		60	70	mA
Output Specifications							
I_{OUT}	Output Current Range		●	0		135	A
$I_{OUT(MAX)}$	Output Current Limit				175		A
V_{OUT}	Output Voltage Programming Range			0.5		1	V
V_{OUT}	Regulated Output Voltage	I_{OUT} = 0A, V_{IN} = 54V, V_{OUT} Set to 0.800V, T_J = 25°C		0.796	0.800	0.804	V
		I_{OUT} = 0A, V_{IN} = 54V, V_{OUT} Set to 0.800V, T_J = 0°C to 125°C	●	0.788	0.800	0.812	V
$V_{OUT(LOAD+LINE)}$	Line + Load Regulation	I_{OUT} = 0A to 135A, V_{IN} = 45V to 65V	●	0.792	0.800	0.808	V
$V_{OUT(AC)}$	$V_{OUT(PK-PK)}$	V_{IN} = 54V, V_{OUT} = 0.75V, C_{OUT} = 800µF MLCC, 5.6mF POSCAP			5		mV
	$V_{OUT(RMS)}$	V_{IN} = 54V, V_{OUT} = 0.75V, C_{OUT} = 800µF MLCC, 5.6mF POSCAP			2		mV
T_{START}	Start Time	CTRL High to V_{OUT} = 0.75V			10		ms
T_{STOP}	Stop Time	CTRL Low to Output Disable			10		µs
$\Delta V_{OUT(LS)}$	Maximum Output Voltage Excursion for Dynamic Load Step	V_{IN} = 54V, V_{OUT} = 0.75V, C_{OUT} = 800µF MLCC, 5.6mF POSCAP, ΔI_{LOAD} = 35A See waveforms in the Typical Performance Characteristics section.			20		mV
T_{SETTLE}	V_{OUT} Settling Time to 1%	V_{IN} = 54V, V_{OUT} = 0.75V, C_{OUT} = 800µF MLCC, 5.6mF POSCAP, ΔI_{LOAD} = 35A See waveforms in the Typical Performance Characteristics section.			30		µs
Efficiency		V_{IN} = 54V, V_{OUT} = 0.75V, I_{OUT} = 33.75A			84.5		%
		V_{IN} = 54V, V_{OUT} = 0.75V, I_{OUT} = 67.5A			88.3		%
		V_{IN} = 54V, V_{OUT} = 0.75V, I_{OUT} = 101.25A			88.9		%
		V_{IN} = 54V, V_{OUT} = 0.75V, I_{OUT} = 135A			87.8		%
Oscillator							
f_{SW}	Switching Frequency	Switching Frequency set to 700kHz	●	679	700	721	kHz
f_{SYNC}	SYNC Range		●	630	700	770	kHz
PMBus Monitoring							
$I_{MON(OUT)}$	Output Current Monitor	V_{IN} = 54V, V_{OUT} = 0.75V, I_{OUT} = 135A	●		±3		%
$I_{MON(IN)}$	Input Current Monitor	V_{IN} = 54V, V_{OUT} = 0.75V, I_{OUT} = 135A	●		±5		%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUTMON}	Output Voltage Monitor	V_{IN} = 54V, V_{OUT} = 0.75V, I_{OUT} = 0A, T_J = 25°C			±0.5		%
		V_{IN} = 54V, V_{OUT} = 0.75V, I_{OUT} = 0A, T_J = 0°C to 125°C	●	–1.5		+1.5	%
V_{INMON}	Input Voltage Monitor	V_{IN} = 45V to 65V, V_{OUT} = 0.75V, I_{OUT} = 67.5A	●		±2		%
T_{MON}	Temp Monitor	V_{IN} = 54V, V_{OUT} = 0.75V, I_{OUT} = 67.5A	●		±10		°C
Leakage Current Digital Inputs (CTRL, SDA, SCL, SYNC)							
I_{DGTL}	Input Leakage Current	0V ≤ V_{PIN} ≤ 3.6V	●			10	µA
Control Section							
VS_{CM}	VS Common Mode Range		●	–100		+100	mV
V_{MRGN}	Output Voltage Margin Range			0.5		1.0	V
$V_{OUT(OVLO)}$	Output Overvoltage Protection				1.2		V
Digital Inputs (CTRL, SDA, SCL, SYNC)							
V_{IH}	Input High Threshold Voltage	V_{3V3} = 3.3V	●	2.1			V
V_{IL}	Input Low Threshold Voltage	V_{3V3} = 3.3V	●			0.8	V
Digital Outputs (SDA, SMBALERT)							
V_{OL}	Output Low Voltage		●			0.6	V
PMBus Timing Characteristics (SDA, SCL)							
f_{SCL}	Serial Bus Frequency		●	10		400	kHz

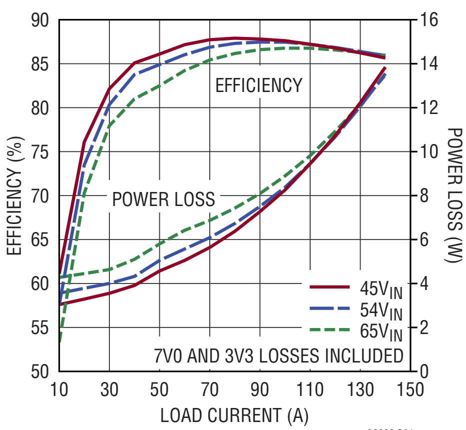
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTP8800-2I is guaranteed over the full 0°C to 125°C operating junction temperature range. Operating lifetime is derated at junction temperatures greater than 125°C.

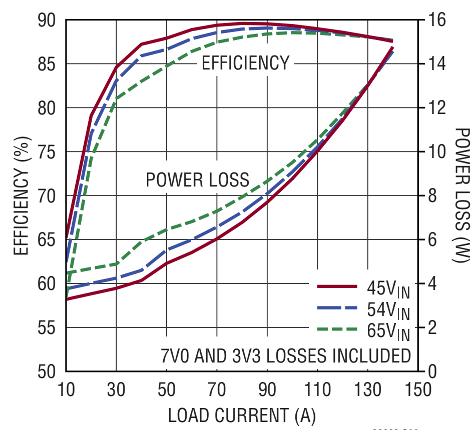
Note 3: The LTP8800-2I includes overtemperature protection intended to protect the device during thermal overload conditions. Internal junction temperature may exceed 150°C if the overtemperature circuitry is active.

TYPICAL PERFORMANCE CHARACTERISTICS

600mV$_{OUT}$ Efficiency and Power Loss vs Output Current

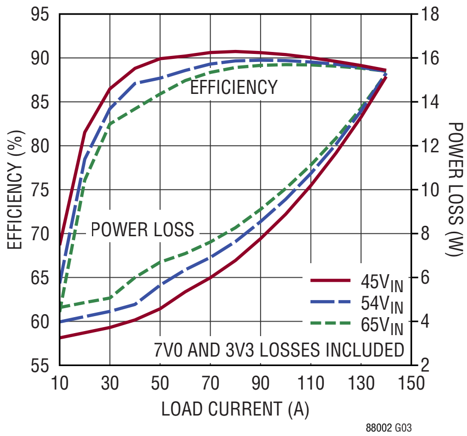


750mV$_{OUT}$ Efficiency and Power Loss vs Output Current



TYPICAL PERFORMANCE CHARACTERISTICS

850mV$_{OUT}$ Efficiency and Power Loss vs. Output Current



Load Transient Response 101A to 135A Load Step 34A/µs 45V$_{IN}$ to 0.75V$_{OUT}$

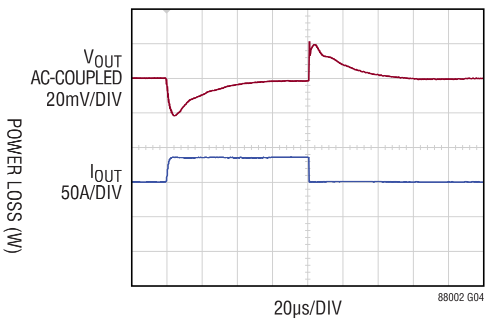
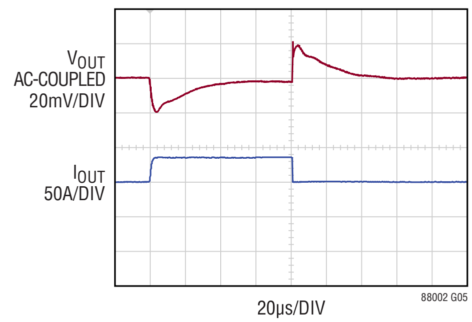


FIGURE 10 CIRCUIT
V_{IN} = 45V, V_{OUT} = 0.75V, f_{SW} = 700kHz
C_{OUT} = 560µF ×10 POSCAP + 100µF ×8 CERAMIC
REG FE01h = 15, REG FE02h = 230,
REG FE03h = 104, REG FE04h = 85

Load Transient Response 101A to 135A Load Step 34/µs 54V$_{IN}$ to 0.75V$_{OUT}$



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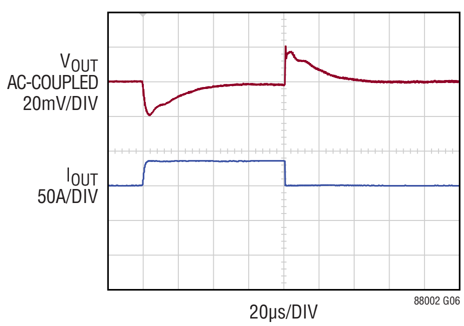
Load Transient Response 101A to 135A Load Step 34A/µs 65V$_{IN}$ to 0.75V$_{OUT}$



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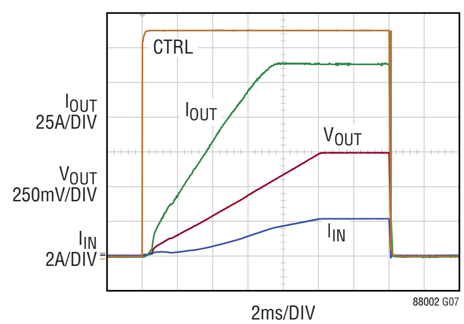
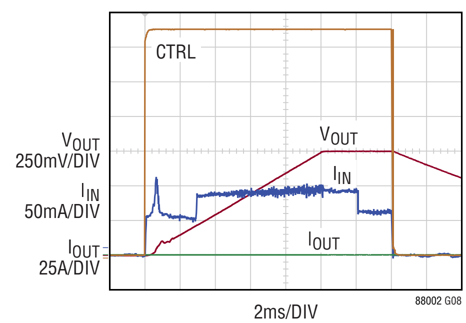
Full Load Start-Up and Shut-Down Triggered by CTRL



No Load Start-Up and Shut-Down Triggered by CTRL



45V$_{IN}$ No Load V$_{OUT}$ Ripple

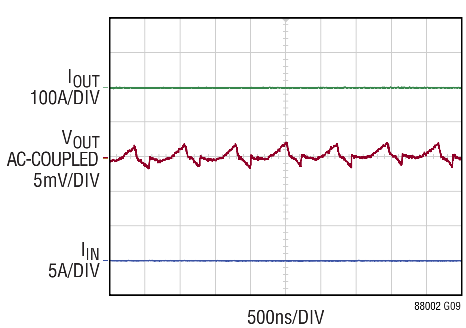


FIGURE 10 CIRCUIT
V_{IN} = 45V, V_{OUT} = 0.75V, f_{SW} = 700kHz
NO LOAD ON V_{OUT}

54V$_{IN}$ No Load V$_{OUT}$ Ripple

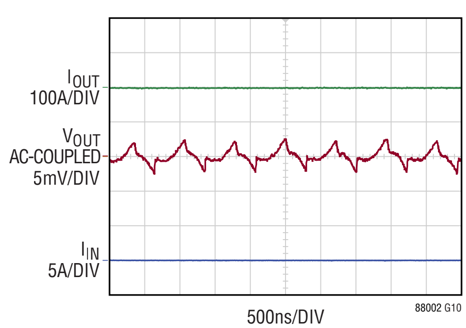


FIGURE 10 CIRCUIT
V_{IN} = 54V, V_{OUT} = 0.75V, f_{SW} = 700kHz
NO LOAD ON V_{OUT}

65V$_{IN}$ No Load V$_{OUT}$ Ripple

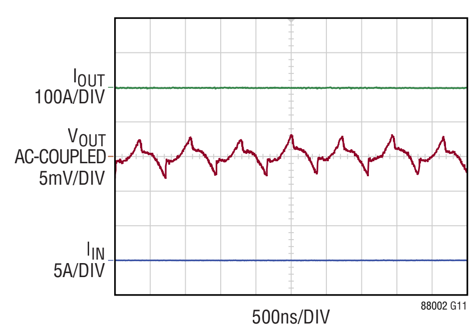


FIGURE 10 CIRCUIT
V_{IN} = 65V, V_{OUT} = 0.75V, f_{SW} = 700kHz
NO LOAD ON V_{OUT}

TYPICAL PERFORMANCE CHARACTERISTICS

$45V_{IN}$ Full Load V_{OUT} Ripple

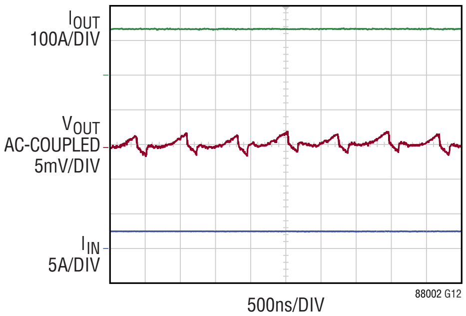


FIGURE 10 CIRCUIT
V_{IN} = 45V, V_{OUT} = 0.75V, f_{SW} = 700kHz
135A LOAD ON V_{OUT}

$54V_{IN}$ Full Load V_{OUT} Ripple

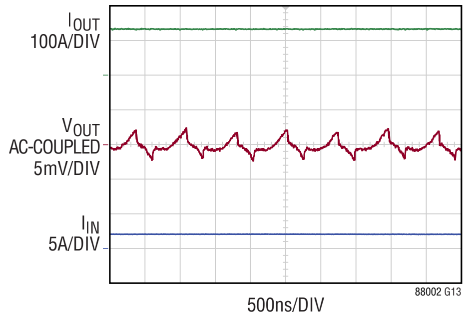


FIGURE 10 CIRCUIT
V_{IN} = 54V, V_{OUT} = 0.75V, f_{SW} = 700kHz
135A LOAD ON V_{OUT}

$65V_{IN}$ Full Load V_{OUT} Ripple

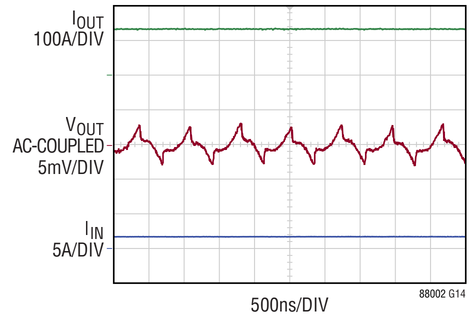
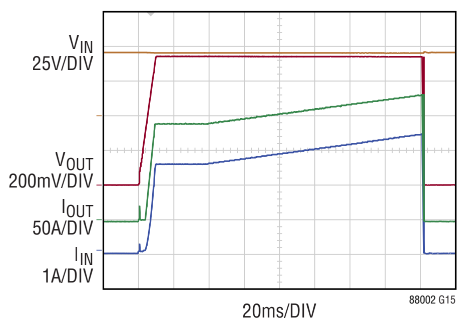
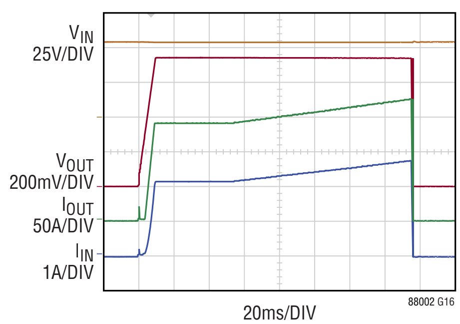


FIGURE 10 CIRCUIT
V_{IN} = 65V, V_{OUT} = 0.75V, f_{SW} = 700kHz
135A LOAD ON V_{OUT}

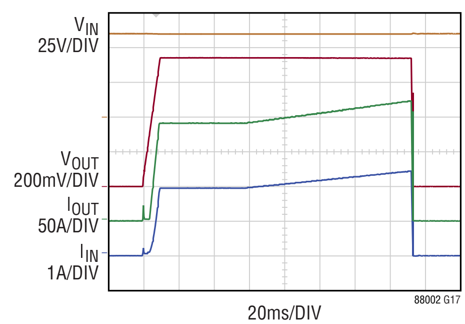
$45V_{IN}$ OCP



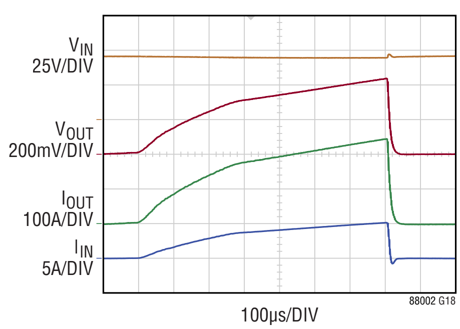
$54V_{IN}$ OCP



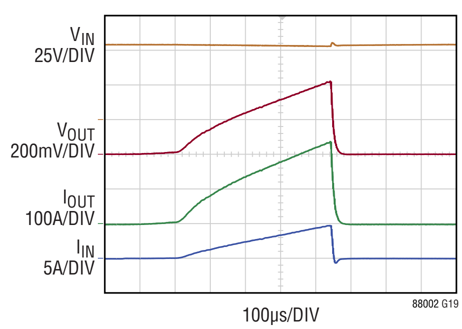
$60V_{IN}$ OCP



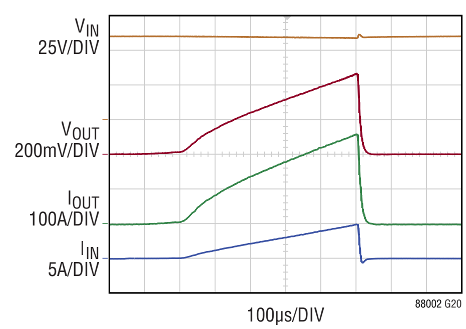
$45V_{IN}$ Short-Circuit Start-Up



$54V_{IN}$ Short-Circuit Start-Up



$60V_{IN}$ Short-Circuit Start-Up



PIN FUNCTIONS

$\overline{\text{SMBALERT}}$ (Pin 1): Power-Good Output (Open-Drain). This pin is also used as the PMBus SMBALERT# signal. If unused, connect to GND.

ISHARE (Pin 2): Analog Current Sharing Input and Output. This pin must connect to other µModule IC's ISHARE pins for current sharing. If not used, this pin should be left floating. Do not load ISHARE with external circuitry.

CTRL (Pin 3): Power Supply ON/OFF Input. This pin performs hardware on/off control. The factory default setting is to enable the LTP8800-2 only when CTRL is logic-high (active-high), but can optionally be changed to active-low, or ignored, using register 0x02.

If this pin is not used, connect to 3V3 if it is configured active-high, or GND if it is configured active-low or ignored.

ADD (Pin 4): I^2C/PMBus Address Select Input. Connect a resistor from ADD to GND. See the Applications Information section for more information about the PMBus address selection.

V_S^+ (Pin 5): Non-Inverting Voltage Sense Input. This pin functions as the Kelvin sense of V_{OUT} at the load as well as the feedback point for the converter control loop. The V_S^+ pin should be tied to a precision feedback resistor divider connected to the output voltage. The V_S^+ pin requires 100pF capacitance to the V_S^- pin placed close to the LTP8800-2. The V_S^+ feedback resistors must have an equivalent parallel resistance < 2k. Otherwise, the control loop may be adversely affected.

V_S^- (Pin 6): Inverting Voltage Sense Input. This pin functions as the Kelvin sense of GND at the load as well as the GND connection for the feedback point for the converter control loop.

SYNC (Pin 7): Synchronization Input Signal. This pin is used as a reference for the internal oscillator and is referenced to GND. Synchronization is disabled by default.

To enable synchronization, set 0xFE55[6] = 0 and then set 0xFE00 = 0b0100000 for the value to take effect.

It is recommended that this input be disabled when not in use. To disable, set 0xFE55[6] = 1 and then set 0xFE00 = 0b0100000 for the value to take effect.

To accomplish phase interleaving of multiple devices, a phase delay in steps of 22.5 degrees can be added using register 0x37[3:0].

3V3 (Pin 8): The 3V3 pin powers internal µModule circuitry. The typical 3V3 supply current when operating is 60mA. The voltage on this pin must be within the specified operating range before the LTP8800-2 can be enabled.

GND (Pins 9, 14, 15, 19): µModule Ground. The GND pins carry high current and must be connected to large planes with sufficient internal layers. Be sure to keep the voltage at the pins roughly equal by taking care of the direction of current flow and debiasing of the ground planes.

7V0 (Pin 10): The 7V0 pin powers internal µModule circuitry, including gate drivers. The typical 7V0 supply current when operating is 0.26A. The voltage on this pin must be within the specified operating range before the LTP8800-2 can be enabled.

V_{OUT} (Pins 11, 12, 13, 16, 17, 18): The V_{OUT} pins carry the high output current of the converter. As such, these pins must be connected to large power planes with sufficient internal layers. The PCB layout must be such that the two sets of V_{OUT} pins see roughly the same voltage. This ensures high efficiency and balanced currents. Output voltage is digitally programmable from 0.5V to 1V. The V_{OUT} pins are two rows of terminals and carry high steady-state output currents (from 0A up to 135A) and transient currents up to 175A.

SCL (Pin 20): I^2C/PMBus Serial Clock Input and Output (Open-Drain).

SDA (Pin 21): I^2C/PMBus Serial Data Input and Output (Open-Drain).

V_{IN} (Pin 22): The V_{IN} pin supplies current to the primary power switches and operates from 54V/48V nominal inputs; for further details, see Absolute Maximum Ratings and Electrical Characteristics table for input voltage range. The LTP8800-2 requires, at minimum, a total of 5µF from low ESR ceramic bypass capacitors, located as close as possible to the V_{IN} and GND pins. One 4.7µF 1206/1210 X7* capacitor is recommended.

APPLICATIONS INFORMATION

COMPENSATION

The LTP8800-2 offers programmable loop compensation to optimize the transient response without any hardware change. A Type 3 filter architecture has been implemented. To tailor the loop response to the specific application, the low frequency gain, zero location, pole location, and high frequency gain can all be set individually. From the sensed voltage to the duty cycle, the transfer function of the filter in z-domain is resolved by Equation 1.

$$H(z) = \left(\frac{D}{LFG} \times \frac{1}{(1-z^{-1})} + \frac{C}{HFG} \frac{\left(1-\frac{B}{256}z^{-1}\right)}{\left(1-\frac{A}{256}z^{-1}\right)} \right) \quad (1)$$

where:

A = filter pole register value (in decimal), 0xFE03.

B = filter zero register value (in decimal), 0xFE02.

C = high frequency gain register value (in decimal), 0xFE04.

D = low frequency gain register value (in decimal), 0xFE01.

$LFG = 4.7744 \times 10^7/f_{SW}$.

$HFG = 2.984 \times 10^6/f_{SW}$.

As shown in Figure 1, adjusting low frequency gain register value changes the gain of the compensation over the low frequency range without moving the pole and zero locations. Adjusting high frequency gain register value changes the gain of the compensation over the high frequency range without moving the pole and zero locations. As shown in Figure 2, adjusting the pole and zero register values move the double-poles and double-zeros of the compensation. Increasing the filter zero and pole register values separate the double-zeros and double-poles. It is recommended that LTpowerPlay® be used to program the filter.

It is recommended that the user determines the appropriate value for the compensation registers using the LTpowerCAD® tool. An example of the bode plot of the typical application circuit with the recommended compensation settings is shown in Figure 3. Measured bode plot of the LTP8800-2 in circuit Figure 9 with register setting (in decimal): 0xFE02 = 226, 0xFE03 = 180, 0xFE04 = 70, 0xFE01 = 8; crossover frequency: 58.35kHz, phase margin 65.8dB, gain margin 11.2dB.

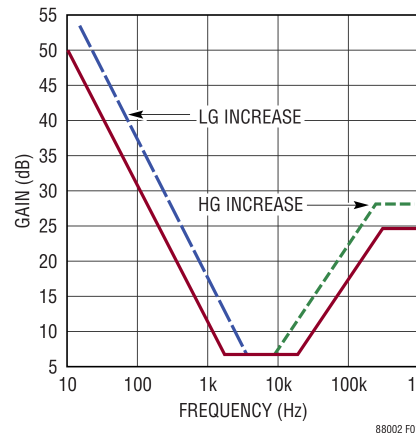


Figure 1. Compensation Gain Adjustment

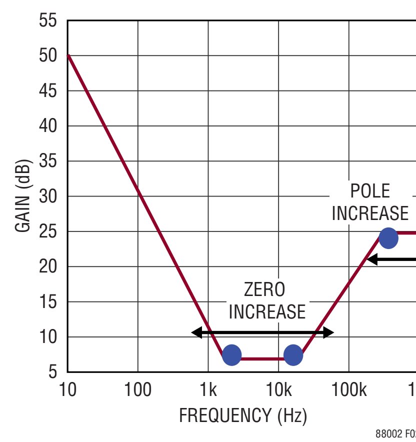


Figure 2. Compensation Poles and Zeros Adjustment

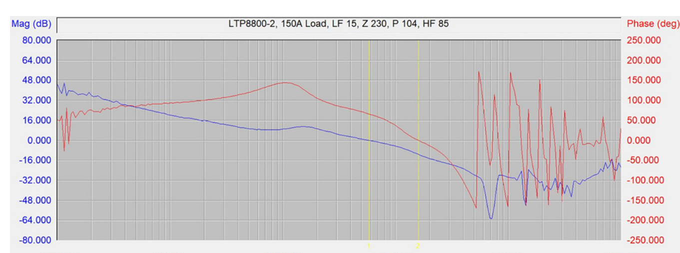


Figure 3. Measured Bode Plot of the LTP8800-2

APPLICATIONS INFORMATION

PolyPhase CONFIGURATION

When configuring a PolyPhase® rail with multiple LTP8800-2, share the SYNC and ISHARE pins, and provide an external clock source. The digital phase-locked loop is capable of determining the frequency on the SYNC pin and locking it to the internal oscillator. The lock or capture range is ±10% of the switching frequency (700kHz). The relative phasing can be configured in steps of 22.5 degrees, using register 0x37[3:0].

PolyPhase LOAD SHARING

Multiple LTP8800-2 can be arrayed to provide a balanced load-share solution by connecting the ISHARE pins. Figure 4 illustrates a 2-phase design sharing connections required for load sharing.

PMBus COMMANDS AND LTpowerPlay

PMBus Commands

There are multiple PMBus commands and manufacturer-specific commands, which can be customized to adjust the settings of LTP8800-2 module, as listed in Table 1. These commands comply to the PMBus Power System Management Protocol. Refer to the PMBus Communication and Command Processing section for details.

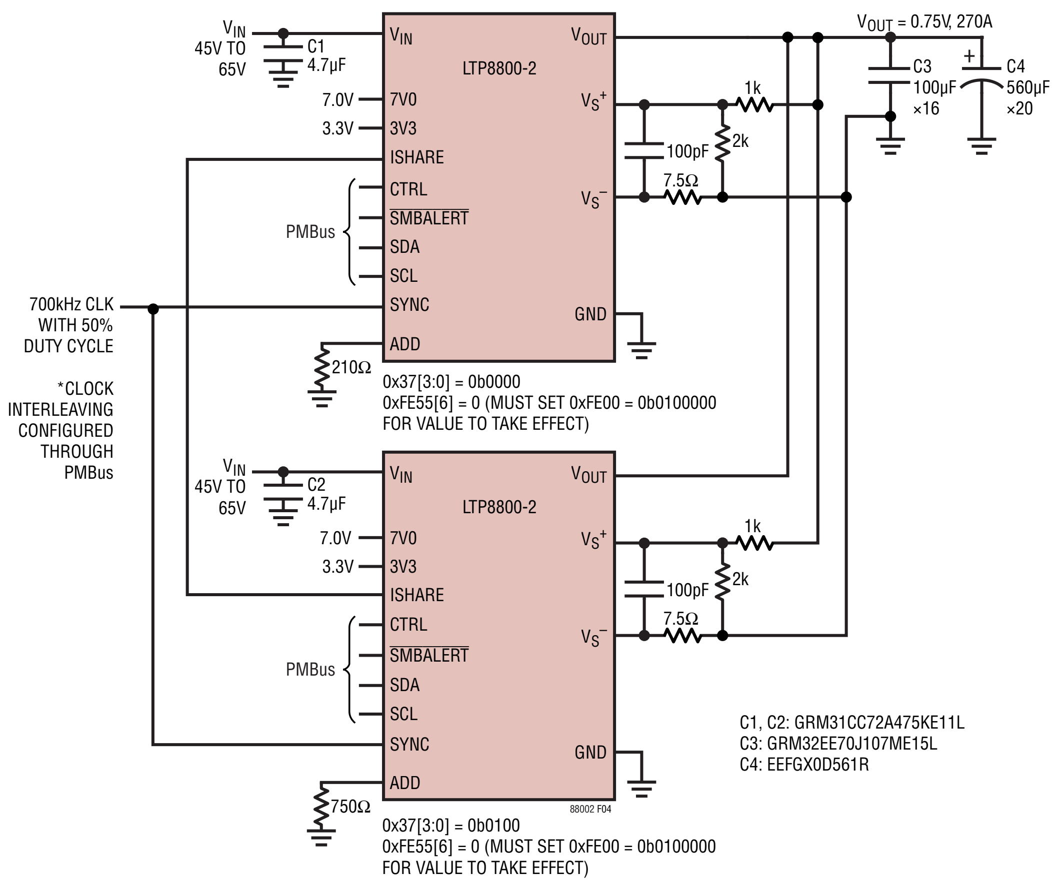


Figure 4. 2-Phase Operation Producing 0.75V at 270A

APPLICATIONS INFORMATION

Table 1. LTP8800-2 Summary of Customizable Commands and Features

PMBus COMMAND NAME OR FEATURE	CMD CODE REGISTER	COMMAND OR FEATURE DESCRIPTION	TYPE	DATA UNITS	DATA FORMAT	NVM ATTRIBUTES
WRITE_PROTECT	0x10	Protect the PMBus device against accidental writes.	R/W Byte	NA	Bit Field	Stored in user-editable NVM.
VIN_ON	0x35	Sets the value of the input voltage (V_{RMS}) at which the device starts power conversion.	R/W Word	Volts	Linear 11	Stored in user-editable NVM.
VIN_OFF	0x36	Sets the value of the input voltage (V_{RMS}) at which the device stops power conversion.	R/W word	Volts	Linear 11	Stored in user-editable NVM.
VIN_OV_FAULT_LIMIT	0x55	Sets the upper voltage threshold (in volts) measured at the sense/input pin that causes an overvoltage fault condition.	R/W Word	Volts	Linear 11	Stored in user-editable NVM.
VIN_UV_FAULT_LIMIT	0x59	Sets the lower voltage threshold (in volts) measured at the sense/input pin that causes an undervoltage fault condition.	R/W Word	Volts	Linear 11	Stored in user-editable NVM.
IIN_OC_FAULT_LIMIT	0x5B	Sets the threshold value (in amperes) measured at the sense/input pin that causes an overcurrent fault condition.	R/W Word	Amps	Linear 11	Stored in user-editable NVM.
POUT_OP_FAULT_LIMIT	0x68	Sets the upper power threshold (in watts) measured at the sense/output pin that causes an output overpower fault condition.	R/W Word	Watts	Linear 11	Stored in user-editable NVM.
NM_DIGFILT_LF_GAIN_SETTING	0xFE01	Determines the low frequency gain of the loop response in normal mode.	R/W Byte	NA	NA	Stored in user-editable NVM.
NM_DIGFILT_ZERO_SETTING	0xFE02	Determines the position of the final zero in normal mode.	R/W Byte	NA	NA	Stored in user-editable NVM.
NM_DIGFILT_POLE_SETTING	0xFE03	Determines the position of the final pole in normal mode.	R/W Byte	NA	NA	Stored in user-editable NVM.
NM_DIGFILT_HF_GAIN_SETTING	0xFE04	Determines the high frequency gain of the loop response in normal mode.	R/W Byte	NA	NA	Stored in user-editable NVM.

APPLICATIONS INFORMATION

LTpowerPlay: AN INTERACTIVE GUI FOR DIGITAL POWER MODULES

The LTpowerPlay is a powerful graphical user interface (GUI) that supports the digital power module LTP8800-2, as shown in Figure 5. In online mode, LTpowerPlay can be used to evaluate single or multiple LTP8800-2 power modules of different types by connecting to a demo board or the user application. In offline mode with no hardware connected through PMBus, LTpowerPlay can also be used to build the project file with configuration of multiple modules, and the project file can be saved and reloaded later.

Moreover, during board bring-up, LTpowerPlay can be used as a valuable diagnostic tool to program the power system, to tweak the system settings, or to diagnose system issues.

The LTpowerPlay utilizes Analog Device's USB-to-I^{2}C/SMBus/PMBus Controller, DC1613A, to communicate with circuit boards including the DC3190B-E (single LTP8800-2 module) demo board or a customer target system. Further context information, including tutorial demos, is available here.

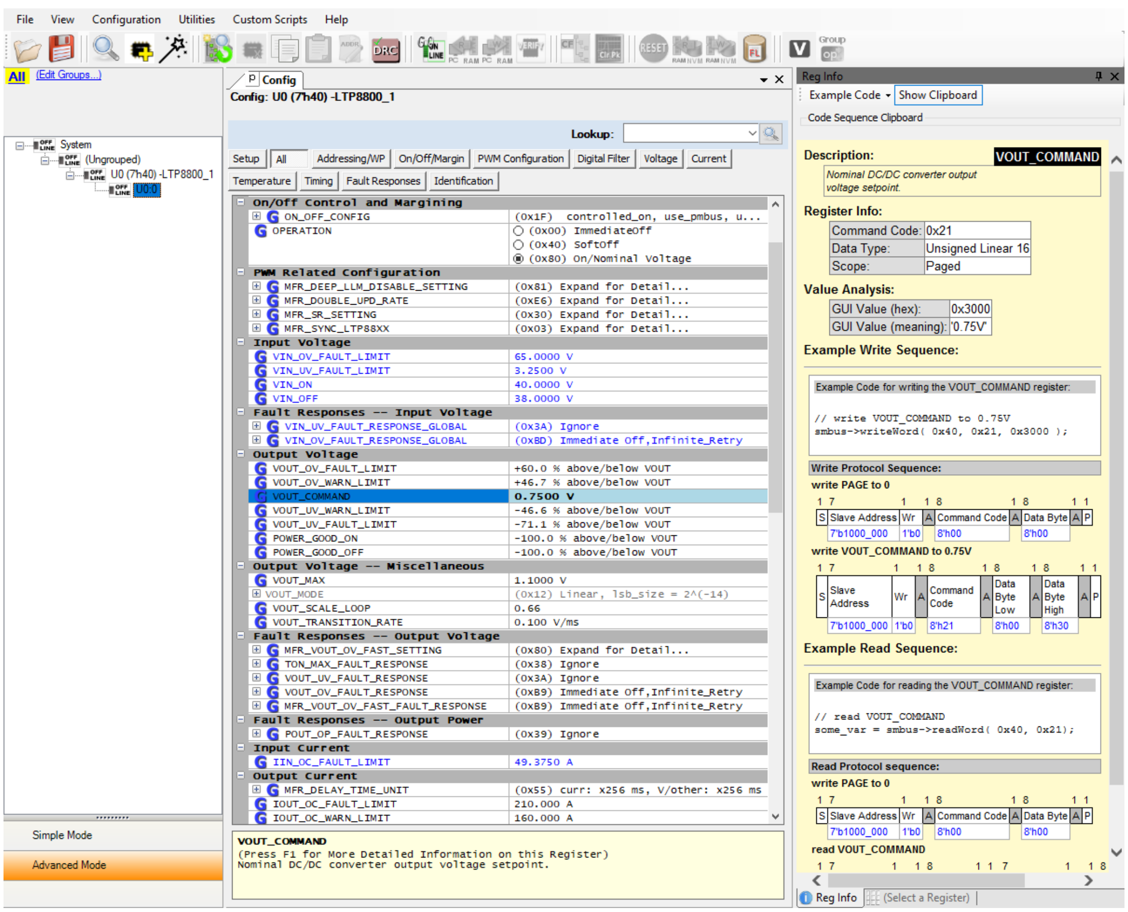


Figure 5. LTpowerPlay Main Interface

APPLICATIONS INFORMATION

PMBus COMMUNICATION AND COMMAND PROCESSING

The LTP8800-2 series communicate through PMBus with other compliant devices. The LTP8800-2 is always configured as a subordinate device in the overall system, requiring a two-wire interface with one data pin (SDA) and one clock pin (SCL). As subordinate devices, LTP8800-2 power modules decode the command sent from the main device and respond accordingly. Data transfer of the PMBus subordinate is based on PMBus commands. According to the PMBus/SMBus/I^2C communication protocol, all PMBus commands start with a subordinate address with the R/W bit cleared (set to 0), followed by the command code, with mostly the stop bit as the last bit in a complete data transfer.

Commands can be categorized as send, read, or write types. For read or write commands, data is transferred between devices in a byte wide format. For send commands, the subordinate device executes the commands upon receiving the stop bit. To ensure robust communication, the main and subordinate devices send acknowledge (ACK) or no acknowledge (NACK) bits as a method of handshaking, eliminating the busy errors between devices.

Manufacturer-specific extended commands are also supported by LTP8800-2. These commands follow the same protocol as the standard PMBus commands. However, the command code consists of two bytes: Command code extension (0xFE) and Extended command code (0x00 to 0xFF). By use of the manufacturer-specific extended commands, the PMBus command set is greatly extended.

PMBus ADDRESS SELECTION

The PMBus address is set by connecting an external resistor from the ADD pin to GND. Table 2 lists the recommended resistor values and associated PMBus addresses.

Table 2. Recommended Resistor Values and Associated PMBus Addresses

PMBus ADDRESS	1% RESISTOR ON ADD PIN (Ω)
0x40	210 (or Connect to GND)
0x41	750
0x42	1330
0x43	2050
0x44	2670
0x45	3570
0x46	4420
0x47	5360
0x48	6340
0x49	7320
0x4A	8450
0x4B	9530
0x4C	10,700
0x4D	12,100
0x4E	13,700
0x4F	15,000 (or Connect to 3V3)

APPLICATIONS INFORMATION

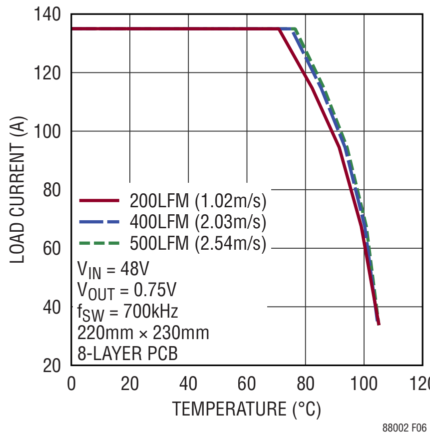


Figure 6. Thermal Derating $48V_{IN}$, $0.75V_{OUT}$

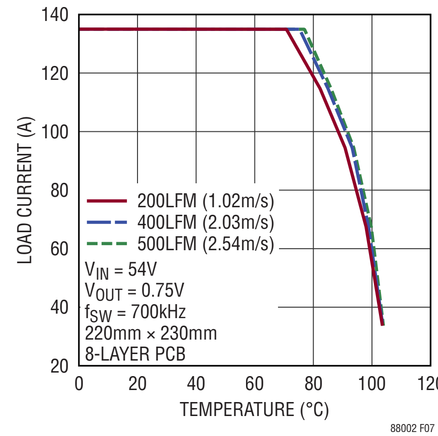
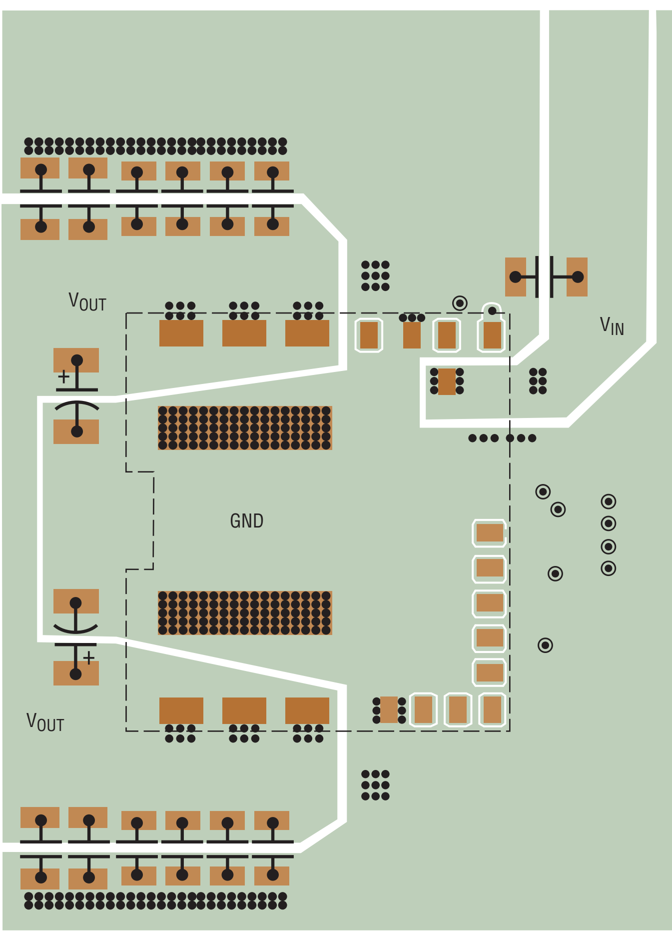
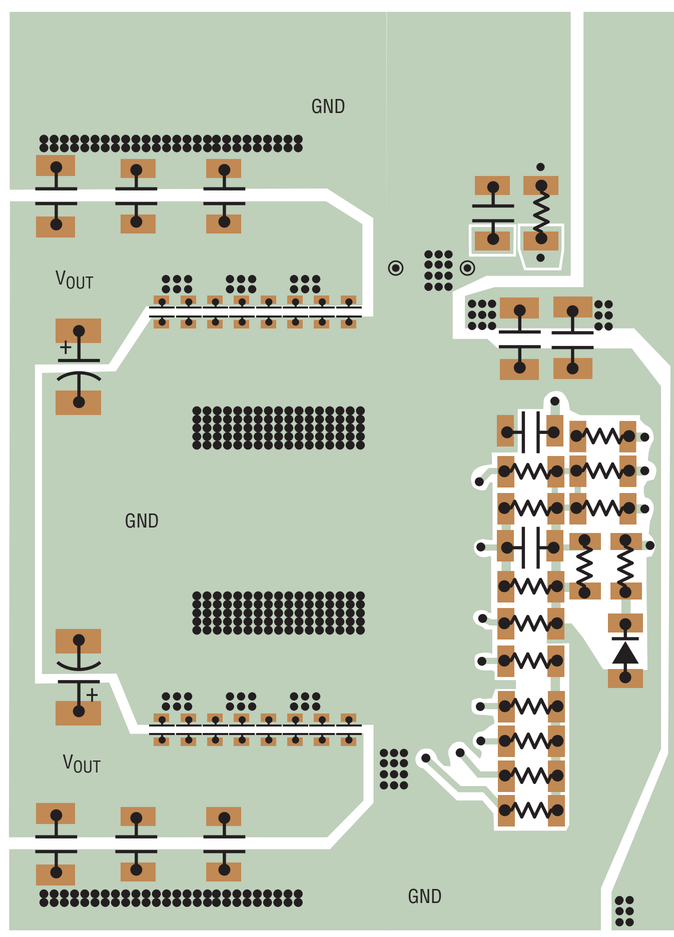


Figure 7. Thermal Derating $54V_{IN}$, $0.75V_{OUT}$



(a) Top Layer



(a) Bottom Layer

Figure 8. Recommended PCB Layout, Top View

TYPICAL APPLICATION

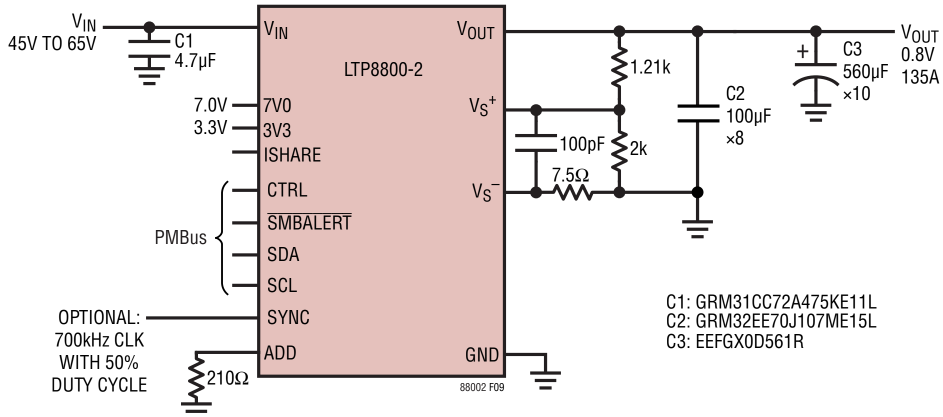


Figure 9. 0.8V, 135A Step-Down Module with PMBus

TYPICAL APPLICATION

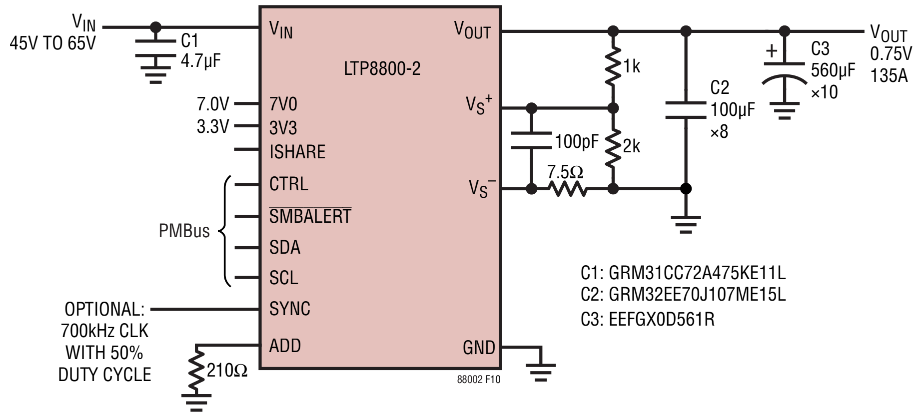


Figure 10. 0.75V, 135A Step-Down Module with PMBus

TYPICAL APPLICATION

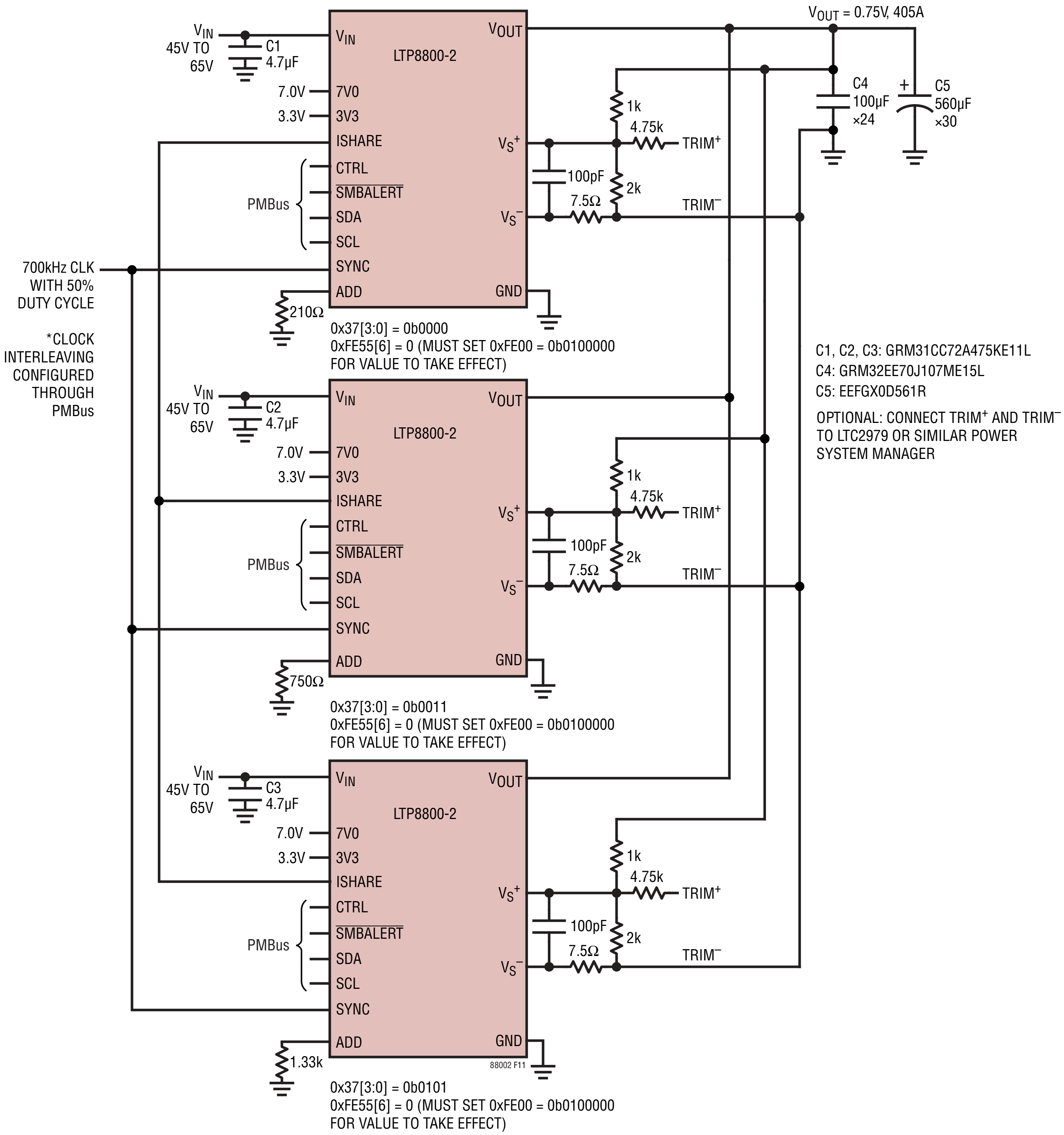
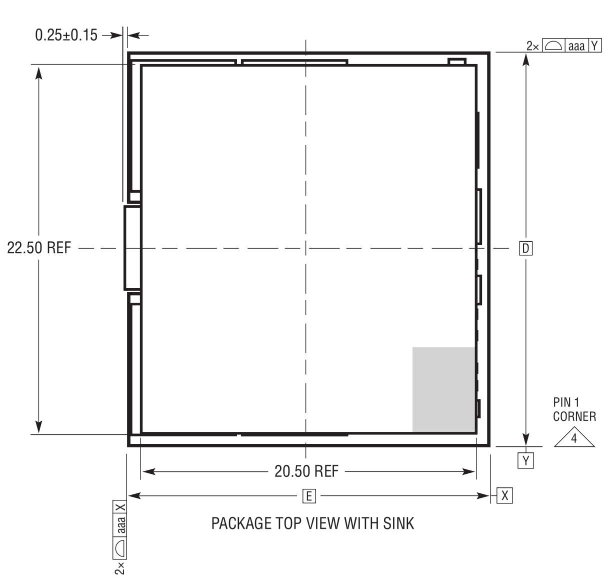


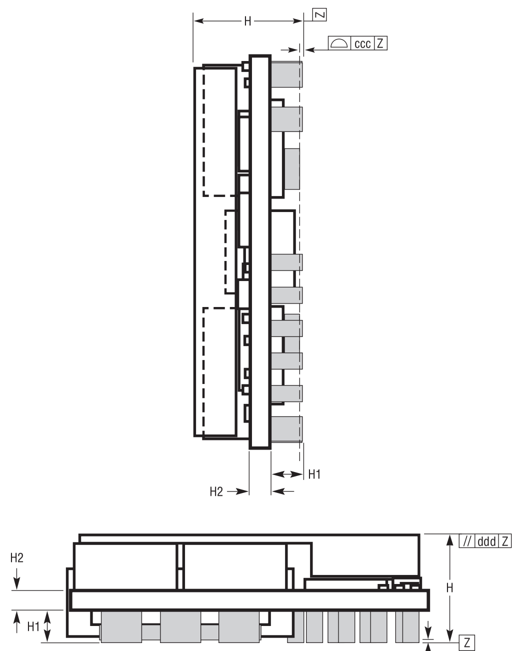
Figure 11. 3-Phase Operation Producing 0.75V at 405A with Power System Management Features

PACKAGE DESCRIPTION

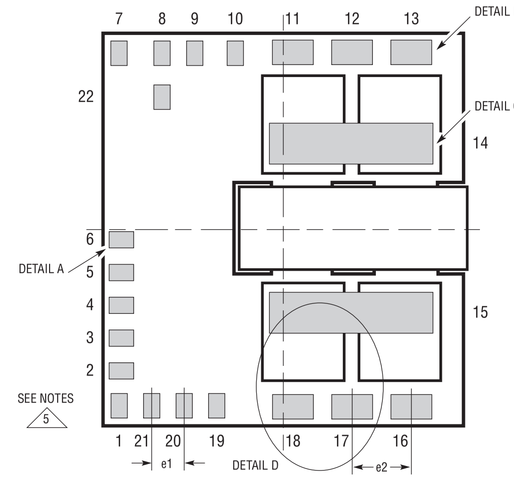
PCA Package
22-Lead (22mm × 24mm × 6.70mm)
(Reference LTC DWG #05-08-7006 Rev B)



PACKAGE TOP VIEW WITH SINK

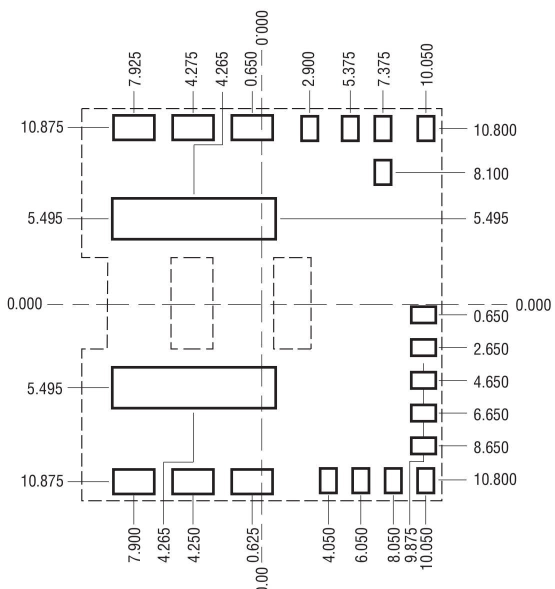


SIDE VIEWS



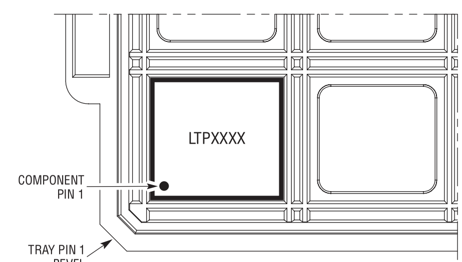
PACKAGE BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PACKAGE PIN LABELING MAY VARY AMONG PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



SUGGESTED PCB LAYOUT
TOP VIEW

DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
D		24.00		
E		22.00		
H	6.35	6.70	7.05	
H1	1.70	1.90	2.10	
H2	1.05	1.20	1.35	PCB THK
e1		2.00		
e2		3.65		
aaa			0.20	
bbb			0.40	
ccc			0.20	
ddd			0.35	
TOTAL NUMBER OF INTERCONNECTS: 22				

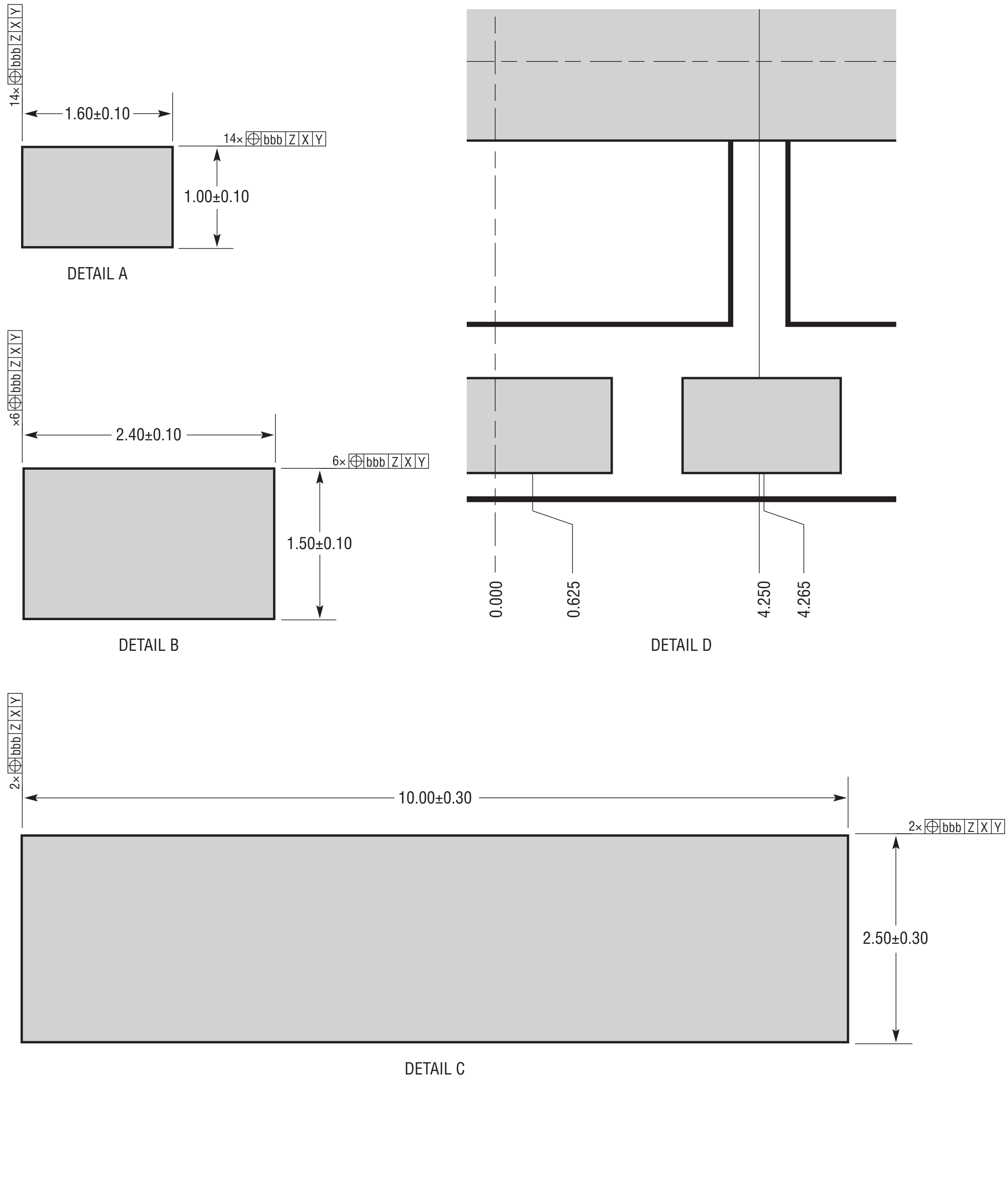


PACKAGE IN TRAY LOADING ORIENTATION

PCA22 0621 REV B

PACKAGE DESCRIPTION

PCA Package
22-Lead (22mm × 24mm × 6.70mm)
(Reference LTC DWG #05-08-7006 Rev B)



REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
0	01/24	Initial Release.	—
A	03/24	Updated Figure 6 and Figure 7	13

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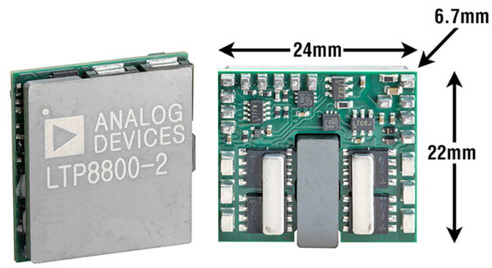
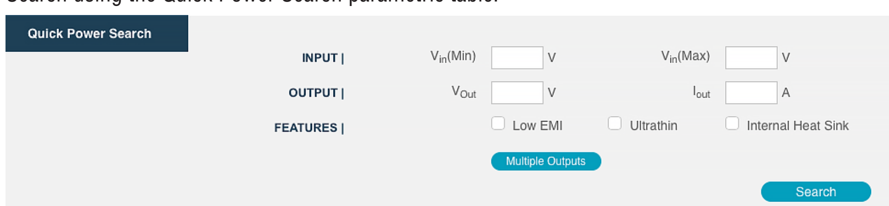
PACKAGE PHOTOS

Part marking is either ink mark or laser mark



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table.	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTP8800-1A	$54V_{IN}$, 150A µModule Regulator with Digital Power System Management, Optimized $0.8V_{OUT}$	$45V \le V_{IN} \le 65V$, $0.5V \le V_{OUT} \le 1.1V$, PMBus with Control and Telemetry, ±0.5% of Maximum DC Output Error, 22mm × 24mm × 6.7mm Surface-Mount Package
LTP8800-4A	$54V_{IN}$, 200A Module Regulator with Digital Power System Management, Optimized for $0.8V_{OUT}$	$45V \le V_{IN} \le 65V$, $0.5V \le V_{OUT} \le 1.1V$, PMBus with Control and Telemetry, ±0.5% of Maximum DC Output Error, 22mm × 24mm × 22mm Surface-Mount Package
LTP8802A-1B	$54V_{IN}$, 140A Module Regulator with Digital Power System Management, Optimized for $3.3V_{OUT}$	$45V \le V_{IN} \le 65V$, $0.5V \le V_{OUT} \le 3.6V$, PMBus with Control and Telemetry, ±0.5% of Maximum DC Output Error, 22mm × 24mm × 22mm Surface-Mount Package
LTP8803-1A	$54V_{IN}$, 160A Module Regulator with Digital Power System Management, Optimized for $1.2V_{OUT}$	$45V \le V_{IN} \le 65V$, $0.5V \le V_{OUT} \le 1.5V$, PMBus with Control and Telemetry, ±0.5% of Maximum DC Output Error, 22mm × 24mm × 22mm Surface-Mount Package
LTM®4664	$54V_{IN}$, Dual 25A or Single 50A µModule Regulator with Digital Power System Management	$30V \le V_{IN} \le 58V$, $0.5V \le V_{OUT} \le 1.5V$, PMBus with Control and Telemetry, ±0.5% of Maximum DC Output Error, 16mm × 16mm × 7.72mm BGA Package
LTM4664A	$54V_{IN}$, Dual 30A or Single 60A µModule Regulator with Digital Power System Management	$30V \le V_{IN} \le 58V$, $0.5V \le V_{OUT} \le 1.2V$. PMBus with Control and Telemetry, ±0.5% of Maximum DC Output Error; 16mm × 16mm × 7.72mm BGA Package
LTM4700	Dual 50A or Single 100A µModule Regulator with Digital Power System Management	$4.5V \le V_{IN} \le 16V$, $0.5V \le V_{OUT} \le 1.8V$, PMBus with Control and Telemetry, ±0.5% of Maximum DC Output Error, 15mm × 22mm × 7.87mm BGA Package
LTM4681	Quad 31.25A or Single 125A µModule Regulator with Digital Power System Management	$4.5V \le V_{IN} \le 16V$, $0.5V \le V_{OUT} \le 3.3V$, PMBus with Control and Telemetry, ±0.5% of Maximum DC Output Error; 15mm × 22mm × 8.17mm BGA Package
LTM4660	60V, 300W Non-Isolated µModule Bus Converter	$30V \le V_{IN} \le 60V$, $7.5V \le V_{OUT} \le 18V$, Up to 300W, 16mm × 16mm × 10.34 BGA Package

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