Datasheet

Tungsten510 SMARC

Version 1.0

Revision History

Version	Date	Notes	Contributors	Approver
0.1	27 Mar 2024	Preliminary Release	Jody Van	Gary Bisson
0.2	13 June 2024	Added SMARC_CAR to orderable parts.	Dave Drogowski	Jonathan Kaye
0.3	21 June 2024	Added DC Consumption Data	Jody Van	Jonathan Kaye
0.4	3 July 2024	Added Reliability Test information	Connie Lin	Jonathan Kaye
1.0	17 Sep 2024	Removed references to JTAG. Initial release.	Dave Drogowski	Jody Van

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1 Scope

This document describes key hardware aspects of Boundary Device's Tungsten510 SMARC system-on-module which is based on the MediaTek Genio 510 (MT8370) processor family and our Sona MT320, based on the the Filogic 320 (MT7921) Wi-Fi/BT combo radio.

Note: Information in this document is subject to change. Contact us for the most updated version of this document.

2 Introduction

The Tungsten510 SMARC module uses the MediaTek Genio 510 (MT8370) processor which integrates a hexa-core CPU with 2 'big core' Arm Cortex-A78 CPUs and 4 'efficiency core' Cortex-A55 CPU, plus a highly capable Arm Mali-G57 GPU with up to 8GB of quad-channel LPDDR4(X) memory.

The highly efficient, in-chip AI multi-processor (APU) offers 4 TOPS performance for Deep Learning (DL), Neural Network (NN) acceleration and Computer Vision (CV) applications when combined with high-detail cameras up to 32MP at 30fps (via in-chip ISP and MIPI-CSI interface). The MediaTek APU supports both efficiency focused INT8 and INT16, and precision focused FP16 tasks.

Using the advanced TSMC N6 (6nm-class) production process allows the Genio 510 to be exceptionally power efficient, enabling product designers to use fanless enclosures or even off-grid power solutions. Extensive platform integration plus a small footprint helps minimize BOM and development costs, accelerating time to market.

Support for up to 4K60 + FHD60 dual displays provide huge screen real-estate, while advanced multimedia encoding/decoding engines (4K75 decode, 4K30 encode), including AV1 decoding, makes the Genio 510 ideal for human-centric applications like interactive advertising, streaming audio and video services, and video conferencing.

A variety of robust control networks for industrial applications are possible via many interfaces: SPI, I2C, UART, USB 3.0, PCIe and Gigabit Ethernet.

The Tungsten510 SMARC with the MT7921 Wi-Fi/BT combo provides IEEE 802.11 ax 2x2 MIMO Wi-Fi capability and a BT 5.3 radio solution. The radio interface is SDIO 3.0 for Wi-Fi and Bluetooth for optimized power usage.

The Tungsten510 SMARC has several product SKUs providing different eMMC and LPDDR4 memory configurations, see Ordering Information section.

3 Tungsten510 SMARC Features Summary

The Tungsten510 SMARC module is based on MT8370 from MediaTek which offers a variety of interfaces and different memory configurations. Most of these interfaces are multiplexed and not able to be used simultaneously.

It complies with the SMARC v2.1 specification from SGET.

Key features of Tungsten510 SMARC are described in Table 1.

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Table 1: Key Features of Tungsten510 SMARC

Feature	Description
CPU	Dual-core Arm Cortex-A78 up to 2 GHz • 64 KB L1 Instruction Cache • 64 KB L1 Data Cache • 256KB private (not shared) L2 cache for each core Quad Cortex-A55 up to 2 GHz • 32 KB L1 Instruction Cache • 32 KB L1 Data Cache • 128KB private (not shared) L2 cache for each core
Memory interface	• On module: Up to 8GB LPDDR4-3200 (size, please refer to Ordering Information) • On module: 8-bits eMMC 5.1 with HS400 speed (size, please refer Ordering Information)
Graphic Processing Unit	Graphics Accelerator Mali-G57 MC3 up to 950 MHz • OpenGL ES 1.1, 2.0, and 3.2 • Vulkan 1.0 and 1.1 • OpenCL 1.0, 1.1, 1.2, 2.0, 2.1, 2.2 • Secure processing of Digital Rights Management (DRM) protected content
Video Processing Unit	Video Decoder (VDEC) • 4K75 HEVC/H.265 Main, Main 10 (up to level 5.1) • 4K75 AV1 Main profile (up to level 5.1) • 4K75 VP9 Profile 0 / 2 • 4K75 H.264 Baseline, Main, High, High 10 profile • 1080p60 H.263 Baseline profile • 1080p60 VP8 • 1080p60 MPEG-2 Main profile • 1080p60 MPEG-4 Simple, Advanced Simple Profile • HEIF Main, Main 10 profile up to 16383 × 16383 Video Encode (VENC) • 4K30 H.264 encoder • 4K30 HEVC/H.265 encoder
AI Processing Unit	Programmable Vision Processor Unit (APU – Cadence VP6) for both AI and CV • TOPS performance: – Fix 8: 0.43 TOPS – Fix 16: 0.11 TOPS – FP16: 0.06 TOPS – FP32: 0.03 TOPS AIA for high computation demanding Neural Network (NN) applications • TOPS performance ○ Fix 8 × Fix 8: 3.7 TOPS ○ Fix 16 × Fix 8: 1.9 TOPS ○ Fix 16 × Fix 16: 0.9 TOPS ○ FP 16/BF 16: 0.9 TOPS

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Feature	Description
Display	HDMI 2.0b Tx (HDMITX) ▪ Up to 4K60 resolution ▪ Compatible with Digital Visual Interface (DVI) 1.0 ▪ High-bandwidth Digital Content Protection (HDCP) 1.4/HDCP 2.3 function ▪ Support Consumer Electronics Control (CEC) DisplayPort Interface (DPTX) ▪ DP v1.4 standard compliant ▪ 4 lanes with up to 5.4 Gbps per lane ▪ Up to 4K60 (10-bit) Embedded DisplayPort Interface (EDPTX) ▪ eDP v1.2 standard compliant ▪ Up to 5.4 Gbps per lane ▪ Up to 1920x1440 @60Hz MIPI Display Serial Interfaces (2x 4-lane DSI) ▪ Throughput up to 1.2 Gbps per data lane ▪ Compliance with MIPI D-PHY Specification v1.2 ▪ Compliance with MIPI C-PHY Specification v1.0 ▪ Second MIPI-DSI requires a BOM change (removing eDP feature)
Imaging	Camera Image Signal Processing (ISP) • Single camera: 32MP @ 30fps • Dual camera: 16MP + 16MP @ 30fps • Video High Dynamic Range (HDR) with stagger HDR sensor: up to 16 MP at 30 fps Face Detection (FD) • Input image formats: o YUV420: 2 plane o YUV422: 2 plane (Y/UV, Y/VU) o YUV422: 1 plane (YUYV, YVYU, UYVY, VYUY) • YUV to RGB888 format conversion • Image up/down-scaling o Maximum resize width: 640 pixels Camera Serial Interface (CSI) • MIPI D-PHY Specification Revision 2.1 • MIPI C-PHY Specification Revision 1.2 • Primary CSI-2 interface (CSI0), can be used in the following configurations: o One 4-data lane interface in D-PHY mode, or o Two 2-data lane interfaces in D-PHY mode, or o One 3-trio interface in C-PHY mode, or o Two 2-trio interfaces in C-PHY mode • Secondary CSI-2 interface (CSI1), can be used in one of the following configurations: o One 4-data lane interface in D-PHY mode, or o One 3-trio interface in C-PHY mode • Pixel formats: RAW8/RAW10/RAW12/RAW14/YUV422 8-bit
Audio	• Two I2S interfaces • Cadence® Tensilica® HiFi 5 Audio Engine Digital Signal Processor (DSP)
Connectivity	• One PCI Express (PCIe) Gen2 Single Lane • Two USB 3.0 Host interfaces (also supports USB 2.0) • Two USB 2.0 Host interfaces • One USB 2.0 OTG interface • One Ultra Secure Digital Host Controller interface • Two Gigabit Ethernet controller (1x RGMII, 1x USB) • Three Universal Asynchronous Receiver/Transmitter (UART) modules • Five I2C modules • Three SPI modules
Security	• Arm® TrustZone® (TZ) architecture

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Feature	Description
Debug Interface	• Debug UART port
RF output	• Two RF output with MHF4 connectors provide flexible external antenna selection for optimized performance • Main antenna: Support both Wi-Fi and BT • Aux Antenna: Support Wi-Fi only

4 Block Diagram

The figure below shows the block diagram of the Tungsten510 SMARC which contains the MediaTek MT8370 processor, PMIC (MT6319 & MT6365) and the MT7921 Wi-Fi/BT combo.

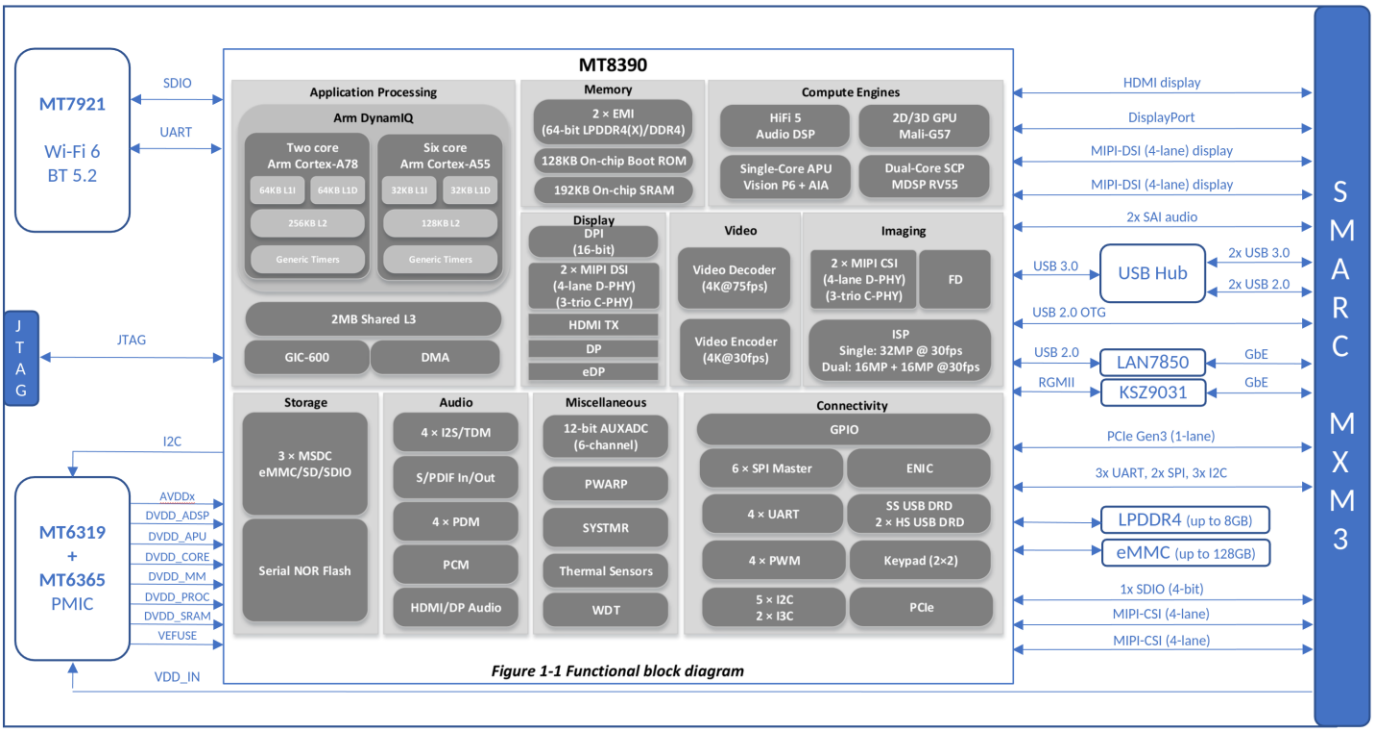

Figure 1: Tungsten510 SMARC block diagram

Detailed connections between the MT7921 and the MT8370 are detailed in Table 2 below.

Table 2: MT7921 to MT8370 Connections

	MT7921	MT8370
SDIO	SD_CLK/SD_CMD/SD0-3	MSDC2_CLK/ MSDC2_CMD/ MSDC2_DAT0-3
PCM	PCM_IN/OUT/SYNC/CLK	PCM_DI/DO/SYNC/CLK
CLK	SUSCLK	RTC32K_1V8_1
BT_EN	W_DISABLE2#	DPI_D14
BT_IRQ	BT_HOST_WAKE	CMMRST1
WL_EN	W_DISABLE1#	CMMPDN1
WL_IRQ	SDIO_WAKE#	GPIO08

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5 Boot mode

The MT8370 SoC can only boot from eMMC as detailed in Table 3.

Table 3: Boot mode combinations

AUD_SYNC_MOSI	BOOT MODE
0	eMMC (default)
1	SPI NOR

6 Electrical Characteristic and Power Consumption

6.1 Absolute Maximum Ratings

Table 4 summarizes the absolute maximum ratings and Table 5 lists the recommended operating conditions for the Tungsten510 SMARC product series. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Note: Maximum rating for signals follows the supply domain of the signals.

Table 4: Absolute maximum ratings

Symbol (Domain)	Parameter	Min.	Max	Unit
VSYS_5V	Input voltage for the SOM	-0.5	+6.0	V
I/O Input/output voltage range	Any I/O pin referred to VDD_1V8; VDDA_1V8; WI-FI_1V8; NVCC_SNVS_1V8	-0.3	+2.1	V
I/O Input/output voltage range	Any I/O pin referred to VDD_3V3; VSD_3V3; NVCC_SD2	-0.3	+3.6	V
$T_{STORAGE}$	Storage Temperature Range	-40	+125	°C
ANT0; ANT1	Maximum RF input (reference to 50-Ω input)	NA	+10	dBm
ESD	Electrostatic discharge tolerance	-2000	+2000	V

6.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
VSYS_5V	Input voltage for the SOM	3.3	5.0	5.5	V
I/O Input/output voltage range	Any I/O pin referred to VDD_1V8; VDDA_1V8; WI-FI_1V8; NVCC_SNVS_1V8	1.71	1.8	1.89	V
I/O Input/output voltage range	Any I/O pin referred to VDD_3V3; VSD_3V3; NVCC_SD2	3.0	3.3	3.6	V
T-ambient	Operating Ambient temperature	-40	25	85	°C

Note: The operating ambient temperature ratings are highly dependent on the design-case, such as the enclosure design, system design, processor activity, GPU/VPU activity, and peripherals used.

Running over 70° C ambient temperature typically requires the implementation of thermal management strategies such as passive (heatsink/spreader). Please contact Ezurio if you need information and guidance for thermal management.

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6.3 DC current consumption

Several power saving modes are available and are listed in Table 6.

Note: These figures are estimates and subject to change.

Table 6: Typical current consumption (VSYS = 3.8V)

Mode	Description	Current (Avg)
RAM Suspend Mode	Memory is in self-refresh, CPU and wireless connection are off.	69mA
Stress Test	Wi-Fi + Ethernet 1 & 2 + CPU/GPU + iPerf.	1004mA
Stress Test	Wi-Fi + Ethernet 1 & 2 + iPerf.	544mA
Idle (All CPU)	Only CPU	145mA

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7 Module pin out and Pinmux table

Table 7: Pinout table for Tungsten510 SMARC edge connector (J2)

SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P1	SMB_ALERT#	**GPIO**: GPIO12 **GPIO**: TP_GPIO4_AO **SPI**: SPIM4_CSB **HDMI**: HDMITX20_HTPLG	DI	1.8 to 5 V	
P2	GND	NA	-	NA	
P3	CSI1_CK+	CSI1A_L2P_T1B	DO	1.8V	
P4	CSI1_CK-	CSI1A_L2N_T1C	DO	1.8V	
P5	GBE1_SDP	NA	-	NA	
P6	GBE0_SDP	**GPIO**: GPIO14 **GPIO**: TP_GPIO6_AO **SPI**: SPIM4_MOSI **HDMI**: HDMITX20_SCL	DI/O	3.3V	
P7	CSI1_RX0+	CSI1A_L1P_T0C	DI	1.8V	
P8	CSI1_RX0-	CSI1A_L1N_T1A	DI	1.8V	
P9	GND	NA	-	NA	
P10	CSI1_RX1+	CSI1B_L0P_T0A	DI	1.8V	
P11	CSI1_RX1-	CSI1B_L0N_T0B	DI	1.8V	
P12	GND	NA	-	NA	
P13	CSI1_RX2+	CSI1A_L0P_T0A	DI	1.8V	
P14	CSI1_RX2-	CSI1A_L0N_T0B	DI	1.8V	
P15	GND	NA	-	NA	
P16	CSI1_RX3+	CSI1B_L1P_T0C	DI	1.8V	
P17	CSI1_RX3-	CSI1B_L1N_T1A	DI	1.8V	
P18	GND	NA	-	NA	
P19	GBE0_MDI3-	TXRXM_D	DI/O	1.8V	From KSZ9031 (U13)
P20	GBE0_MDI3+	TXRXP_D	DI/O	1.8V	From KSZ9031 (U13)
P21	GBE0_LINK100#	LED1	DO	3.3V	From KSZ9031 (U13)
P22	GBE0_LINK1000#	LED2	DO	3.3V	From KSZ9031 (U13)
P23	GBE0_MDI2-	TXRXM_C	DI/O	1.8V	From KSZ9031 (U13)
P24	GBE0_MDI2+	TXRXP_C	DI/O	1.8V	From KSZ9031 (U13)
P25	GBE0_LINK_ACT#	LED1	DO	3.3V	From KSZ9031 (U13)
P26	GBE0_MDI1-	TXRXM_B	DI/O	1.8V	From KSZ9031 (U13)
P27	GBE0_MDI1+	TXRXP_B	DI/O	1.8V	From KSZ9031 (U13)
P28	GBE0_CTREF	TP28	-	NA	Test point
P29	GBE0_MDI0-	TXRXM_A	DI/O	1.8V	From KSZ9031 (U13)
P30	GBE0_MDI0+	TXRXP_A	DI/O	1.8V	From KSZ9031 (U13)
P31	SPI0_CS1#	**GPIO**: GPIO82 **SPI**: SPIM2_MISO **SPI**: SCP_SPI2_MI **I2S**: I2SO1_D0 **UART**: UCTS2 **UART**: TP_UCTS2_AO **PCM**: PCM_DI	DO	1.8V	
P32	GND	NA	-	NA	

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SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P33	SDIO_WP	**GPIO**: GPIO11 **GPIO**: TP_GPIO3_AO **SPDIF**: SPDIF_OUT **I2S**: I2SO1_D0 **DMIC**: DMIC2_DAT_R **CAM**: CMVREF6	DI	1.8 or 3.3V	
P34	SDIO_CMD	**GPIO**: GPIO163 **SDIO**: MSDC1_CMD **SPDIF**: SPDIF_OUT	DI/O	1.8 or 3.3V	
P35	SDIO_CD#	**GPIO**: GPIO02 **GPIO**: TP_GPIO2_AO **SPI**: SPIM5_MOSI **UART**: URTS1 **DMIC**: DMIC3_DAT_R **I2S**: I2SIN_WS **I2S**: I2SO2_WS	DI	1.8 or 3.3V	
P36	SDIO_CK	**GPIO**: GPIO164 **SDIO**: MSDC1_CLK **SPDIF**: SPDIF_IN0	DO	1.8 or 3.3V	
P37	SDIO_PWR_EN	**GPIO**: GPIO111 **I2S**: I2SIN_D1 **I2S**: SPLIN_D1 **DMIC**: DMIC3_CLK **SPDIF**: SPDIF_OUT	DO	3.3V	
P38	GND	NA	-	NA	
P39	SDIO_D0	**GPIO**: GPIO165 **SDIO**: MSDC1_DAT0 **SPDIF**: SPDIF_IN1	DI/O	1.8 or 3.3V	
P40	SDIO_D1	**GPIO**: GPIO166 **SDIO**: MSDC1_DAT1 **SPDIF**: SPDIF_IN2	DI/O	1.8 or 3.3V	
P41	SDIO_D2	**GPIO**: GPIO167 **SDIO**: MSDC1_DAT2 **PWM**: PWM_0	DI/O	1.8 or 3.3V	
P42	SDIO_D3	**GPIO**: GPIO168 **SDIO**: MSDC1_DAT3 **PWM**: PWM_0 **CLK**: CLKM0	DI/O	1.8 or 3.3V	
P43	SPI0_CS0#	**GPIO**: GPIO75 **SPI**: SPIM1_CSB **SPI**: SCP_SPI1_A_CS **TDM**: TDMIN_MCK **I2C**: SCP_SCL0 **CAM**: CMVREF6	DO	1.8V	
P44	SPI0_CK	**GPIO**: GPIO76 **SPI**: SPIM1_CLK **SPI**: SCP_SPI1_A_CK **TDM**: TDMIN_BCK **I2C**: SCP_SDA0 **CAM**: CMVREF7	DO	1.8V	
P45	SPI0_DIN	**GPIO**: GPIO78 **SPI**: SPIM1_MISO **SPI**: SCP_SPI1_A_MI **TDM**: TDMIN_DI **I2C**: SCP_SDA1	DI	1.8V	

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SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P46	SPI0_DO	**GPIO**: GPIO77 **SPI**: SPIM1_MOSI **SPI**: SCP_SPI1_A_MO **TDM**: TDMIN_LRCK **I2C**: SCP_SCL1	DO	1.8V	
P47	GND	NA	-	NA	
P48	SATA_TX+	CSI0A_L0P_T0A	DI	1.8V	SMARC exception
P49	SATA_TX-	CSI0A_L0N_T0B	DI	1.8V	SMARC exception
P50	GND	NA	-	NA	
P51	SATA_RX+	CSI0B_L1P_T0C	DI	1.8V	SMARC exception
P52	SATA_RX-	CSI0B_L1N_T1A	DI	1.8V	SMARC exception
P53	GND	NA	-	NA	
P54	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	**GPIO**: GPIO69 **SPI**: SPIM0_CSB **SPI**: SCP_SPI0_CS **DMIC**: DMIC3_CLK **CAM**: CMVREF0	DO	1.8V	
P55	SPI1_CS1# / ESPI_CS1# / QSPI_CS1#	**GPIO**: GPIO91 **USB**: VBUSVALID_2P **UART**: URXD3	DO	1.8V	
P56	SPI1_CK / ESPI_CK / QSPI_CK	**GPIO**: GPIO70 **SPI**: SPIM0_CLK **SPI**: SCP_SPI0_CK **DMIC**: DMIC3_DAT **CAM**: CMVREF1	DO	1.8V	
P57	SPI1_DIN / ESPI_IO_0 / QSPI_IO_0	**GPIO**: GPIO72 **SPI**: SPIM0_MISO **SPI**: SCP_SPI0_MI **DMIC**: DMIC4_CLK **CAM**: CMVREF3	DI	1.8V	
P58	SPI1_DO / ESPI_IO_1 / QSPI_IO_1	**GPIO**: GPIO71 **SPI**: SPIM0_MOSI **SPI**: SCP_SPI0_MO **DMIC**: DMIC3_DAT_R **CAM**: CMVREF2	DO	1.8V	
P59	GND	NA	-	NA	
P60	USB0+	USB_DP_P0	DI/O	3.3V	
P61	USB0-	USB_DM_P0	DI/O	3.3V	
P62	USB0_EN_OC#	**GPIO**: GPIO84 **USB**: USB_DRVVBUS	DI	3.3V	
P63	USB0_VBUS_DET	**GPIO**: GPIO85 **USB**: VBUSVALID	DI	5V	
P64	USB0_OTG_ID	**GPIO**: GPIO83 **USB**: IDDIG	DI	3.3V	
P65	USB1+	USB2DN_DP2	DI/O	3.3V	From USB Hub (U9)
P66	USB1-	USB2DN_DM2	DI/O	3.3V	From USB Hub (U9)
P67	USB1_EN_OC#	PRT_CTL2	DI	3.3V	From USB Hub (U9)
P68	GND	NA	-	NA	
P69	USB2+	USB2DN_DP3	DI/O	3.3V	From USB Hub (U9)
P70	USB2-	USB2DN_DM3	DI/O	3.3V	From USB Hub (U9)
P71	USB2_EN_OC#	PRT_CTL3	DI	3.3V	From USB Hub (U9)
P72	RSVD	CLKOUT2	DO	1.8V	

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P73	RSVD	NA	-	NA	
P74	USB3_EN_OC#	PRT_CTL1	DI	3.3V	From USB Hub (U9)
P75	PCIE_A_RST#	**GPIO**: GPIO48 **PCI**: PERSTN	-	NA	
P76	USB4_EN_OC#	PRT_CTL4	DI	3.3V	From USB Hub (U9)
P77	PCIE_B_CKREQ#	NA	-	NA	
P78	PCIE_A_CKREQ#	**GPIO**: GPIO49 **PCI**: CLKREQN	DI/O	3.3V	
P79	GND	NA	-	NA	
P80	PCIE_C_REFCK+	NA	-	NA	
P81	PCIE_C_REFCK-	NA	-	NA	
P82	GND	NA	-	NA	
P83	PCIE_A_REFCK+	PCIE_CKP	DO	1.8V	
P84	PCIE_A_REFCK-	PCIE_CKN	DO	1.8V	
P85	GND	NA	-	NA	
P86	PCIE_A_RX+	PCIE_LN0_RXP	DO	1.8V	
P87	PCIE_A_RX-	PCIE_LN0_RXN	DO	1.8V	
P88	GND	NA	-	NA	
P89	PCIE_A_TX+	PCIE_LN0_TXP	DO	1.8V	
P90	PCIE_A_TX-	PCIE_LN0_TXN	DO	1.8V	
P91	GND	NA	-	NA	
P92	HDMI_D2+ / DP1_LANE0+	HDMITX21_CH2_P	DO	1.8V	
P93	HDMI_D2- / DP1_LANE0-	HDMITX21_CH2_M	DO	1.8V	
P94	GND	NA	-	NA	
P95	HDMI_D1+ / DP1_LANE1+	HDMITX21_CH1_P	DO	1.8V	
P96	HDMI_D1- / DP1_LANE1-	HDMITX21_CH1_M	DO	1.8V	
P97	GND	NA	-	NA	
P98	HDMI_D0+ / DP1_LANE2+	HDMITX21_CH0_P	DO	1.8V	
P99	HDMI_D0- / DP1_LANE2-	HDMITX21_CH0_M	DO	1.8V	
P100	GND	NA	-	NA	
P101	HDMI_CK+ / DP1_LANE3+	HDMITX21_CH2_P	DO	1.8V	
P102	HDMI_CK- / DP1_LANE3-	HDMITX21_CH2_M	DO	1.8V	
P103	GND	NA	-	NA	
P104	HDMI_HPD / DP1_HPD	HDMITX_HTPLG	DI	1.8V	
P105	HDMI_CTRL_CK / DP1_AUX+	HDMITX_SCL	DI/O	1.8V	
P106	HDMI_CTRL_DAT / DP1_AUX-	HDMITX_SDA	DI/O	1.8V	
P107	DP1_AUX_SEL	HDMITX_CEC	DI/O	1.8V	SMARC exception

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SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P108	GPIO0 / CAM0_PWR#	**GPIO**: GPIO0 **GPIO**: TP_GPIO0_AO **SPI**: SPIM5_CSB **UART**: UTXD1 **DMIC**: DMIC3_CLK **I2S**: I2SIN_MCK **I2S**: I2SO2_MCK	DI/O	1.8V	
P109	GPIO1 / CAM1_PWR#	**GPIO**: GPIO1 **GPIO**: TP_GPIO1_AO **SPI**: SPIM5_CLK **UART**: URXD1 **DMIC**: DMIC3_DAT **I2S**: I2SIN_BCK **I2S**: I2SO2_BCK	DI/O	1.8V	
P110	GPIO2 / CAM0_RST#	**GPIO**: GPIO50 **HDMI**: HDMITX20_PWR5V **USB**: IDDIG_1P	DI/O	1.8V	
P111	GPIO3 / CAM1_RST#	**GPIO**: GPIO3 **GPIO**: TP_GPIO3_AO **SPI**: SPIM5_MISO **UART**: UCTS1 **DMIC**: DMIC4_CLK **I2S**: I2SIN_D0 **I2S**: I2SO2_D0	DI/O	1.8V	
P112	GPIO4 / HDA_RST#	**GPIO**: GPIO4 **GPIO**: TP_GPIO4_AO **SPDIF**: SPDIF_IN2 **I2S**: I2SO1_MCK **DMIC**: DMIC4_DAT **I2S**: I2SIN_D1 **I2S**: I2SO2_D1	DI/O	1.8V	
P113	GPIO5 / PWM_OUT	**GPIO**: GPIO10 **GPIO**: TP_GPIO2_AO **SPI**: SPIM3_MISO **TDMIN**: TDMIN_DI **DMIC**: DMIC2_DAT **CAM**: CMFLASH1 **PWM**: PWM_1	DI/O	1.8V	
P114	GPIO6 / TACHIN	**GPIO**: GPIO6 **GPIO**: TP_GPIO6_AO **SPDIF**: SPDIF_IN0 **I2S**: I2SO1_WS **DMIC**: DMIC1_CLK **I2S**: I2SIN_D3 **I2S**: I2SO2_D3	DI/O	1.8V	
P115	GPIO7	**GPIO**: GPIO7 **GPIO**: TP_GPIO7_AO **SPI**: SPIM3_CSB **TDMIN**: TDMIN_MCK **DMIC**: DMIC1_DAT **CAM**: CMVREF0 **CAM**: CLKM0	DI/O	1.8V	

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SMARC Pin #	SMARC Pin Name	CPU PIN / Multiplexing (red = default muxing)	I/O	I/O Level	Comments
P116	GPIO8	**GPIO**: GPIO9 **GPIO**: TP_GPIO1_AO **SPI**: SPIM3_MOSI **TDMIN**: TDMIN_LRCK **DMIC**: DMIC2_CLK **CAM**: CMFLASH0 **PMW**: PWM_0	DI/O	1.8V	
P117	GPIO9	**GPIO**: GPIO43 **KP**: KPCOL1 **DP**: DP_TX_HPD **CAM**: CMFLASH2	DI/O	1.8V	
P118	GPIO10	**GPIO**: GPIO44 **KP**: KPROW0	DI/O	1.8V	
P119	GPIO11	**GPIO**: GPIO45 **KP**: KPROW1 **EDP**: EDP_TX_HPD **CAM**: CMFLASH3 **I2S**: I2SIN_MCK	DI/O	1.8V	
P120	GND	NA	-	NA	
P121	I2C_PM_CK	**GPIO**: GPIO57 **I2C**: SCL1	DI/O	1.8V	
P122	I2C_PM_DAT	**GPIO**: GPIO58 **I2C**: SDA1	DI/O	1.8V	
P123	BOOT_SEL0#	NA	-	NA	
P124	BOOT_SEL1#	NA	-	NA	
P125	BOOT_SEL2#	NA	-	NA	
P126	RESET_OUT#	**GPIO**: GPIO130 **DMIC**: DMIC2_DAT_R **SPI**: SPINOR_IO3 **SPDIF**: SPDIF_IN2 **TCSYS**: LVTS_SDI	DI/O	1.8V	
P127	RESET_IN#	SYSRSTB	DI	1.8V	AND gated with MT6365 (U200) RESETB signal
P128	POWER_BTN#	PWRKEY	DI	1.8 - 5V	From MT6365 PMIC (U200)
P129	SER0_TX	**GPIO**: GPIO33 **UART**: UTXD1 **UART**: URTS2 **UART**: TP_UTXD1_AO	DO	1.8V	
P130	SER0_RX	**GPIO**: GPIO34 **UART**: URXD1 **UART**: UCTS2 **UART**: TP_URXD1_AO	DI	1.8V	
P131	SER0_RTS#	**GPIO**: GPIO35 **UART**: UTXD2 **UART**: URTS1 **UART**: TP_URTS1_AO **UART**: TP_UTXD2_AO	DI	1.8V	
P132	SER0_CTS#	**GPIO**: GPIO36 **UART**: URXD2 **UART**: UCTS1 **UART**: TP_UCTS1_AO **UART**: TP_URXD2_AO	DO	1.8V	
P133	GND	NA	-	NA	

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P134	SER1_TX	**GPIO**: GPIO31 **UART**: UTXD0 **UART**: TP_UTXD1_AO **UART**: TP_UTXD2_AO	DO	1.8V	
P135	SER1_RX	**GPIO**: GPIO32 **UART**: URXD0 **UART**: TP_URXD1_AO **UART**: TP_URXD2_AO	DI	1.8V	
P136	SER2_TX	**GPIO**: GPIO16 **GPIO**: TP_GPIO0_AO **UART**: UTXD3 **HDMI**: HDMITX20_PWR5V	DO	1.8V	
P137	SER2_RX	**GPIO**: GPIO17 **GPIO**: TP_GPIO1_AO **UART**: URXD3 **CAM**: CMFLASH2 **EDP**: EDP_TX_HPD **CAM**: CMVREF7	DI	1.8V	
P138	SER2_RTS#	NA	-	NA	
P139	SER2_CTS#	NA	-	NA	
P140	SER3_TX	NA	-	NA	
P141	SER3_RX	NA	-	NA	
P142	GND	NA	-	NA	
P143	CAN0_TX	NA	-	NA	
P144	CAN0_RX	NA	-	NA	
P145	CAN1_TX	NA	-	NA	
P146	CAN1_RX	NA	-	NA	
P147	VDD_IN	VSYS	A	3.0 - 5.25V	
P148	VDD_IN	VSYS	A	3.0 - 5.25V	
P149	VDD_IN	VSYS	A	3.0 - 5.25V	
P150	VDD_IN	VSYS	A	3.0 - 5.25V	
P151	VDD_IN	VSYS	A	3.0 - 5.25V	
P152	VDD_IN	VSYS	A	3.0 - 5.25V	
P153	VDD_IN	VSYS	A	3.0 - 5.25V	
P154	VDD_IN	VSYS	A	3.0 - 5.25V	
P155	VDD_IN	VSYS	A	3.0 - 5.25V	
P156	VDD_IN	VSYS	A	3.0 - 5.25V	
S1	CSI1_TX+ / I2C_CAM1_CK	**GPIO**: GPIO63 **I2C**: SCL4	DO	1.8V	
S2	CSI1_TX- / I2C_CAM1_DAT	**GPIO**: GPIO64 **I2C**: SDA4	DI/O	1.8V	
S3	GND	NA	-	NA	
S4	RSVD	NA	-	NA	
S5	I2C_CAM0_CK / CSI0_TX-	**GPIO**: GPIO61 **I2C**: SCL3 **I2C**: SCP_SCL0 **I2C**: SCP_SCL1	DO	1.8V	
S6	CAM_MCK	**GPIO**: GPIO23 **CAM**: CMMCLK1 **PWM**: PWM_2 **GPIO**: TP_GPIO7_AO **DP**: DP_TX_HPD	DO	1.8V	

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S7	I2C_CAM0_DAT / CSI0_TX+	**GPIO**: GPIO62 **I2C**: SDA3 **I2C**: SCP_SDA0 **I2C**: SCP_SDA1	DI/O	1.8V	
S8	CSI0_CK+	CSI0A_L2P_T1B	DO	1.8V	
S9	CSI0_CK-	CSI0A_L2N_T1C	DO	1.8V	
S10	GND	NA	-	NA	
S11	CSI0_RX0+	CSI0A_L1P_T0C	DI	1.8V	
S12	CSI0_RX0-	CSI0A_L1N_T1A	DI	1.8V	
S13	GND	NA	-	NA	
S14	CSI0_RX1+	CSI0B_L0P_T0A	DI	1.8V	
S15	CSI0_RX1-	CSI0B_L0N_T0B	DI	1.8V	
S16	GND	NA	-	NA	
S17	GBE1_MDI0+	TR0_P	DI/O	1.8V	From LAN7850 (U14)
S18	GBE1_MDI0-	TR0_N	DI/O	1.8V	From LAN7850 (U14)
S19	GBE1_LINK100#	LED1	DO	3.3V	From LAN7850 (U14)
S20	GBE1_MDI1+	TR1_P	DI/O	1.8V	From LAN7850 (U14)
S21	GBE1_MDI1-	TR1_N	DI/O	1.8V	From LAN7850 (U14)
S22	GBE1_LINK1000#	LED0	DO	3.3V	From LAN7850 (U14)
S23	GBE1_MDI2+	TR2_P	DI/O	1.8V	From LAN7850 (U14)
S24	GBE1_MDI2-	TR2_N	DI/O	1.8V	From LAN7850 (U14)
S25	GND	NA	-	NA	
S26	GBE1_MDI3+	TR3_P	DI/O	1.8V	From LAN7850 (U14)
S27	GBE1_MDI3-	TR3_N	DI/O	1.8V	From LAN7850 (U14)
S28	GBE1_CTREF	NA	-	NA	
S29	PCIE_D_TX+ / SERDES_0_TX+	NA	-	NA	
S30	PCIE_D_TX- / SERDES_0_TX-	NA	-	NA	
S31	GBE1_LINK_ACT#	LED2	DO	3.3V	
S32	PCIE_D_RX+ / SERDES_0_RX+	NA	-	NA	
S33	PCIE_D_RX- / SERDES_0_RX-	NA	-	NA	
S34	GND	NA	-	NA	
S35	USB4+	USB2DN_DP4	DI/O	3.3V	From USB Hub (U9)
S36	USB4-	USB2DN_DM4	DI/O	3.3V	From USB Hub (U9)
S37	USB3_VBUS_DET	NA	-	NA	
S38	AUDIO_MCK	**GPIO**: GPIO119 **I2S**: I2SO2_D2 **I2S**: I2SIN_D2 **UART**: UTXD3 **TDMIN**: TDMIN_LRCK **I2S**: I2SO1_MCK	DO	1.8V	
S39	I2S0_LRCK	**GPIO**: GPIO112 **I2S**: I2SIN_D2 **I2S**: SPLIN_D2 **DMIC**: DMIC3_DAT **TDMIN**: TDMIN_MCK **I2S**: I2SO1_WS	DI/O	1.8V	

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S40	I2S0_SDOUT	**GPIO**: GPIO113 **I2S**: I2SIN_D3 **I2S**: SPLIN_D3 **DMIC**: DMIC3_DAT_R **TDMIN**: TDMIN_BCK **I2S**: I2SO1_D0	DO	1.8V	
S41	I2S0_SDIN	**GPIO**: GPIO110 **I2S**: I2SIN_D0 **SPLIN**: SPLIN_D0 **DMIC**: DMIC4_DAT_R **CAM**: CMVREF7 **AUXIF**: AUXIF_CLK1	DI	1.8V	
S42	I2S0_CK	**GPIO**: GPIO120 **I2S**: I2SO2_D3 **I2S**: I2SIN_D3 **UART**: URXD3 **TDMIN**: TDMIN_DI **I2S**: I2SO1_BCK	DI/O	1.8V	
S43	ESPI_ALERT0#	**GPIO**: GPIO81 **SPI**: SPIM2_MOSI **SCPI**: SCP_SPI2_MO **I2S**: I2SO1_WS **UART**: URTS2 **UART**: TP_URTS2_AO **PCM**: PCM_DO	DI/O	1.8V	
S44	ESPI_ALERT1#	**GPIO**: GPIO79 **SPI**: SPIM2_CSB **SCPI**: SCP_SPI2_CS **I2S**: I2SO1_MCK **UART**: UTXD2 **UART**: TP_UTXD2_AO **PCM**: PCM_SYNC	DI/O	1.8V	
S45	MDIO_CLK	NA	DI/O	1.8V	
S46	MDIO_DAT	NA	DI/O	1.8V	
S47	GND	NA	-	NA	
S48	I2C_GP_CK	**GPIO**: GPIO55 **I2C**: SCL0 **I2C**: SCP_SCL0 **I2C**: SCP_SCL1	DO	1.8V	
S49	I2C_GP_DAT	**GPIO**: GPIO56 **I2C**: SDA0 **I2C**: SCP_SDA0 **I2C**: SCP_SDA1	DI/O	1.8V	
S50	I2S2_LRCK / HDA_SYNC	**GPIO**: GPIO109 **I2S**: I2SIN_WS **I2S**: SPLIN_BCK **DMIC**: DMIC4_DAT **CAM**: CMVREF6 **AUXIF**: AUXIF_ST1	DI/O	1.8V	
S51	I2S2_SDOUT / HDA_SDO	**GPIO**: GPIO117 **I2S**: I2SO2_D0 **I2S**: I2SIN_D0	DO	1.8V	
S52	I2S2_SDIN / HDA_SDI	**GPIO**: GPIO118 **I2S**: I2SO2_D1 **I2S**: I2SIN_D1	DI	1.8V	

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S53	I2S2_CK / HDA_CK	**GPIO**: GPIO115 **I2S**: I2SO2_BCK **I2S**: I2SIN_BCK	DI/O	1.8V	
S54	SATA_ACT#	NA	-	NA	
S55	USB5_EN_OC#	NA	-	NA	
S56	ESPI_IO_2 / QSPI_IO_2	**GPIO**: GPIO73 **SPI**: SPIM0_MIO2 **UART**: UTXD3 **DMIC**: DMIC4_DAT **CLK**: CLKM0 **CAM**: CMVREF4	DI/O	1.8V	
S57	ESPI_IO_3 / QSPI_IO_3	**GPIO**: GPIO74 **SPI**: SPIM0_MIO3 **UART**: URXD3 **DMIC**: DMIC4_DAT_R **CLK**: CLKM1 **CAM**: CMVREF5	DI/O	1.8V	
S58	ESPI_RESET#	**GPIO**: GPIO114 **I2S**: I2SO2_MCK **I2S**: I2SIN_MCK	DI/O	1.8V	
S59	USB5+	NA	-	NA	
S60	USB5-	NA	-	NA	
S61	GND	NA	-	NA	
S62	USB3_SSTX+	USB3DN_TXDP1	DI/O	3.3V	From USB Hub (U9)
S63	USB3_SSTX-	USB3DN_TXDM1	DI/O	3.3V	From USB Hub (U9)
S64	GND	NA	-	NA	
S65	USB3_SSRX+	USB3DN_RXDP1	DI/O	3.3V	From USB Hub (U9)
S66	USB3_SSRX-	USB3DN_RXDM1	DI/O	3.3V	From USB Hub (U9)
S67	GND	NA	-	NA	
S68	USB3+	USB2DN_DP1	DI/O	3.3V	From USB Hub (U9)
S69	USB3-	USB2DN_DM1	DI/O	3.3V	From USB Hub (U9)
S70	GND	NA	-	NA	
S71	USB2_SSTX+	USB3DN_TXDP3	DI/O	3.3V	From USB Hub (U9)
S72	USB2_SSTX-	USB3DN_TXDM3	DI/O	3.3V	From USB Hub (U9)
S73	GND	NA	-	NA	
S74	USB2_SSRX+	USB3DN_RXDP3	DI/O	3.3V	From USB Hub (U9)
S75	USB2_SSRX-	USB3DN_RXDM3	DI/O	3.3V	From USB Hub (U9)
S76	PCIE_B_RST#	NA	-	NA	
S77	PCIE_C_RST#	NA	-	NA	
S78	PCIE_C_RX+ / SERDES_1_RX+	NA	-	NA	
S79	PCIE_C_RX- / SERDES_1_RX-	NA	-	NA	
S80	GND	NA	-	NA	
S81	PCIE_C_TX+ / SERDES_1_TX+	NA	-	NA	
S82	PCIE_C_TX- / SERDES_1_TX-	NA	-	NA	
S83	GND	NA	-	NA	
S84	PCIE_B_REFCK+	NA	-	NA	
S85	PCIE_B_REFCK-	NA	-	NA	

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S86	GND	NA	-	NA	
S87	PCIE_B_RX+	NA	-	NA	
S88	PCIE_B_RX-	NA	-	NA	
S89	GND	NA	-	NA	
S90	PCIE_B_TX+	NA	-	NA	
S91	PCIE_B_TX-	NA	-	NA	
S92	GND	NA	-	NA	
S93	DP0_LANE0+	DP_LN0_TXP	AIO	1.2V	
S94	DP0_LANE0-	DP_LN0_TXN	AIO	1.2V	
S95	DP0_AUX_SEL	**GPIO**: GPIO150 **DPI**: DPI_CK **GBE**: GBE_AUX_PPS1 **I2S**: I2SO1_D0 **CAM**: CMVREF3 **SPDIF**: SPDIF_IN2 **UART**: URXD3	DI	1.8V	
S96	DP0_LANE1+	DP_LN1_TXP	AIO	1.2V	
S97	DP0_LANE1-	DP_LN1_TXN	AIO	1.2V	
S98	DP0_HPD	**GPIO**: GPIO46 **DP**: DP_TX_HPD **PWM**: PWM_0 **USB**: VBUSVALID_2P	DI	1.8V	
S99	DP0_LANE2+	DP_LN2_TXP	AIO	1.2V	
S100	DP0_LANE2-	DP_LN2_TXN	AIO	1.2V	
S101	GND	NA	-	NA	
S102	DP0_LANE3+	DP_LN3_TXP	AIO	1.2V	
S103	DP0_LANE3-	DP_LN3_TXN	AIO	1.2V	
S104	USB3_OTG_ID	NA	-	NA	
S105	DP0_AUX+	DPAUXP	AIO	1.2V	
S106	DP0_AUX-	DPAUXN	AIO	1.2V	
S107	LCD1_BKLT_EN	**GPIO**: GPIO15 **GPIO**: TP_GPIO7_AO **SPI**: SPIM4_MISO **HDMI**: HDMITX20_SDA	DI/O	1.8V	
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	EDPAUXP	DO	1.8V	DSI1_CKP_T1B (BOM change)
S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	EDPAUXN	DO	1.8V	DSI1_CKN_T1C (BOM change)
S110	GND	NA	-	NA	
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	EDP_LN0_TXP	DO	1.8V	DSI1_D0P_T0C (BOM change)
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	EDP_LN0_TXN	DO	1.8V	DSI1_D0N_T1A (BOM change)
S113	eDP1_HPD / DSI1_TE	**GPIO**: GPIO26 **DSI**: DSI_TE **DSI**: DSI1_TE **EDP**: EDP_TX_HPD	DI	1.8V	

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S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	EDP_LN1_TXP	DO	1.8V	DSI1_D1P_T2A (BOM change)
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	EDP_LN1_TXN	DO	1.8V	DSI1_D1N_T2B (BOM change)
S116	LCD1_VDD_EN	**GPIO**: GPIO28 **DSI**: DSI1_TE **DSI**: DSI_TE **EDP**: EDP_TX_HPD **CAM**: CMVREF3 **PWM**: PWM_3	DI/O	1.8V	
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	NA	DO	1.8V	DSI1_D2P_T0A (BOM change)
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	NA	DO	1.8V	DSI1_D2N_T0B (BOM change)
S119	GND	NA	-	NA	
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	NA	DO	1.8V	DSI1_D3P_T2C (BOM change)
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	NA	DO	1.8V	DSI1_D3N (BOM change)
S122	LCD1_BKLT_PWM	**GPIO**: GPIO30 **DISP**: DISP_PWM1 **DISP**: DISP_PWM0 **CAM**: CMFLASH3 **PWM**: PWM_1	DO	1.8V	
S123	GPIO13	**GPIO**: GPIO5 **GPIO**: TP_GPIO5_AO **SPDIF**: SPDIF_IN1 **I2S**: I2SO1_BCK **DMIC**: DMIC4_DAT_R **I2S**: I2SIN_D2 **I2S**: I2SO2_D2	DI/O	1.8V	
S124	GND	NA	-	NA	
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	DSI0_D0P_T0C	DO	1.8V	
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	DSI0_D0N_T1A	DO	1.8V	
S127	LCD0_BKLT_EN	**GPIO**: GPIO146 **DPI**: DPI_D15 **GBE**: GBE_RXER **CAM**: CMFLASH1 **SPI**: SPIM3_MISO **GBE**: GBE_AUX_PPS3	DO	1.8V	
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	DSI0_D1P_T2A	DO	1.8V	
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	DSI0_D1N_T2B	DO	1.8V	

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S130	GND	NA	-	NA	
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	DSI0_D2P_T0A	DO	1.8V	
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	DSI0_D2N_T0B	DO	1.8V	
S133	LCD0_VDD_EN	**GPIO**: GPIO25 **LCM**: LCM_RST **LCM**: LCM1_RST **DP**: DP_TX_HPD	DO	1.8V	
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	DSI0_CKP_T1B	DO	1.8V	
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	DSI0_CKN_T1C	DO	1.8V	
S136	GND	NA	-	NA	
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	DSI0_D3P_T2C	DO	1.8V	
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	DSI0_D3N	DO	1.8V	
S139	I2C_LCD_CK	NA	-	NA	
S140	I2C_LCD_DAT	NA	-	NA	
S141	LCD0_BKLT_PWM	**GPIO**: GPIO29 **DISP**: DISP_PWM0 **DISP**: DISP_PWM1	DI/O	1.8V	
S142	GPIO12	**GPIO**: GPIO42 **KP**: KPCOL0	DI/O	1.8V	
S143	GND	NA	-	NA	
S144	eDP0_HPD / DSI0_TE	**GPIO**: GPIO19 **GPIO**: TP_GPIO3_AO **CAM**: CMFLASH1 **CAM**: CMVREF5 **TDMIN**: TDMIN_BCK **UART**: URXD1 **UART**: TP_URXD1_AO	DI/O	1.8V	
S145	WDT_TIME_OUT#	**GPIO**: GPIO100 **WDOG**: WATCHDOG	DO	1.8V	
S146	PCIE_WAKE#	**GPIO**: GPIO47 **PCI**: WAKEN	DI	3.3V	
S147	VDD_RTC	VRTC28	A	1.8V	From MT6365 (U200)
S148	LID#	**GPIO**: GPIO65 **I2C**: SCL5 **I2C**: SCP_SCL0 **I2C**: SCP_SCL1	DI	1.8 - 5V	
S149	SLEEP#	**GPIO**: GPIO66 **I2C**: SDA5 **I2C**: SCP_SDA0 **I2C**: SCP_SDA1	DI	1.8 - 5V	

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S150	VIN_PWR_BAD#	**GPIO**: GPIO86 **USB**: IDDIG_1P **UART**: UTXD1 **UART**: URTS2 **PWM**: PWM_2 **GPIO**: TP_GPIO4_AO **AUXIF**: AUXIF_ST0	DI	VDD_IN	
S151	CHARGING#	**GPIO**: GPIO88 **USB**: VBUSVALID_1P **UART**: UTXD2 **UART**: URTS1 **CLK**: CLKM2 **GPIO**: TP_GPIO6_AO **AUXIF**: AUXIF_ST1	DI	1.8 - 5V	
S152	CHARGER_PRSNT#	**GPIO**: GPIO129 **DMIC**: DMIC2_DAT **SPI**: SPINOR_IO2 **SPDIF**: SPDIF_IN1 **TCSYS**: LVTS_SCK	DI	1.8 - 5V	
S153	CARRIER_STBY#	**GPIO**: GPIO128 **DMIC**: DMIC2_CLK **SPI**: SPINOR_IO1 **TDMIN**: TDMIN_DI **TCSYS**: LVTS_SCF	DO	1.8V	
S154	CARRIER_PWR_ON	**GPIO**: GPIO127 **DMIC**: DMIC1_DAT_R **SPI**: SPINOR_IO0 **TDMIN**: TDMIN_LRCK **TCSYS**: LVTS_26M	DO	1.8V	
S155	FORCE_RECOV#	**GPIO**: GPIO126 **DMIC**: DMIC1_DAT **SPI**: SPINOR_CS **TDMIN**: TDMIN_BCK **TCSYS**: LVTS_SDO	DI	1.8V	
S156	BATLOW#	**GPIO**: GPIO125 **DMIC**: DMIC1_CLK **SPI**: SPINOR_CK **TDMIN**: TDMIN_MCK **TCSYS**: LVTS_FOUT	DI	1.8 - 5V	
S157	TEST#	**GPIO**: GPIO149 **DPI**: DPI_DE **GBE**: GBE_AUX_PPS0 **I2S**: I2SO1_WS **CAM**: CMVREF2 **SPDIF**: SPDIF_IN1 **UART**: UTXD3	DI	1.8 - 5V	
S158	GND	NA	-	NA	

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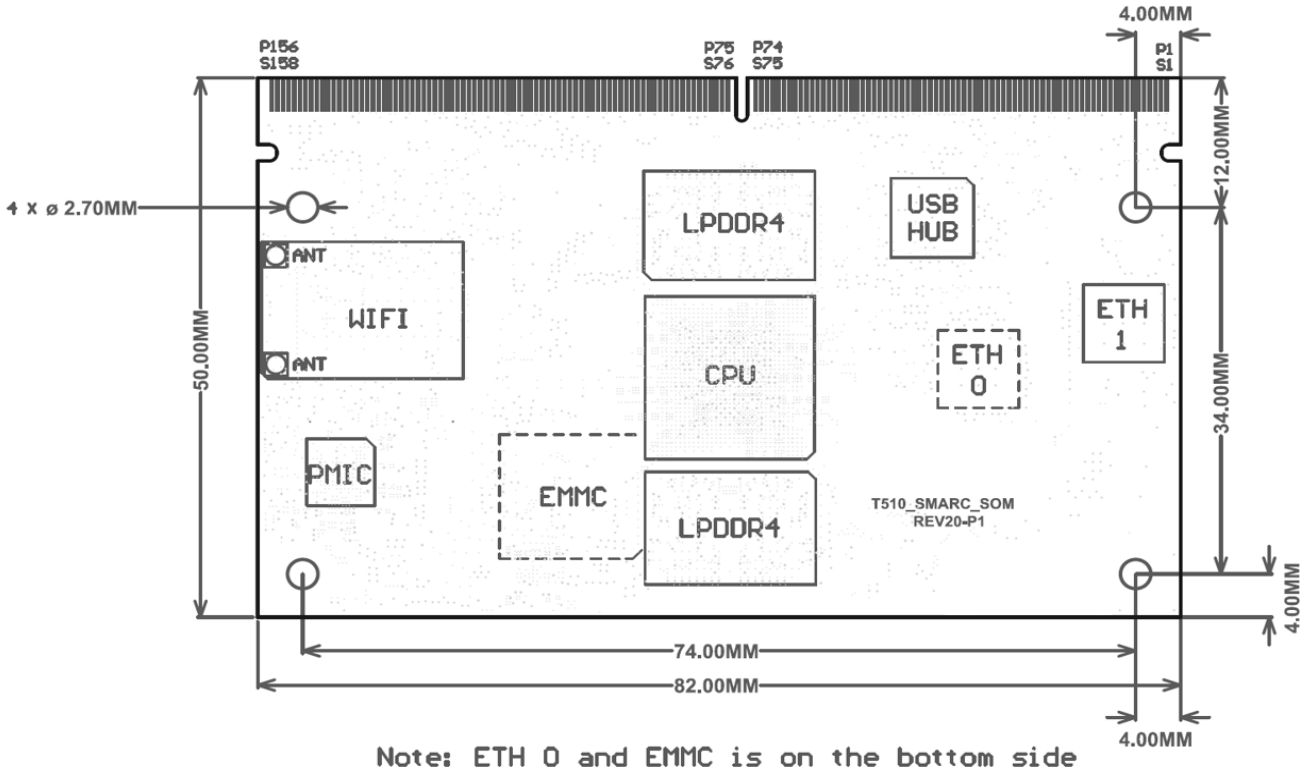
8 Mechanical and PCB footprint specification

The Tungsten510 SMARC module dimensions are 82 x 50 mm. Detail drawings are shown below.



Note: ETH 0 and EMMC is on the bottom side

9 Storage instructions

Required Storage Conditions:

- **Prior to Opening the Dry Packing**
  The following are required storage conditions prior to opening the dry packing:
  - Normal temperature: 5~40℃
  - Normal humidity: 80% (Relative humidity) or less
  - Storage period: One year or less

10 Ordering Information

Order Model	Description
T510_SMARC_SOM_4r16eWB	SMARC SOM: MT8370 / 4GB / 16GB eMMC / Sona MT320
T510_SMARC_SOM_8r16eWB	SMARC SOM: MT8370 / 8GB / 16GB eMMC / Sona MT320 (MOQ requirements)
SMARC_CAR	Kit - Universal SMARC Carrier Board. Includes 3x EFB2471A3S-10MH4L and 2x 001-0021 antennas, power supply, DB9 cable
SMARC_CAR_BRD	Universal Carrier Board - SMARC (Note - SOM sold separately)

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11 Reliability Test

11.1 Dynamic Reliability Test

Table 8: Dynamic Reliability Test Results for Tungsten510 Modules

Test Item	Specification	Standard	Test Result
Vibration Non-Operating Unpackaged device	Vibration Wave Form: Sine Waveform Vibration frequency / Displacement: 20-80 Hz/1.5mm Vibration frequency / Acceleration: 80-2000 Hz/20g Cycle Time: 4 min/cycle Number of Cycles: 4 cycle/axis Vibration Axes: X, Y and Z (Rotate each axis on vertical vibration table)	JEDEC 22-B103B (2016)	Pass
Mechanical Shock Non-Operating Unpackaged device	Pulse shape: Half-sine waveform Impact acceleration: 1500 g Pulse duration: 0.5 ms Number of shocks: 30 shocks (5 shocks for each face) Orientation: Bottom, top, left, right, front, and rear faces	JEDEC 22-B110B.01 (2019)	Pass

12 Regulatory

Radio certifications for SOMs with wireless options are held under the specific wireless module listings:

Order Model with Wireless	Module Product Page	RIG
T510_SMARC_SOM_4r16eWB	Sona MT320	Sona MT320 Regulatory information (Coming Soon)
T510_SMARC_SOM_8r16eWB	Sona MT320	Sona MT320 Regulatory information (Coming Soon)

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13 Additional Information

Please contact your local sales representative or our support team for further assistance:

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