AS0149AT

Product Preview

1/4-Inch CMOS Digital Image SOC

ON Semiconductor®

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Table 1. KEY PARAMETERS

Parameter		Value
Optical Format		1/4”
Pixel Size and Type		3.0 μm x 3.0 μm
Maximum Resolution		1312 x 992 (1.3 Mp)
Input Clock Range		10−30 MHz
Output Pixel Clock maximum		100 MHz at 2 clock per pixel
Frame Rate		30 fps (at 1280 x 960, not full resolution)
Color Filter Array		RGB Bayer
Shutter Type		Electronic Rolling Shutter
Output Interface		2−lane MIPI CSI−2, Parallel
Output Data Formats		RGB888, RGB565, YUV422(8b, 10b, BT.656, BT.601) Raw Data Bypass Modes: 20b HDR 16b HDR companded 14b HDR companded 12b companded (or 12b SDR)
Supply Voltage	VDDIO	1.8 or 2.8 V Nominal
	VAA	2.8 V Nominal
	VAA_PIX	2.8 V Nominal
	VDD_PHY	1.2 or 2.8 V Nominal
	VDD	1.2 V Nominal
Package		8 mm x 9 mm, 89 pin iBGA
Temperature		Operating Temperature −40°C to 105°C (ambient) Operating Temperature −40°C to 125°C (junction)
Power consumption		< 320 mW typical

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

Features

- Combined HDR RAW Output, up to 20−bit (>120 dB)
- Support for full−resolution 120 dB HDR+LFM
- New High−Performance 3.0 μm BSI Pixel, with Super−Exposure HDR+LFM Mode
- Advanced HDR Image Combination with Flexible Exposure Ratio Control
- RAW bypass capability
- Color and gamma correction
- Auto exposure, auto white balance, distortion correction and overlays
- Adaptive Local Tone Mapping (ALTM)
- Two−wire serial programming interface (CCIS)
- Output formats RGB888, RGB565, YUV422(8/10 bit (2 clock per pixel), BT.656, BT.601)
- Real−time Functional Safety Mechanisms and Fault Detection (Not ASIL B standalone)
- Up to 6 GPIO
- Spacial Transform Endine (STE) and overlay support
- Data Interfaces: 2−lane MIPI CSI−2, Parallel
- Selectable Automatic or User Controlled Black level control
- Multi−Camera Synchronization Support
- AEC−Q100 Grade 2

Applications

- Rear View Camera (RVC)
- Surround View Camera (SVC)
- Camera Mirror Replacement System (CMS)

Table 2. ORDERING INFORMATION

Part Number	Product Description	Orderable Product Attribute Description
AS0149ATSC00XUEA0−DPBR−E	Sample, 8x9 iBGA	Dry pack with PF
AS0149ATSC00XUEA0−DRBR−E	Sample, 8x9 iBGA	Dry pack without PF

GENERAL DESCRIPTION

ON Semiconductor AS0149AT is a 1/4 − inch, single−chip CMOS digital image sensor SOC. It captures high−quality color images with a 1312 H x 992 V active−pixel array, and outputs formats with RGB888, YUV422, BT.656 or BT.601.

This advanced automotive sensor captures images in either linear, or high dynamic range, with rolling−shutter readout. AS0149AT is optimized for both low light and challenging high dynamic range scene performance, with a 3μm BSI pixel and on−sensor up to 120 dB HDR capture capability. The sensor includes flexible functions such as windowing, and both video and single frame modes. The device is programmable through a simple two−wire serial interface, and supports both MIPI CSI−2 and Parallel output interfaces.

The AS0149 is a complete camera−on−a−chip, it performs sophisticated processing functions including color and gamma correction, auto white balance, distortion correction, overlays, ALTM (Adaptive Local Tone Mapping),and supports Super−Exposure HDR+LFM mode.

FUNCTIONAL OVERVIEW

Figure 1 shows the typical configuration of the AS0149AT in a camera system. On the host side, a two−wire serial interface is used to control the operation of the AS0149AT, and image data is transferred using the parallel or MIPI interface between the AS0149A Tand the host.

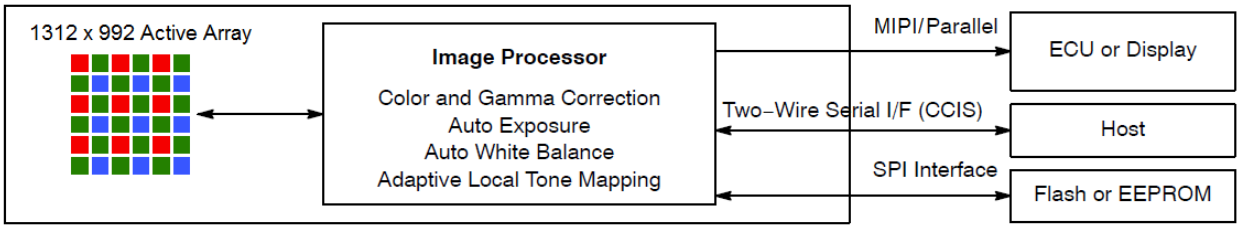
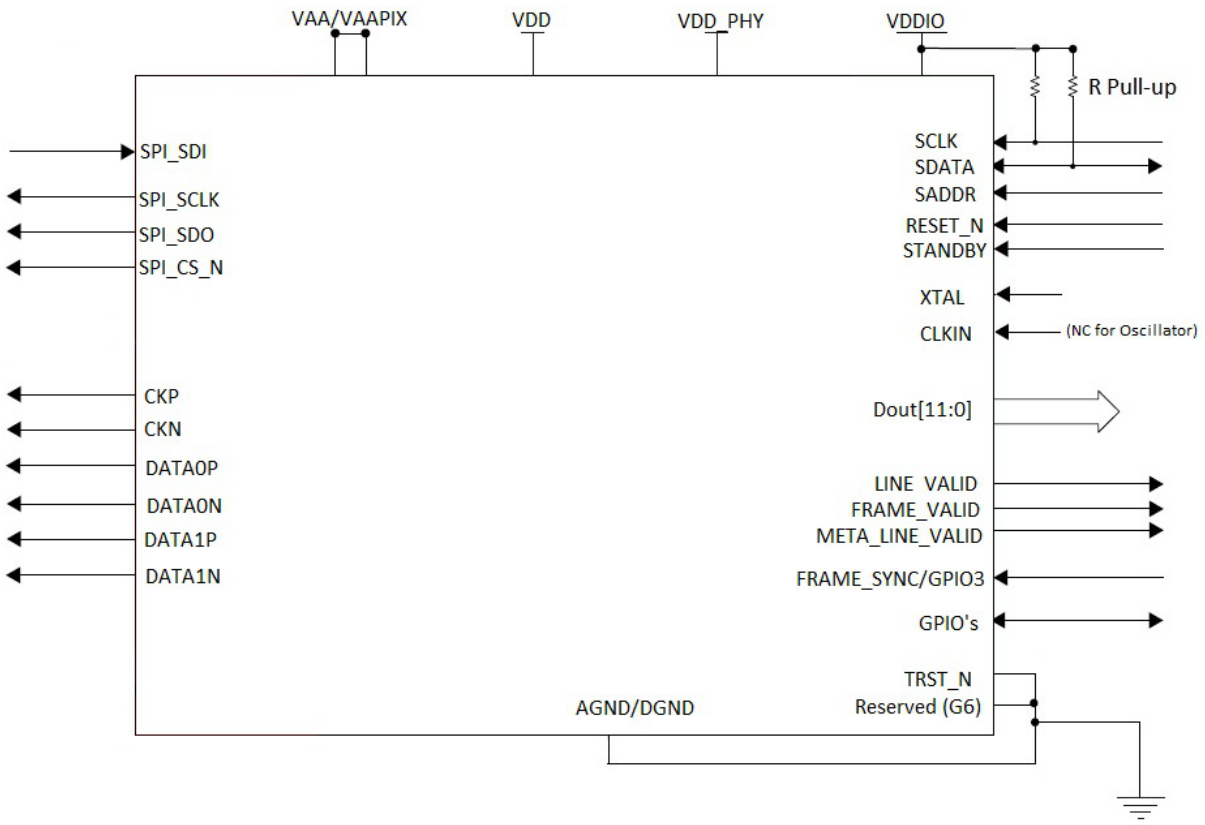


Figure 1. AS0149AT Connectivity

SYSTEM INTERFACES

All power supply rails must be decoupled from ground using capacitors as close as possible to the package. Table 3 provides pin descriptions for the AS0149AT.



1. This typical configuration shows only one scenario out of multiple possible variations for this device.
2. ON Semiconductor recommends a 1.5 k resistor value for the two−wire serial interface RPULL−UP; however, greater values may be used for slower transmission speed.
3. ON Semiconductor recommends that 0.01, 0.1, 1 and 10 uF decoupling capacitors for each power supply are mounted as close as possible to the pin. Actual values and numbers may vary depending on lay−out and design consideration.

Figure 2. Typical Configuration

Table 3. PIN DESCRIPTION

Pin Number	Pin Name	Type	Description
CLOCK AND RESET			
G3	CLKIN	Input	If XTAL is connected to one pin of a crystal, this signal is connected to the other pin, otherwise this signal should be left unconnected.
G7	STANDBY	Input	Standby mode control, active HIGH
G8	RESET_N	Input	Master reset signal, active LOW. There is no pullup on the RESET_N pin, so must be actively driven high or low to the VDDIO level
G6	Reserved	Input	This signal should be connected to GND.
G2	XTAL	Input	Master Input Clock. Nominally 27MHz. This can either be a square−wave generated from an oscillator (in which case the CLKIN input must be left unconnected) or direct connection to a crystal.
REGISTER INTERFACE			
D8	SCLK	Input	SCLK: Two−wire Serial Interface Clock (Host Interface)

Table 3. PIN DESCRIPTION

Pin Number	Pin Name	Type	Description
REGISTER INTERFACE			
C7	SDATA	I/O	Two−wire Serial Interface Data (Host Interface)
B5	SADDR	Input	Selects device address for the two−wire slave serial interface. When connected to GND the device ID is 0x90. When wired to VDDIO, a device ID of 0xBA is selected.
SPI INTERFACE			
H2	SPI_CLK	Output	Clock Output for Interfacing to an External SPI Flash or EEPROM Memory
C4	SPI_SDI	Input	Data in from SPI flash or EEPROM memory. When no SPI device is fitted, this signal can be left unconnected. This signal has an internal pull−up resistor.
B4	SPI_SDO	Output	Data Out to SPI Flash or EEPROM Memory
C3	SPI_CS_N	Output	Chip Select Out to SPI Flash or EEPROM Memory
OUTPUT INTERFACES			
J7	META_LINE_VALID	Output	Line valid signal to indicate when Metadata is valid. In addition, there is an option to allow META_LINE_VALID to be reflected in LV_OUT.
H6	FRAME_VALID	Output	Frame valid output (synchronous to PIXCLK)
J6	LINE_VALID	Output	Line valid output (synchronous to PIXCLK)
H4	PIXCLK	Output	Pixel clock output
J2	DOUT0	Output	Pixel data output
J3	DOUT1	Output	
H3	DOUT2	Output	
D4	DOUT3	Output	
E4	DOUT4	Output	
F4	DOUT5	Output	
G4	DOUT6	Output	
J4	DOUT7	Output	
J5	DOUT8	Output	
G5	DOUT9	Output	
F5	DOUT10	Output	
F6	DOUT11	Output	
E2	CKP	Output	Differential MIPI clock
E1	CKN	Output	Differential MIPI clock
F2	DATA0P	Output	Differential MIPI data lane 0
F1	DATA0N	Output	Differential MIPI data lane 0
D2	DATA1P	Output	Differential MIPI data lane 1
D1	DATA1N	Output	Differential MIPI data lane 1
GPIO			
H8	GPIO_0	I/O	General purpose digital I/O. The GPIO configured as inputs may be tied high or low through resistor to VDDIO or GND, but not connected directly to VDDIO nor GND. GPIO configured as outputs may be left as floating.
E6	GPIO_1	I/O	General purpose digital I/O
E7	GPIO_2	I/O	General purpose digital I/O

Table 3. PIN DESCRIPTION

Pin Number	Pin Name	Type	Description
GPIO			
D5	FRAME_SYNC/ GPIO_3	I/O	FRAME_SYNC is used to synchronize to external sources or multiple cameras together. Comes up as FRAME_SYNC Input by default Can be configured as GPIO3 General purpose digital I/O
D6	GPIO_4	I/O	General purpose digital I/O
D7	GPIO_5	I/O	General purpose digital I/O
POWER			
A2, A4, A9, D3, E5, E9, F3, G1, H5, H9, K1, K4, K6, K9	DGND	Supply	Digital ground
B3, B8, C8	AGND	Supply	Analog ground
A3, A8, D9, G9, J1, K2, K5, K8	VDDIO	Supply	I/O supply power (1.8V or 2.8V)
B1, B9, C9	VAA	Supply	Analog power (2.8V)
B2	VAA_PIX	Supply	Analog power for pixel array (2.8V)
C2	VDD_SLVS_PH Y	Supply	Do not connect. Manufacturing test access only
E3	VDD_PHY	Supply	Digital PHY power (1.2V). Can be 2.8V with minimal power impact
A5, C1 , F9, H1, J9, K3, K7	VDD	Supply	Digital power (1.2V)
SPECIAL PINS			
A7	ATEST1	Output	Do not connect. Manufacturing test access only.
A6	ATEST2	Output	Do not connect. Manufacturing test access only.
B7	ATEST3	Output	Do not connect. Manufacturing test access only.
B6	ATEST4	Output	Do not connect. Manufacturing test access only.
F8	TDO	Output	JTAG Test pin (Reserved for Test Mode)
E8	TDI	Input	JTAG Test pin (Reserved for Test Mode)
C6	TMS	Input	JTAG Test pin (Reserved for Test Mode)
C5	TCK	Input	JTAG Test pin (Reserved for Test Mode)
J8	TRST_N	Input	Connect to GND.
F7	SYS_CHECK	Output	Fault Pin. Combined OR of error flags. Leave unconnected if not used.
H7	TEMP_FLAG	Output	Serial temperature code output

Table 4. RESET/DEFAULT STATE OF INTERFACES

	Hardware States		Firmware States				
AS0149	Reset State	Default State	Hard Standby	Soft Standby	Streaming	Idle	Notes
XTAL	(clock running or stopped)	(clock running)	(clock running or stopped)	(clock running)	(clock running)	(clock running)	Input
CLKIN	n/a	n/a	n/a	n/a	n/a	n/a	Input
RESET_N	(asserted)	(negated)	(negated)	(negated)	(negated)	(negated)	Input
SCLK	n/a	n/a	(clock running or stopped)	(clock running or stopped)	(clock running or stopped)	(clock running or stopped)	Input. Must always be driven to a valid logic level
SDATA	high−impedance	high−impedance	high−impedance	high−impedance			Input/Output. A valid logic level should be established by pull−up

Table 4. RESET/DEFAULT STATE OF INTERFACES

AS0149	Hardware States		Firmware States				Notes
	Reset State	Default State	Hard Standby	Soft Standby	Streaming	Idle	
SADDR0	n/a	n/a	n/a	n/a	n/a	n/a	Input. Must always be driven to a valid logic level
FRAME_SYNC	n/a	n/a	n/a	n/a	n/a	n/a	Input. Must always be driven to a valid logic level
STANDBY	n/a	(negated)	(asserted)	(negated)	(negated)	(negated)	Input. Must always be driven to a valid logic level
SPI_SCLK	high−impedance	driven, logic 0	driven, logic 0	driven, logic 0			Output
SPI_SDI	internal pull−up enabled	internal pull−up enabled	internal pull−up enabled	internal pull−up enabled			Input. Internal pull−up permanently enabled.
SPI_SDO	high−impedance	driven, logic 0	driven, logic 0	driven, logic 0			Output
SPI_CS_N	high−impedance	driven, logic 1	driven, logic 1	driven, logic 1			Output
GPIO5	high−impedance	high−impedance	Driven if used	Driven if used	Driven if used	Driven if used	Input/Output. After reset these pins are high impedance.
GPIO4	high−impedance	high−impedance	Driven if used	Driven if used	Driven if used	Driven if used	
GPIO3	high−impedance	high−impedance	Driven if used	Driven if used	Driven if used	Driven if used	
GPIO2	high−impedance	high−impedance	Driven if used	Driven if used	Driven if used	Driven if used	
GPIO1	high−impedance	high−impedance	Driven if used	Driven if used	Driven if used	Driven if used	Input/Output. After reset these pins are high impedance.
GPIO0	high−impedance	high−impedance	Driven if used	Driven if used	Driven if used	Driven if used	Input/Output. After reset these pins are high impedance.
TRST_N	n/a	n/a	(negated)	(negated)	(negated)	(negated)	Input. Must always be driven to a valid logic level. Tied to GND for normal operation.
TCK	high−impedance	high−impedance	high−impedance	high−impedance	n/a	n/a	
TMS	high−impedance	high−impedance	high−impedance	high−impedance	n/a	n/a	
TDI	high−impedance	high−impedance	high−impedance	high−impedance	n/a	n/a	
TDO	high−impedance	high−impedance	high−impedance	high−impedance	n/a	n/a	
MIPI_OUT_CLKP	driven, logic 0	driven, logic 0	driven, logic 0	driven, logic 0	driven, logic 0	driven, logic 0	
MIPI_OUT_CLKN							
MIPI_OUT_0P							
MIPI_OUT_0N							
MIPI_OUT_1P							
MIPI_OUT_1N							
META_LINE_VALID	high−impedance	driven, logic 0	driven, logic 0	driven, logic 0	driven (video data)	driven, logic 0	
FRAME_VALID							
LINE_VALID							
PIXCLK							
DOUT0							
DOUT1							
DOUT2							
DOUT3							
DOUT4							
DOUT5							
DOUT6							
DOUT7							
DOUT8							
DOUT9							
DOUT10							
DOUT11							

Table 5. AS0149 8 mm x 9mm iBGA PACKAGE PINOUT

	1	2	3	4	5	6	7	8	9
A		DGND	VDDIO	DGND	VDD	ATEST2	ATEST1	VDDIO	DGND
B	VAA	VAA_PIX	AGND	SPI_SDO	SADDR0	ATEST4	ATEST3	AGND	VAA
C	VDD	VDD_SLVS_ PHY	SPI_CS_N	SPI_SDI	TCK	TMS	SDATA	AGND	VAA
D	DATA1N	DATA1P	DGND	DOUT3	FRAME_ SYNC, GPIO_3	GPIO_4	GPIO_5	SCLK	VDDIO
E	CLKN	CLKP	VDD_PHY	DOUT4	DGND	GPIO_1	GPIO_2	TDI	DGND
F	DATA0N	DATA0P	DGND	DOUT5	DOUT10	DOUT11	SYS_CHECK	TDO	VDD
G	DGND	XTAL	CLKIN	DOUT6	DOUT9	Reserved	STANDBY	RESET _N	VDDIO
H	VDD	SPI_CLK	DOUT2	PIXCLK	DGND	FRAME_ VALID	TEMP_FLAG	GPIO_0	DGND
J	VDDIO	DOUT0	DOUT1	DOUT7	DOUT8	LINE_VA LID	META_LINE_VA LID	TRST_ N	VDD
K	DGND	VDDIO	VDD	DGND	VDDIO	DGND	VDD	VDDIO	DGND

Table 6. OPERATING CURRENT CONSUMPTION, SUPER EXPOSURE T1+T2,

Current Type	Condition	Symbol	Voltage	Typ	Max	Unit
Analog Operating Current	Streaming, 1280x960, MIPI	I_{AA}	2.8	51	65	mA
Digital Operating Current	Streaming, 1280x960, MIPI	I_{DD}	1.2	109	130	mA
I/O Supply Current	Streaming, 1280x960, MIPI	I_{DD_I0}	1.8	0	1	mA
PHY Supply Current	Streaming, 1280x960, MIPI	I_{DD_PHY}	1.2	7	5	mA
Pixel Supply Current	Streaming, 1280x960, MIPI	I_{AA_PIX}	2.8	7	15	mA
SLVS Supply Current	Streaming, 1280x960, MIPI	$I_{DD\_SLVS\_PHY}$	1.2	0	0	mA

POWER UP SEQUENCE

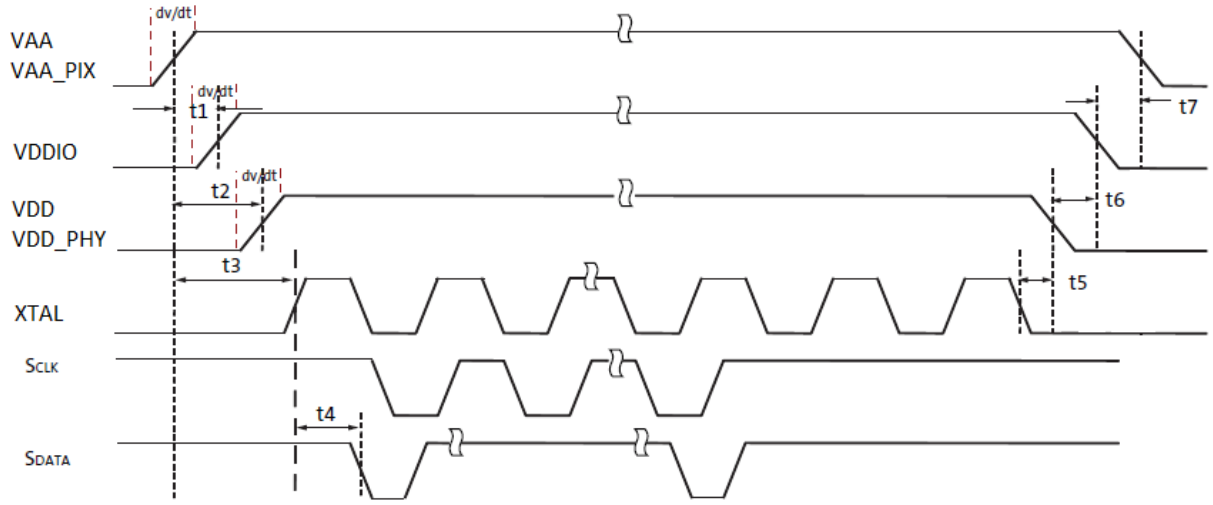


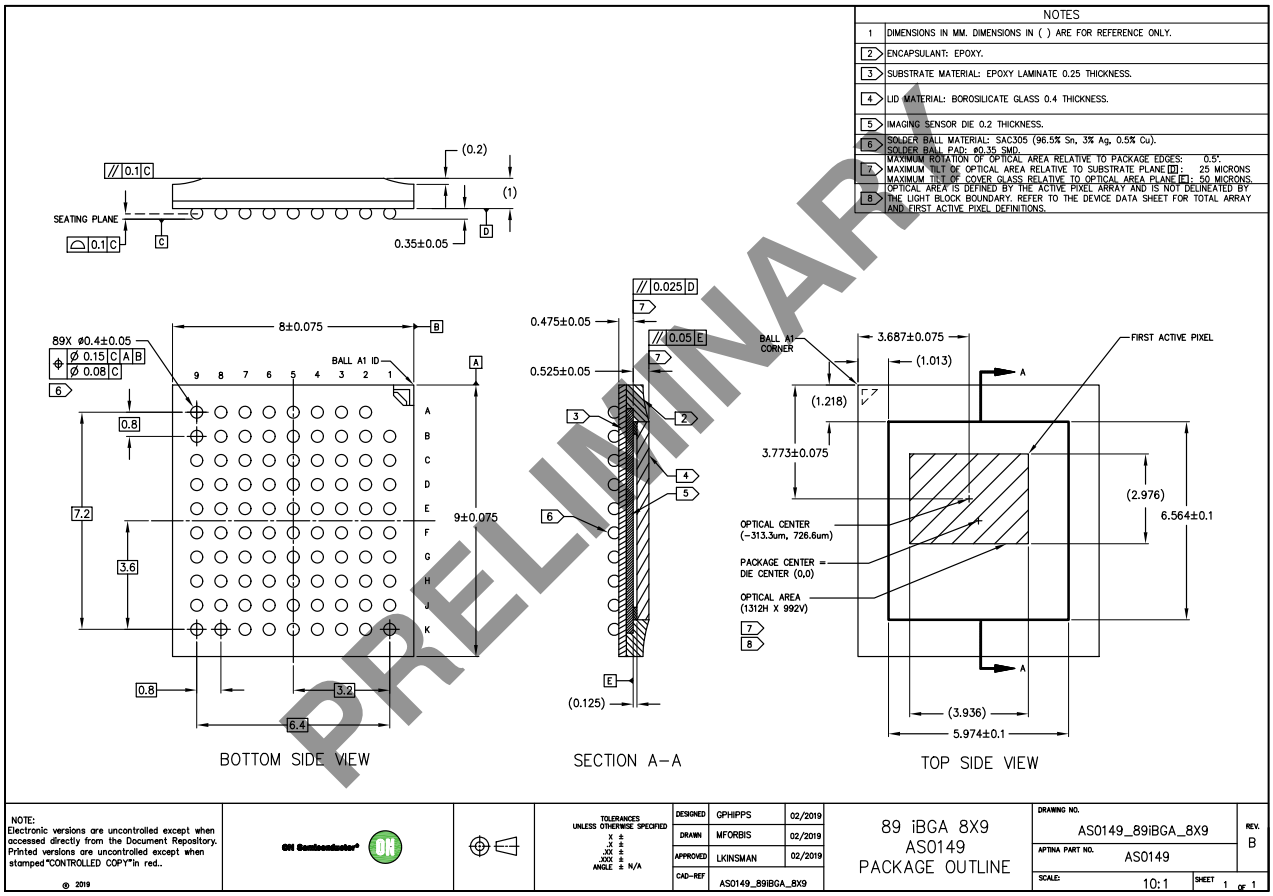
Figure 3.

Table 7.

Symbol	Parameter	Min	Typ	Max	Unit
t1	Delay from VAA to VDDIO	0			ms
t2	Delay from VDDIO to VDD/VDD_PHY	0			ms
t3	EXTCLK activation	T1 + t2			ms
t4	First serial command	100			EXTCLK cycles
t5	EXTCLK deactivation	0			ms
t6	Delay from VDD/VDD_PHY to VDDIO	0			ms
t7	Delay from VDDIO to VAA	0			ms

1. Note that all supplies can power up and down together

PACKAGE DIMENSIONS



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