1/1.8-Inch 8 Mp CMOS Digital Image Sensor

AR0822

General Description

The AR0822 is a stacked 1/1.8−inch BSI (back side illuminated) CMOS digital image sensor with an active−pixel array of 3840 (H) x 2160 (V). It captures images in either linear or high dynamic range modes with a rolling−shutter readout, and includes sophisticated camera functions such as binning, windowing and both video and single frame modes. It is designed for both low light and high dynamic range performance. AR0822 can combine on chip up to three exposures and compand to 12−bit HDR output or it could provide line interleaved output of two exposures to support off chip HDR in an ISP chip. It could also provide enhanced Dynamic Range from single exposure. The AR0822 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for security applications.

Table 1. KEY PARAMETERS

Parameter	Typical Value
Optical format	1/1.8 inch (8.81 mm diagonal)
Active pixels	3840(H) x 2160 (V)
Pixel size	2.0 μm x 2.0 μm, BSI
Color filter array	RGB Bayer
Chief ray angle (CRA)	10°
Shutter type	ERS and GRR
Input clock range	6 ~ 48 MHz
Serial bitrate range	350 Mbps ~ 2 Gbps per lane
Pixel clock range	164.25 MHz
Output Interface	4−lane MIPI−CSI2 (1−lane, 2−lane supported)
ADC resolution	12−bit, on die
Analog gain Analog gain range	0 ~ 24 dB (Linear) 0 ~ 18 dB (Li−HDR, eHDR)
Digital gain Digital gain range	24 ~ 44.625 dB (Linear) 18 ~ 44.625 dB (Li−HDR, eHDR) 0 ~ 5.625 dB (eDR)
Subsampling	bin2, bin4, skip2, skip4
Output format	Linear: 10 bit and 12 bit eHDR: 10, 12, 14, 16 and 20 bit
Frame rate	Linear: 4k @ 60 fps LI−HDR (2exp): 4k @ 30 fps eHDR (3exp): 4k @ 30 fps
Responsivity	18 ke−/lux*sec
SNRMAX	39 dB

1. θJA is dependent on the customer module design and should not be used for calculating junction temperature.

Features

- 4k (8 Mp) at 60 fps for excellent Video Performance
- Fast Full Resolution Video Capture of 3840 x 2160 at up to 30 fps in 3−exposure eHDR
- Advanced On−Sensor embedded High Dynamic Range (eHDR) Reconstruct with Flexible Exposure Ratio Control
- Motion detection, auto wake up from standby mode.
- enhanced Dynamic Range (eDR) mode to reach enhanced Dynamic Range yet no motion artifact from multiple exposures
  - eDR mode: enhanced Dynamic Range from single exposure.
- LI−eDR: T1−eDR + T2 output in line−interleaved mode
- Two exposure LI−HDR output
- Enhanced NIR response

Applications

- Security Camera
- IoT
- Car DVR

Table 1. KEY PARAMETERS

Parameter	Typical Value
Maximum dynamic range	Linear: 78 dB eHDR 3−exp: 120 dB
Supply voltage	I/O: 1.8 V (1.7V < V_{supply} < 1.9 V) or 2.7 V < V_{supply} < 2.9 V) Digital : 1.05 V (1.0 V < V_{supply} < 1.1 V) Analog: 2.8 V (2.7 V < V_{supply} < 2.9 V) MIPI: 1.05 V (1.0 V < V_{supply} < 1.1 V)
Power consumption (typical) The power consumption is estimated	Linear 30 fps: 223 mW 3−exp eHDR 30 fps: 540 mW
Operating Temperature Range (at junction) − T_J	−30°C to +85°C (Junction)
Optimal Performance Temperature Range (at junction) − T_J	0°C to +60°C (Junction)
Package options	mPBGA 14 x 9.5 mm θJA: 31°C/W (Note) θJB: 19°C/W

1. θJA is dependent on the customer module design and should not be used for calculating junction temperature.

Table 2. ORDER INFORMATION

Part Number Description	Orderable Product Attribute	Description
AR0822NPSC10SMTA0−DP	RGB, 10°CRA, mPBGA Packge	Dry Pack with Protective Film
AR0822NPSC10SMTA0−DR	RGB, 10°CRA, mPBGA package	Dry Pack without Protective Film
AR0822NPSC10SMTA0−DP−E	RGB, 10°CRA, mPBGA Packge	Dry Pack with Protective Film Engineering Sample
AR0822NPSM10SMTA0−DP	Mono, 10°CRA, mPBGA package	Dry Pack with Protective Film
AR0822NPSM10SMTA0−DR	Mono, 10°CRA, mPBGA package	Dry Pack without Protective Film
AR0822NPSM10SMTA0−DP−E	Mono, 10°CRA, mPBGA Packge	Dry Pack with Protective Film Engineering Sample
AR0822NPSC10SMTAH3−GEVB	RGB, 10°CRA	Demo3 Headboard
AR0822NPSM10SMTAH3−GEVB	Mono, 10°CRA	Demo3 Headboard

Table 3. 12−bit MODE OF OPERATION AND POWER

Mode Name	Mode Description	Resolution	Frame Rate
Native	4K Linear Full Res	3840 x 2160	60
Native	4K Linear Full Res, Lower Frame Rate	3840 x 2160	30
eHDR Native	4K eHDR 3exp Full Res	3840 x 2160	30
LI Native	4K LI−HDR 2exp	3840 x 2160	30
WoM bin4skip2 (Note 2)	Wake on Motion w/ Streaming	480 x 270	1
Bin2	2MP Linear	1920 x 1080	120
eDR Native (Note 3)	4K eDR	3840 x 2160	30
LI−eDR Native	4K LI−eDR	3840 x 2160	30

2. Actual resolution of sensor is 960 x 270 with every alternate col being dummy pixel output, active resolution is 480 x 270
3. eDR mode could go upto 45 fps

FUNCTIONAL OVERVIEW

AR0822 is a progressive−scan sensor that generates a stream of pixel data at a constant frame rate. It uses on−chip phase−locked loop (PLL) to generate all internal clocks form a single master input clock running between 6 and 48 MHz. The maximum data rate is 2 Gbps/lane for MIPI D−PHY. A block diagram of the sensor is shown in Figure 1. The AR0822 has a wide array of features to enhance functionality and increase versatility. A summary of features is found below.

- Operating Modes
  The AR0822 works in master and trigger modes. In master mode, the sensor generates the integration and readout timing. In trigger mode, it accepts an external trigger to start exposure, then generates the exposure and readout timing. The exposure time is programmed through the two−wire serial interface for both modes.
- Window Control
  Configurable window size and blanking times allow a wide range of resolutions and frame rates. Various analog and digital binning modes are supported, as are vertical and horizontal mirror operations.
- Context Switching
  Context switching may be used to rapidly switch between different readout modes, or to automatically cycle between different readout modes on a frame−by−frame basis or at a rate determined and controlled by the host. Refer to the AR0822 Developer Guide for details.
- Gain
  The AR0822 can be configured for a sensor gain up to 44.625 dB, 0.375 dB per step.
- MIPI
  The AR0822 image sensor supports 4−lane MIPI CSI−2 D−PHY
- PLL An on chip PLL provides reference clock flexibility
- Reset
  The AR0822 may be reset by a register write, or by a dedicated input pin.
- Temperature Sensor
- Motion Detection
- enhanced Dynamic Range (eDR) mode
- Test Pattern

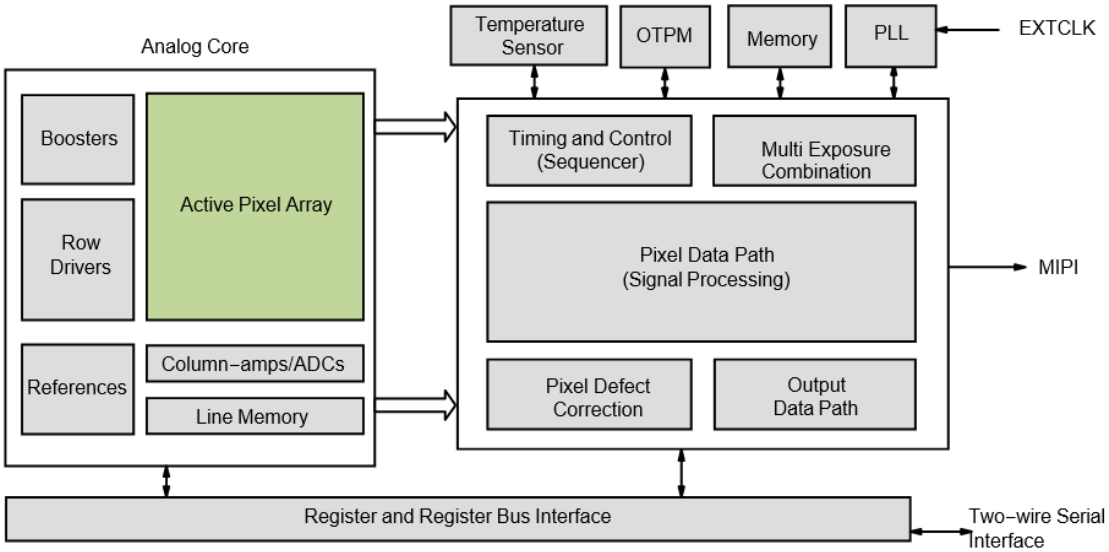


Figure 1. Block Diagram

PIXEL ARRAY

AR0822 sensor core uses a Bayer color pattern, as shown in Figure 2. The even−numbered rows contain green and red pixels; odd−numbered rows contain blue and green pixels. Even−numbered column contains green and blue pixels; odd−numbered columns contain red and green pixels.

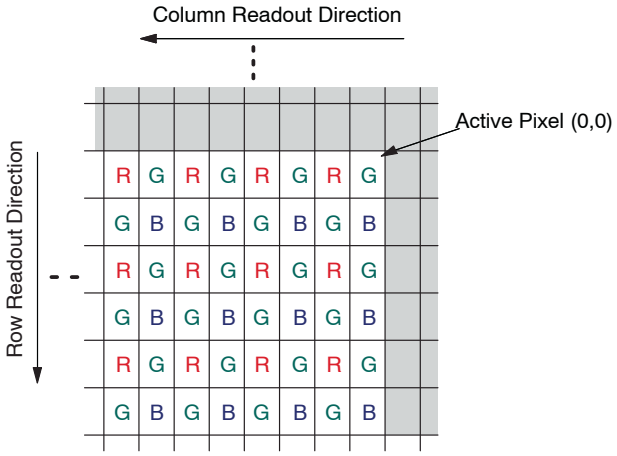


Figure 2. Pixel Color Pattern Detail (Top Right Corner) Bayer

Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 3). This reflects the actual layout of the array on the die.

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 3. When the image is read out of the sensor, it is presented one row at a time, with the rows and columns sequenced as shown in Figure 3.

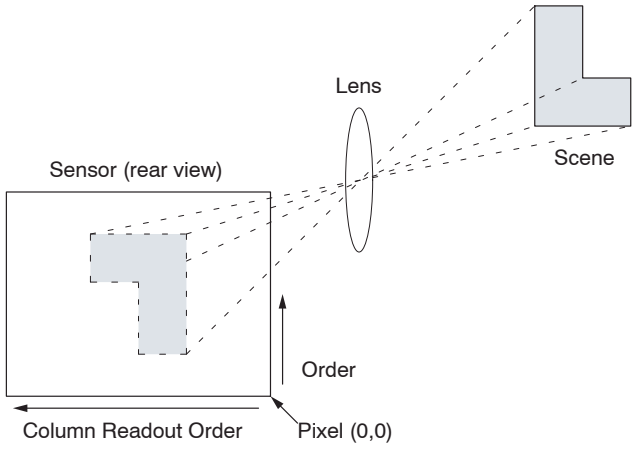


Figure 3. Imaging a Scene

TYPICAL CONNECTIONS

Figure 4 shows the typical AR0822 connections.

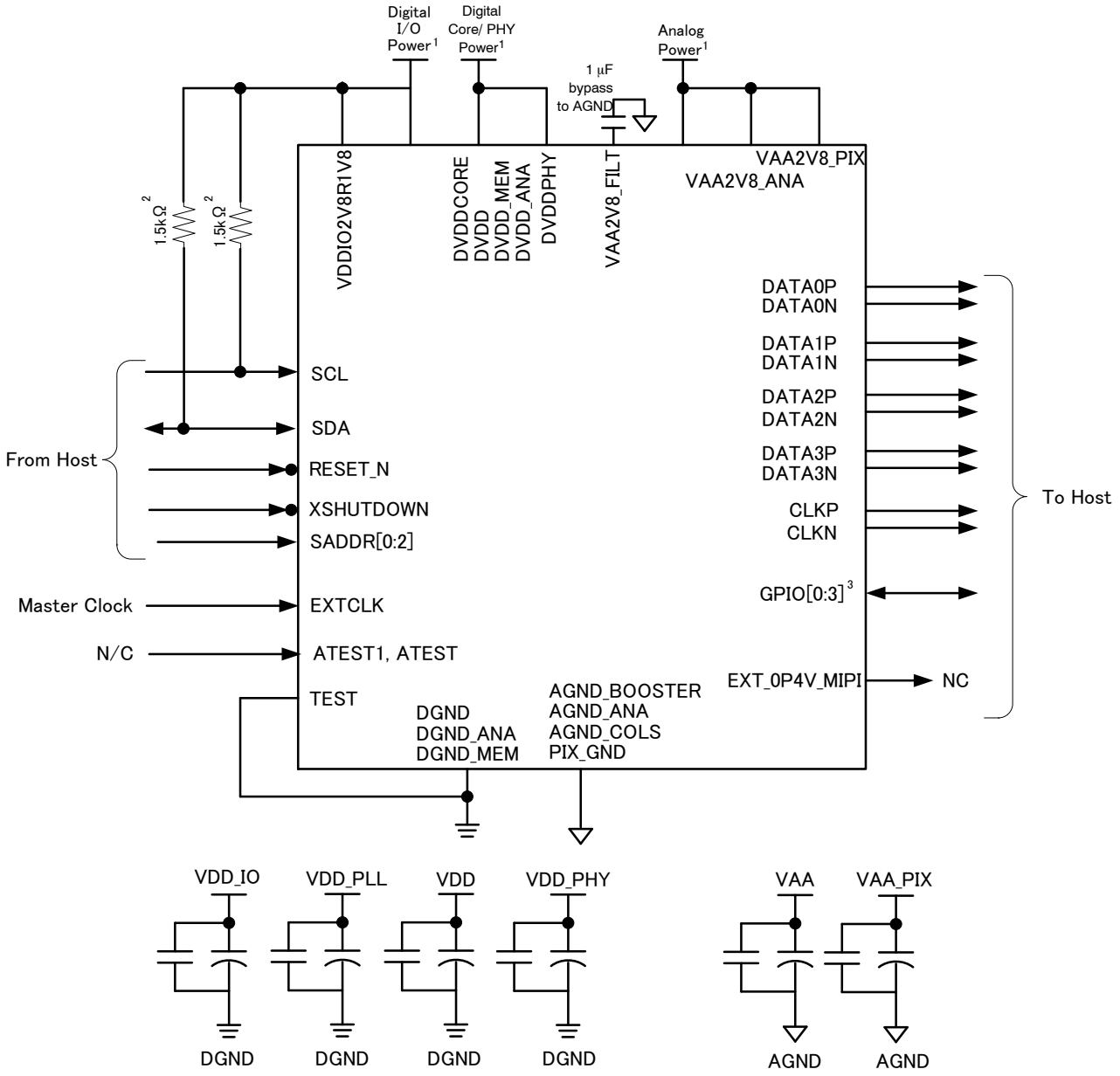


Figure 4. Typical Configuration, Four−Lane MIPI

NOTES:

1. All power supplies must be adequately decoupled.
2. **onsemi** recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two−wire speed.
3. GPIO[3:0] can be left unconnected if not used.
4. **onsemi** recommends that 0.1 µF and 10 µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on lay−out and design considerations. Refer to the AR0822 demo headboard schematics for circuit recommendations.
5. **onsemi** recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. I/O signals voltage must be configured to match VDD_IO voltage to minimize any leakage currents.
7. EXT_0P4V_MIPI can be connected to 0.4 V to use external voltage instead of the internal regulator supplied voltage. Register setting needs to be changed to use the external voltage instead of the internally supplied SLVS voltage.

PACKAGE BALL MAP (TOP VIEW) 75mPBGA_14X9.5													
	1	2	3	4	5	6	7	8	9	10	11	12	
A		VAA2V8_ANA	DATA3N	DATA2N	CLKN	DATA1N	DATA0N	DVDDPHY	DVDD	GPIO_1	GPIO_3	DVDD	A
B	AGND_BOOSTERS	EXT_0P4V_MIPI	DATA3P	DATA2P	CLKP	DATA1P	DATA0P	DVDDCORE	VDDIO2V8R1V8	GPIO_0	GPIO_2	VDDIO2V8R1V8	B
C	VAA2V8_PIX	ATEST2									SCL	SDA	C
D	VAA2V8_ANA	AGND_ANA		DGND	DGND	DGND	DGND	DGND	DGND		VDDIO2V8R1V8	DVDD	D
E	VDDIO2V8R1V8	AGND_BOOSTERS		DGND	DGND	DGND	DGND	DGND	DGND		DGND_MEM	DVDD_MEM	E
F	DVDD_MEM	VAA2V8_FILT									ATEST1	VAA2V8_ANA	F
G	VAA2V8_PIX	DVDD_ANA	PIXGND	DGND_ANA	XSHUTDOWN	EXTCLK	SADDR0	TEST	AGND_ANA	DGND_ANA	PIXGND	DVDD_ANA	G
H	DGND	VAA2V8_ANA	AGND_ANA	AGND_COLS	DGND_MEM	RESET_N	SADDR1	SADDR2	AGND_COLS	AGND_ANA	VAA2V8_PIX	VAA2V8_ANA	H
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 5. mPBGA Package Ball Assignment

Table 4. SIGNAL DESCRIPTIONS

Name	mPBGA pin	Type	Description
EXTCLK	G6	Input	Master Input Clock, 6−48 MHz.
RESET_N	H6	Input	Asynchronous active low resets. All settings are restored to factory default.
SCL	C11	Input	Two−Wire Serial clock input
SDA	C12	I/O	Two−Wire Serial data I/O
SADDR0	G7	Input	Two−Wire Serial address select (LSB)
SADDR1	H7	Input	Two−Wire Serial address select
SADDR2	H8	Input	Two−Wire Serial address select (MSB)
TEST	G8	Input	Manufacturing test enable pin (Tied to GND for normal operation)
GPIO_0	B10	I/O	General Purpose I/O
GPIO_1	A10	I/O	General Purpose I/O
GPIO_2	B11	I/O	General Purpose I/O
GPIO_3	A11	I/O	General Purpose I/O
DATA0P	B7	Output	MIPI serial data, lane 0, differential P
DATA0N	A7	Output	MIPI serial data, lane 0, differential N
DATA1P	B6	Output	MIPI serial data, lane 1, differential P
DATA1N	A6	Output	MIPI serial data, lane 1, differential N
DATA2P	B4	Output	MIPI serial data, lane 2, differential P
DATA2N	A4	Output	MIPI serial data, lane 2, differential N
DATA3P	B3	Output	MIPI serial data, lane 3, differential P
DATA3N	A3	Output	MIPI serial data, lane 3, differential N
CLKP	B5	Output	MIPI serial clock differential P
CLKN	A5	Output	MIPI serial clock differential N
DGND, DGND_ANA, DGND_MEM	D4, D5, D6, D7, D8, D9, E4, E5, E6, E7, E8, E9, E11, G4, G10, H1, H5	Supply	Digital Ground.

Table 4. SIGNAL DESCRIPTIONS

Name	mPBGA pin	Type	Description
DVDD DVDD_MEM, DVDD_ANA	A9, A12, D12, E12, F1, G2, G12	Supply	Digital power, 1.05 V nominal
VDDIO2V8R1V8	B9, B12, D11, E1	Supply	Digital I/O power, 1.8 V nominal
AGND_BOOSTER, AGND_ANA, AGND_COLS, PIX_GND	B1, D2, E2, G9, H3, H4, H9, H10 G3, G11	Supply	Analog Ground.
VAA2V8_ANA	A2, D1, F12, H2, H12	Supply	Analog Power, 2.8 V nominal.
VAA2V8_PIX	C1, G1, H11	Supply	Analog pixel array power. 2.8 V nominal.
DVDDPHY	A8	Supply	PHY I/O power, 1.05 V nominal
DVDDCORE	B8	Supply	Core Power 1.05 V nominal
XSHUTDOWN	G5	Supply	Pin to power down to the VDD supply, active low.
VAA2V8_FILT	F2	Supply	Bypass to AGND with 1 μF capacitor.
ATEST1, ATEST2, EXT_0P4V_MIPI	F11, C2, B2	Do Not Connect	

FEATURES

For a complete description, recommendations, and usage guidelines for product features, please refer to the AR0822 Developer Guide. .

3−EXP eHDR

While AR0822 works in linear mode, one can configure it to eHDR mode. The 3−exp eHDR sequentially captures three exposures by maintaining three read and reset pointers that are interleaved within the within the readout, combines the three exposure in sensor, and sends out the combined frame to minimize the data transferred over MIPI and offload activities on back−end AP. This allows the sensor to handle 120dB of dynamic range. T1, T2 and T3 are configured by different registers. The sensor allows one to choose any exposure ratio by setting the T2 and T3 independently of T1 exposure as long as T2 is less than t1 and T3 is less than T2.

LINE INTERLEAVED HDR (LI−HDR)

In 2−exp LI−HDR mode, the sensor sequentially captures two exposures. The data will be output as line interleaved data to enable the offline chip HDR linear combination and processing. T1 and T2 are also configured by different registers to allow flexible exposure ratio.

enhanced Dynamic Range (eDR) MODE

AR0822 can be configured to work in eDR mode, where sensor can deliver enhanced Dynamic Range. eDR mode has benefit in motion artifact reduction. AR0822 has eDR mode as well as the LI−eDR mode, where it outputs an addition T2 information in addition to the eDR output.

WAKE ON MOTION (WOM) MODE

AR0822 can be configured to work in WoM mode, where sensor while operating in super low power mode can detect motion in the scene. On detecting motion it can send an interrupt over GPIO pin which could be used to wake up the processor. In WoM mode the sensor can also stream at bin4skip2, 480 x 270 resolution.

SHADING CORRECTION (SC)

Lenses tend to produce images whose brightness is significantly attenuated near the edges. There are also other factors causing fixed pattern signal gradients in images captured by image sensors. The cumulative result of all these factors is known as image shading. The AR0822 has an embedded shading correction module that can be programmed to counter the shading effects on each individual Red, GreenB, GreenR and Blue color signal.

ONE−TIME PROGRAMMABLE MEMORY (OTPM)

The AR0822 features 164 bytes of one−time programmable memory (OTPM) available for customer use for storing module specific information. The user may program which set to be used. Additional bits are used by the error detection and correction scheme. OTPM can be accessed through two−wire serial interface. The AR0822 uses the auto mode for fast OTPM programming and read operations.

IMAGE ACQUISITION MODE

AR0822 supports two image acquisition modes:

Electronic Rolling Shutter (ERS) Mode

This is the normal mode of operation. When the AR0822 is streaming, it generates frames at a fixed rate, and each frame is integrated (exposed) using the ERS. When ERS mode is in use, the timing and control logic within the sensor sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and subsequently reading that row, the pixels in the row integrate incident light. The integration (exposure) time is controlled by varying the time between

row reset and row readout. For each row in a frame, the time between row reset and row readout is the same, leading to a uniform integration time across the frame. When the integration time is changed (by using the two−wire interface to change register settings), the timing and control logic controls the transition from old to new integration time in such a way that the stream of output frames from the AR0822 switches cleanly from the old integration time to the new while only generating frames with uniform integration.

Global Reset Release (GRR) Mode

This mode can be used to acquire a single image at the current resolution. In this mode, the end point of the pixel integration time is controlled by an external electromechanical shutter, and the AR0822 provides control signals to interface to that shutter. The benefit of using an external electromechanical shutter is that it eliminates the visual artifacts associated with ERS operation. Visual artifacts can arise in ERS operation, particularly at low frame rates, because an ERS image effectively integrates each row of the pixel array at a different point in time.

MULTI−CAMERA SYNCHRONIZATION

Trigger/Slave Mode

AR0822 supports the following Trigger modes:

Table 5. AR0822 TRIGGER MODES

Num	Mode Name
1	Slave Integration Start Mode
2	Slave Stream Start at Integration Mode
3	Slave Readout Start Mode
4	Slave Stream Start at Readout Mode

Tigger/Slave Mode Timing

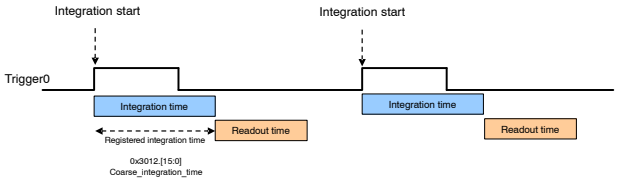


Figure 6. Slave Integration Start Mode

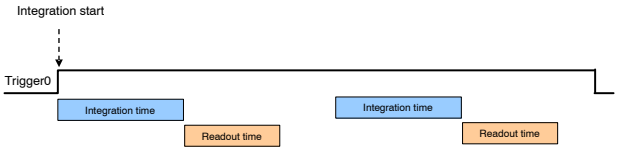


Figure 7. Slave Stream Start at Integration Mode

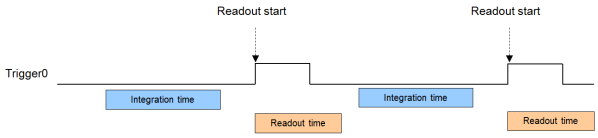


Figure 8. Slave Readout Start Mode

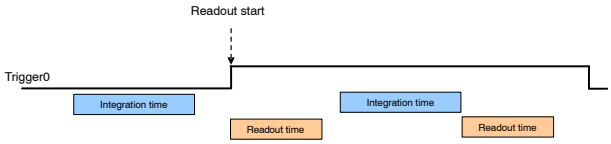


Figure 9. Slave Stream Start at Readout Mode

FLASH TIMING CONTROL

AR0822 supports xenon flash timing through GPIO pins. The timing of Flash Signal is shown in Figure 10.

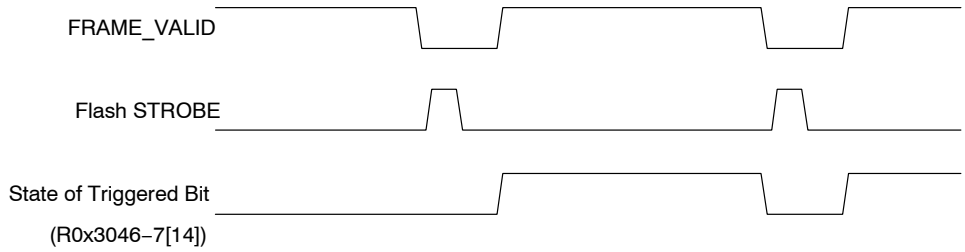


Figure 10. Xenon Flash Enabled

The flash the flash2 registers allow the timing of the flash to be changed. The flash can be programmed to fire only once, delayed by a few frames when asserted, and the flash duration can be programmed.

Pedestal

AR0822 adds the value from R0x301E−F (data_pedestal_) to the incoming value. The data_pedestal_ register is read−only by default but can be made read/write by clearing the reset_register_lock_reg bit in R0x301A−B.

TWO−WIRE SERIAL REGISTER INTERFACE

The two−wire serial interface bus enables read/write access to control and status registers within the AR0822.The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts

as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD off−chip by a 1.5 kΩ resistor. Either the slave or master device can drive SDATA LOW−the interface protocol determines which device is allowed to drive SDATA at any given time.

The protocols described in the two−wire serial interface specification allow the slave device to drive SCLK LOW; the AR0822 uses SCLK as an input only and therefore never drives it LOW.

PROTOCOL

Data transfers on the two−wire serial interface bus are performed by a sequence of low− level protocol elements:

1. A (repeated) start condition
2. A slave address/data direction byte
3. An (a no) acknowledge bit
4. A message byte
5. A stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

Start Condition

A start condition is defined as a HIGH−to−LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a "repeated start" or "restart" condition.

Stop Condition

A stop condition is defined as a LOW−to−HIGH transition on SDATA while SCLK is HIGH.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no−acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A "0" in bit [0] indicates a WRITE, and a "1" indicates a READ. The default slave addresses used by the AR0822 for the MIPI−configured sensor are 0x20 (write address) and 0x21 (read address) in accordance with the MIPI specification. Alternate slave addresses can be selected by configuring the SADDR pads and registers R0x3420 ~ R0x3426.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

Acknowledge Bit

Each 8−bit data transfer is followed by an acknowledge bit or a no−acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

No−Acknowledge Bit

The no−acknowledge bit is generated when the receiver does not drive SDATA LOW during the SCLK clock period following a data transfer. A no−acknowledge bit is used to terminate a read sequence.

TYPICAL SEQUENCE

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8−bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a "0" indicates a write and a "1" indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16−bit register address to which the WRITE should take place. This transfer takes place as two 8−bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8−bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a READ, the master sends the 8−bit write slave address/data direction byte and 16−bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8−bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8−bit transfer. The slave's internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no−acknowledge bit.

Single READ from Random Location

This sequence (Figure 11 on page 10) starts with a dummy WRITE to the 16−bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8−bit read slave address/data direction byte and clocks out one byte of register data. The master terminates the READ by

generating a no−acknowledge bit followed by a stop condition. Figure 11 shows how the internal register address maintained by the AR0822 is loaded and incremented as the sequence proceeds.

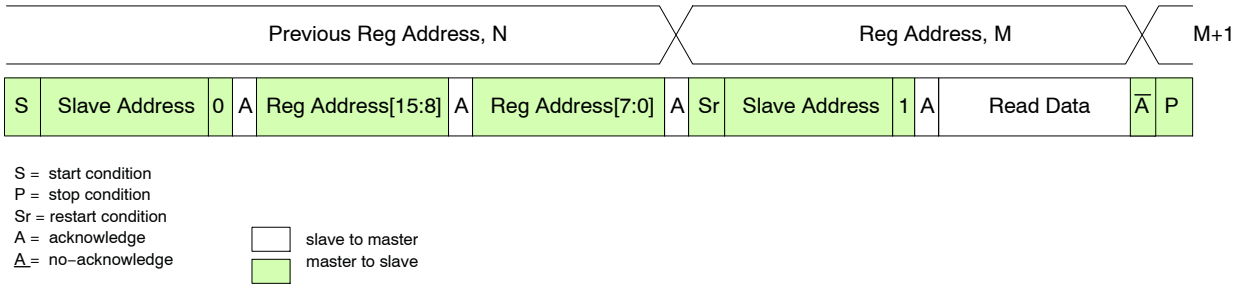


Figure 11. Single READ from Random Location

SINGLE READ FROM CURRENT LOCATION

This sequence (Figure 12) performs a read using the current value of the AR0822 internal register address. The master terminates the READ by generating a no−acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

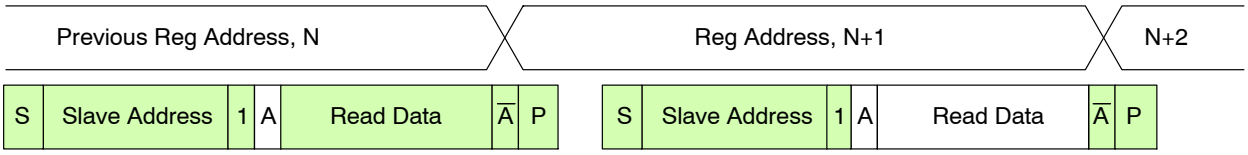


Figure 12. Single READ from Current Location

SEQUENTIAL READ, START FROM RANDOM LOCATION

This sequence (Figure 13) starts in the same way as the single READ from random location (Figure 11). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

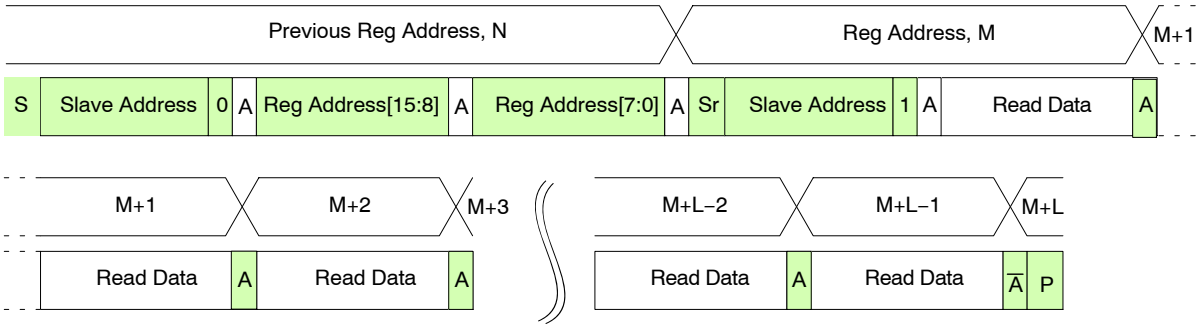


Figure 13. Sequential READ, Start from Random Location

Sequential READ, Start from Current Location

This sequence (Figure 14) starts in the same way as the single READ from current location (Figure 12 on page 10). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

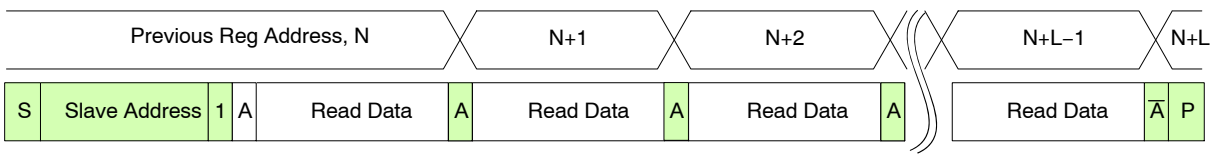


Figure 14. Sequential READ, Start from Current Location

Single WRITE to Random Location

This sequence (Figure 15) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

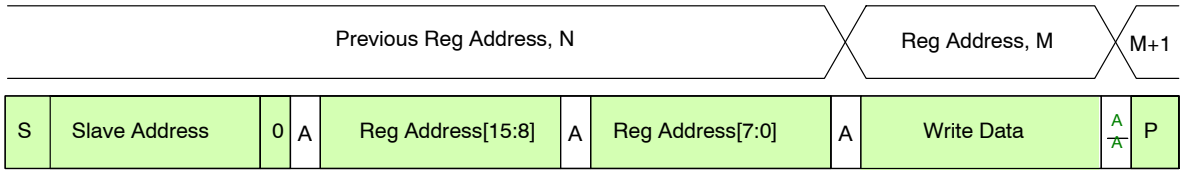


Figure 15. Single WRITE to Random Location

Sequential WRITE, Start at Random Location

This sequence (Figure 16) starts in the same way as the single WRITE to random location (Figure 15). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte WRITEs until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.

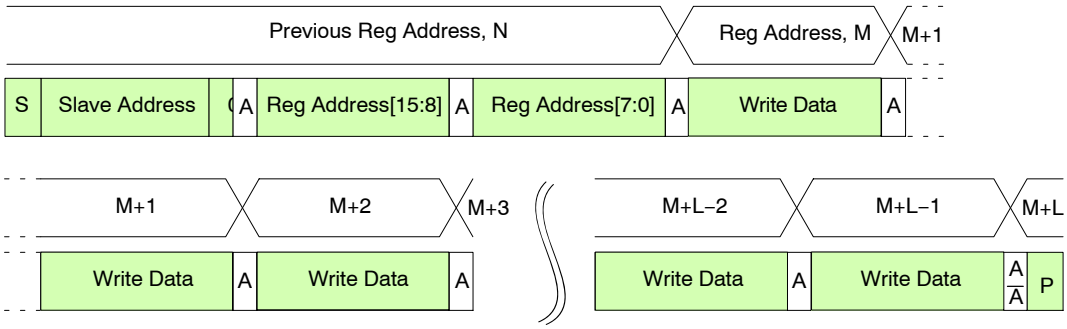
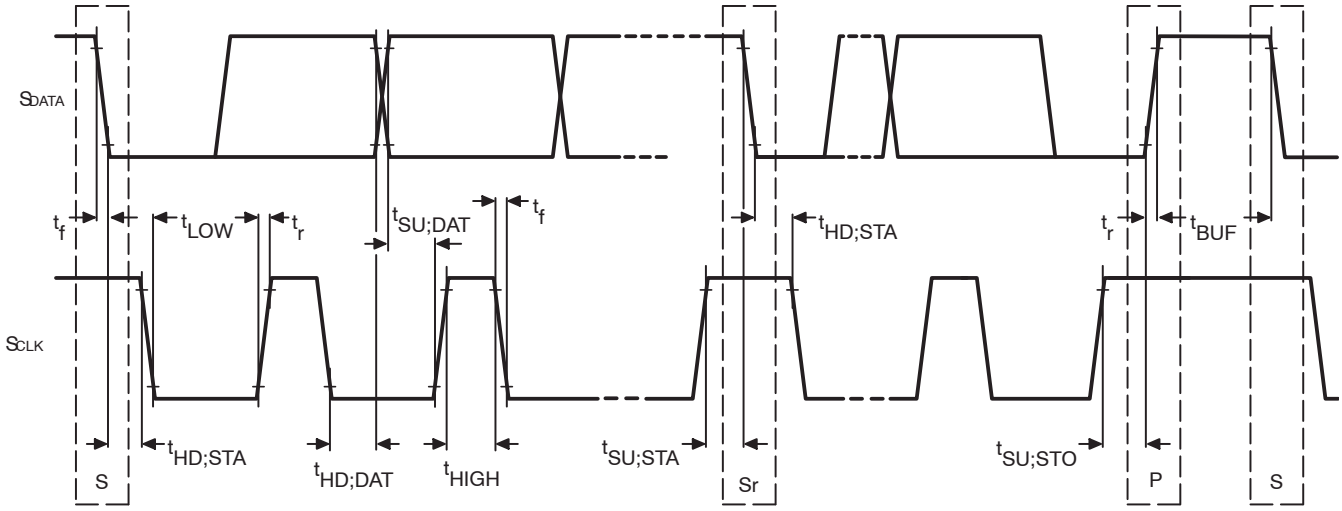


Figure 16. Sequential WRITE, Start at Random Location



Note: Read sequence: For an 8−bit READ, read waveforms start after WRITE command and register address are issued.

Figure 17. Two−Wire Serial Bus Timing Parameters

Table 6. TWO−WIRE SERIAL BUS CHARACTERISTICS

fEXTCLK = 27 MHz; VDD = VDD_PHY = VDD_PLL = 1.05 V; VDD_IO = 1.8 V; VAA = VAA_PIX = 2.8 V; T_A = 25°C

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
M_S_{CLK} Clock Frequency	f_{SCL}	0	100	0	400	0	1000	KHz
S_{CLK} High		8*EXTCLK + S_{CLK} rise time		8*EXTCLK + EXTCLK rise time				μs
S_{CLK} Low		6*EXTCLK + S_{CLK} rise time		6*EXTCLK + S_{CLK} rise time				μs
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4	–	0.6	–	0.26	–	μs
LOW period of the M_S_{CLK} clock	t_{LOW}	4.7	–	1.2	–	0.5	–	μs
HIGH period of the M_S_{CLK} clock	t_{HIGH}	4	–	0.6	–	0.26	–	μs
Set−up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	0.26	–	μs
Data hold time	$t_{HD;DAT}$	0	3.453	0	0.93	0	–	μs
Data set−up time	$t_{SU;DAT}$	250	–	100	–	50	–	ns
Rise time of both M_S_{DATA} and M_S_{CLK} time (10−90%)	t_r	–	1000	20 + 0.1 Cb (Note 4)	300	20 + 0.1 Cb (Note 4)	120	ns
Fall time of both M_S_{DATA} and M_S_{CLK} time (10−90%)	t_f	–	300	20 + 0.1 Cb (Note 4)	300	20 + 0.1 Cb (Note 4)	120	ns
Set−up time for STOP condition	$t_{SU;STO}$	4	–	0.6	–	0.26	–	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	0.5	–	μs
Capacitive load for each bus line	Cb	–	400	–	400	–	500	pF
Serial interface input pin capacitance	C_{IN_SI}	–	3.3	–	3.3	–	3.3	pF
M_S_{DATA} max load capacitance	C_{LOAD_SD}	–	30	–	30	–	30	pF
M_S_{DATA} pull−up resistor	R_{SD}	1.5	4.7	1.5	4.7	1.5	4.7	kΩ

4. This table is based on I^2C standard (v2.1 January 2000). Philips Semiconductor.
5. Two−wire control is I^2C compatible.
6. All values referred to V_{IHmin} = 0.9 V_{DD_IO} and V_{ILmax} = 0.1 V_{DD_IO} levels. Sensor EXCLK = 27 MHz.
7. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK. The two−wire standard specifies a minimum rise and fall time for Fast−Mode and Fast−Mode Plus modes of operation. This specification is not a timing requirement that is enforced on **onsemi** sensor's as a receiver, because these receivers are designed to work in mixed systems with std−mode where no such minimum rise and fall times are required/specified. However, it's the host's responsibility when using fast edge rates, especially when two−wire slew−rate driver control isn't available, to manage the generated EMI, and the potential voltage undershoot on the sensor receiver circuitry, to avoid activating sensor ESD diodes and current−clamping circuits. This is typically not an issue in most applications, but should be checked if below minimum fall times and rise times are required.
8. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the S_{CLK} signal.
9. A Fast−mode I^2C−bus device can be used in a Standard−mode I^2C−bus system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the S_{CLK} signal. If such a device does stretch the LOW period of the S_{CLK} signal, it must output the next data bit to the S_{DATA} line t_r max + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard−mode I^2C−bus specification) before the S_{CLK} line is released.
10. Cb = total capacitance of one bus line in pF.

Table 7. TWO−WIRE SERIAL REGISTER INTERFACE ELECTRICAL CHARACTERISTICS
fEXTCLK = 27 MHz; VDD = VDD_PHY = VDD_PLL = 1.05 V; VDD_IO = 1.8 V; VAA = VAA_PIX = 2.8 V; T_A = 25°C

Parameter	Symbol	Condition	Standard Mode		Fast Mode		Fast Mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
Input HIGH voltage	V_{IH}		0.7 * V_{DDIO}	–	0.7 * V_{DDIO}	–	0.7 * V_{DDIO}	–	V
Input LOW voltage	V_{IL}		–	0.3 * V_{DDIO}	–	0.3 * V_{DDIO}	–	0.3 * V_{DDIO}	V
Output LOW voltage	V_{OL}	V_{DDIO} = (1.7 V − 1.9 V)	–	0.4	–	0.4	–	0.4	V
		I_{OL} = 3 mA							
Output LOW voltage	V_{OL}	V_{DDIO} = (2.6 V − 3.0 V)	–	0.2 * V_{DDIO}	–	0.2 * V_{DDIO}	–	0.2 * V_{DDIO}	V
		I_{OL} = 3 mA							

POWER−ON RESET AND STANDBY TIMING

Power−up Sequence

The recommended power−up sequence for the AR0822 is shown in Figure 18.

The available power supplies (VAA2V8,VAA2V8_PIX,VDDIO2V8R1V8,VDDIO2V8 R1V8_AHM,DVDD, DVDD_DPLL, DVDD1_PHY) must have the separation specified below.

1. Turn on XSHUTDOWN signal at t = 0.
2. Turn on external 2.8 V power supply after t1.
3. After t2, turn on extenal IO power supply.
4. After t3, turn on external 1.05 V supply.
5. After the last power supply is stable, enable EXTCLK.
6. If RESET_N is in a LOW state, hold RESET_N LOW for at least 1ms. If RESET_N is in a HIGH state, assert RESET_N for at least 1 ms.
7. Toggle Stream ON for minimum 2 ms and then off (R0x301A<2> = 1 and 0).
8. Wait 160000 EXTCLKs (for internal initialization into software standby).
9. Configure PLL, output and image settings to desired values.
10. Wait 1 ms for the PLL to lock.
11. Set streaming mode (R0x301A<2> = 1).

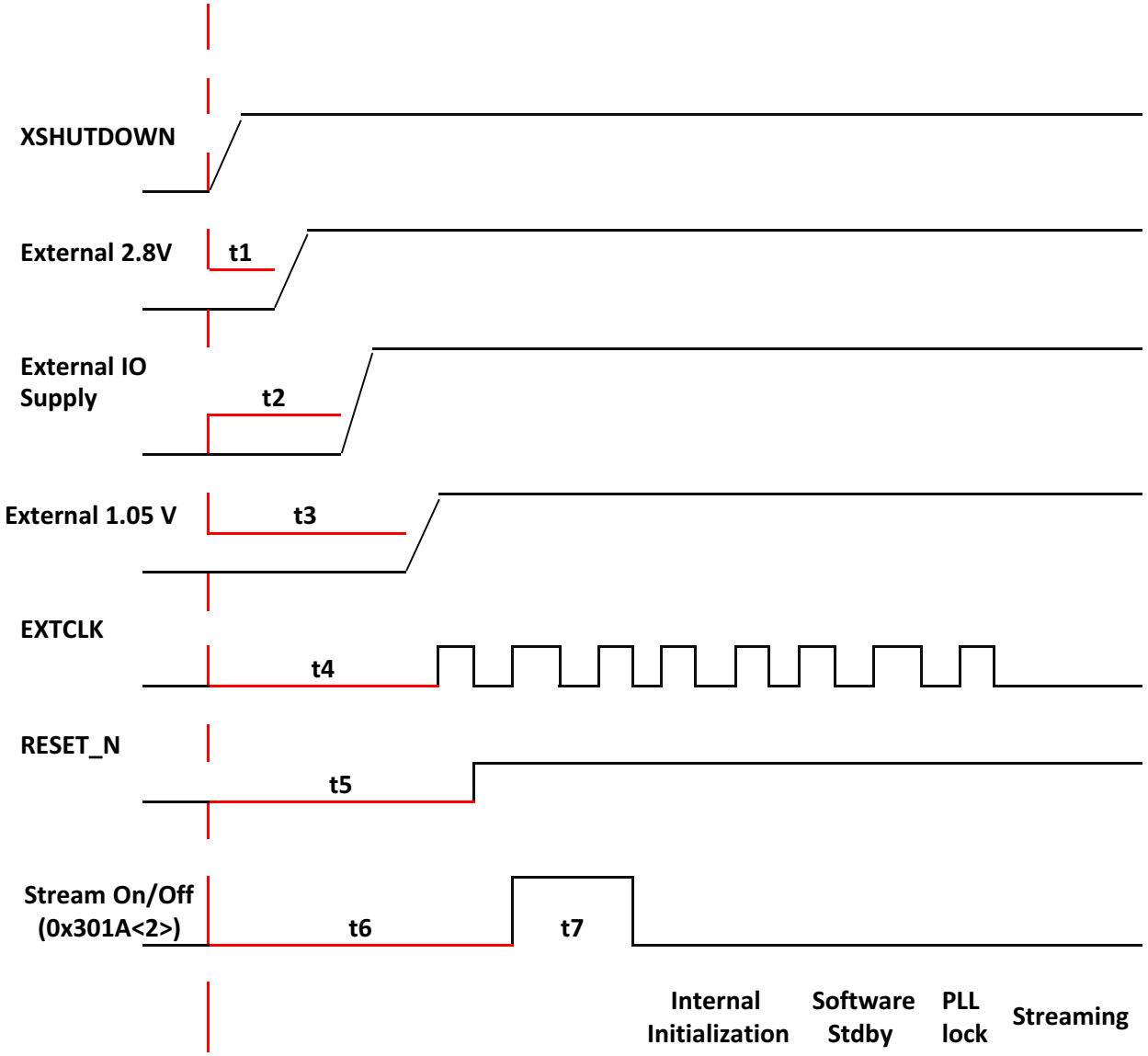


Figure 18. Power−up Sequence

Table 8. RECOMMENDED POWER−UP TIMING

Timing	Min	Typ	Max
t1	10 μs	100 μs	–
t2	10 μs	200 μs	–
t3	10 μs	300 μs	–
t4	500 μs	1 ms	–
t5	–	t4 + 1 ms	–
t6	–	t5 + 1600000 EXTCLK cycles	–
t7	2 ms	–	–

Power−Down Sequence

The recommended power−down sequence for the AR0822 is shown below. The available power supplies must have the separation specified below.

1. Disable streaming if output is active by setting standby R0x301A[2] = 0.
2. Pull RESET_N signal low.
3. Pull XSHUTDOWN signal Low
4. The soft standby state is reached after the current row or frame, depending on configuration, has ended.
5. Turn off external 1.05 V supply
6. Turn off external IO supply
7. Turn off External 2.8 V supply
8. Turn off External Clock
9. From power down to next power (power down and up of the 2.8 V supply as a reference), one has to wait at least 100 ms. All decoupling caps from regulators must be completely discharged.

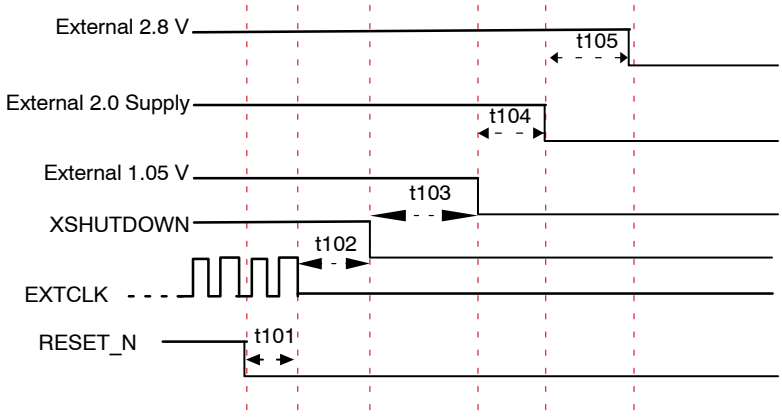


Figure 19. Power−down Sequence

Table 9. RECOMMENDED POWER−DOWN TIMING

Symbol	Min	Max	Unit
t101	0		μs
t102	0	–	μs
t103	0	–	μs
t104	0	–	
t105	0	–	

HARD STANDBY SEQUENCE

The recommended hard standby sequence for the AR0822 is shown below.

1. Disable streaming if output is active by setting standby R0x301a[2] = 0
2. Do a hard reset by pulling down RESET_N.
3. Disable the EXTCLK after 100us.
4. Assert the XSHUTDOWN pin after 100 μs. At this time, make sure EXTCLK should be 0.

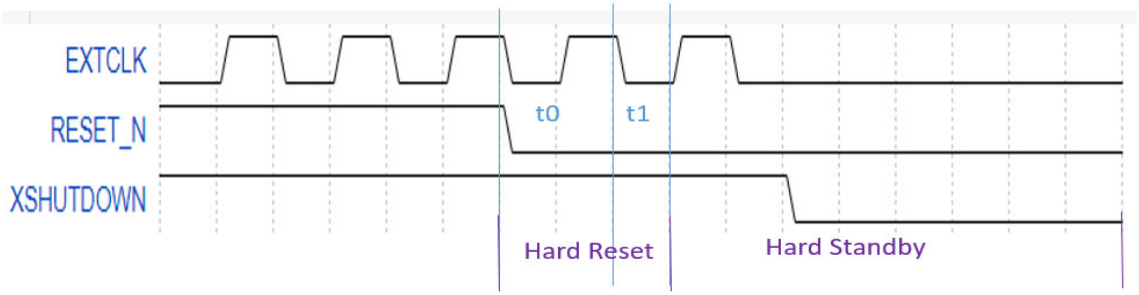


Figure 20.

XSHUTDOWN signaling is ACTIVE LOW.

Note: The difference between Hard reset and Hard standby is that the former will power down all the circuits connected to all power supplies. The latter will make sure the leakage current through VDD and VDD_PHY is minimum.

Table 10. RECOMMENDED HARD STANDBY TIMING

SN	Definition	Symbol	Min	Typ	Max
1	RESET_N to EXTCLK	t0	100 μs	–	–
2	EXTCLK to XSHUTDOWN	t1	100 μs	–	–

SOFT STANDBY AND SOFT RESET

The AR0822 can reduce power consumption by switching to the soft standby state when the output is not needed. Register values are retained in the soft standby state. Once this state is reached, soft reset can be enabled optionally to return all register values back to the default. The details of the sequence are described below and shown in Figure 21 on page 17.

Soft Standby

1. Disable streaming if output is active by setting mode_select = 0 (R0x0100).
2. The soft standby state is reached after the current row or frame, depending on configuration, has ended.
3. The soft standby with external clock disabled retains register values, uses minimum power, and allows faster power−up.

Soft Reset

1. Follow the soft standby sequence list above.
2. Set software_reset = 1 (R0x0103) to start the internal initialization sequence.
3. After 16000 EXTCLKs, the internal initialization sequence is completed and the current state returns to soft standby automatically. All registers, including software_reset, returns to their default values.

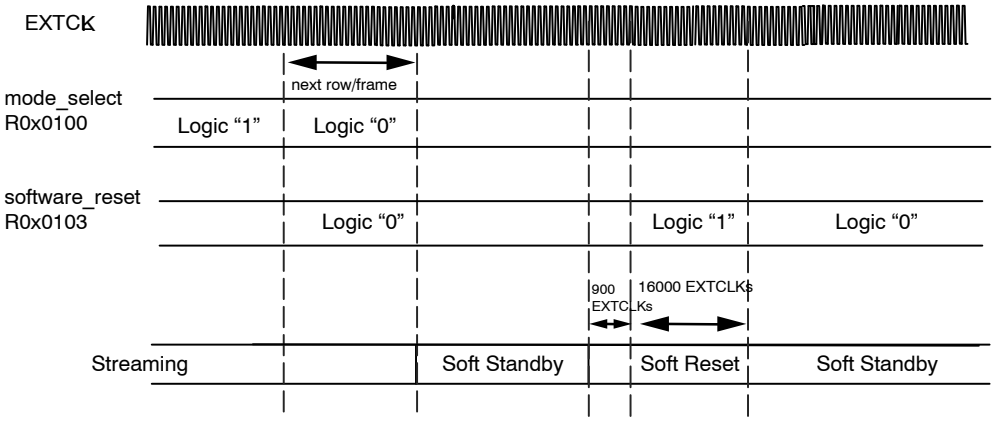


Figure 21. Soft Standby and Soft Reset

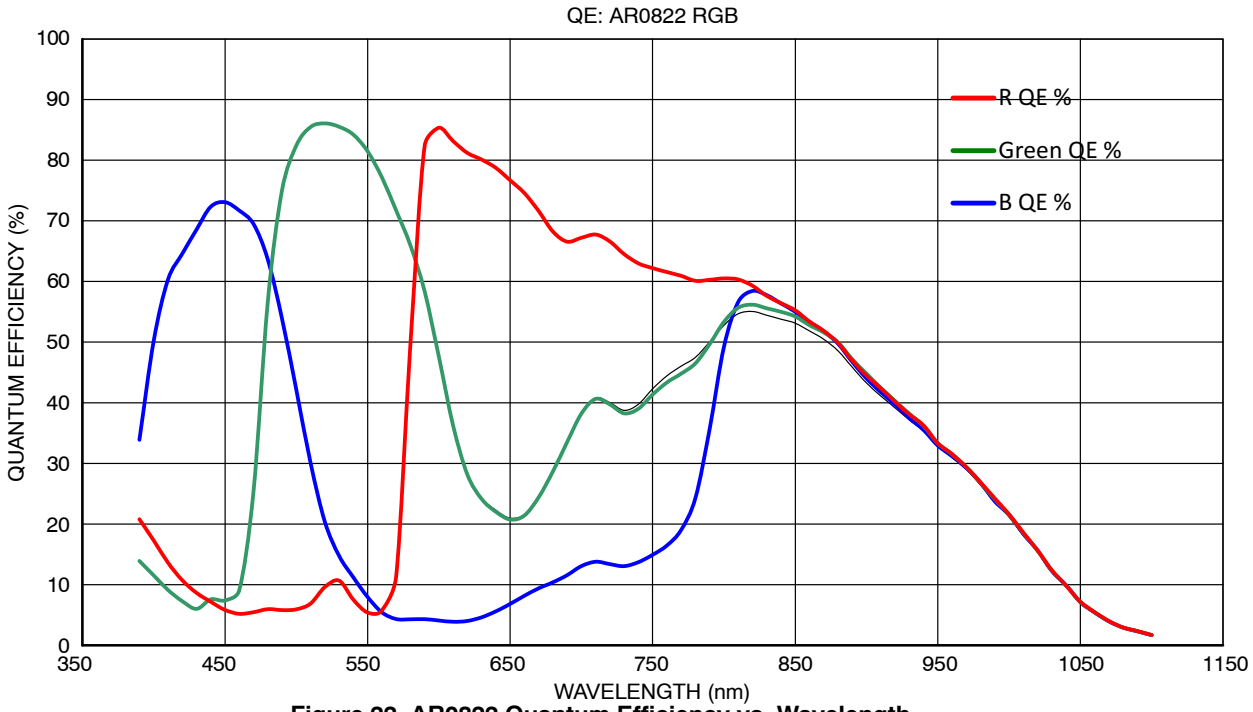


Figure 22. AR0822 Quantum Efficiency vs. Wavelength

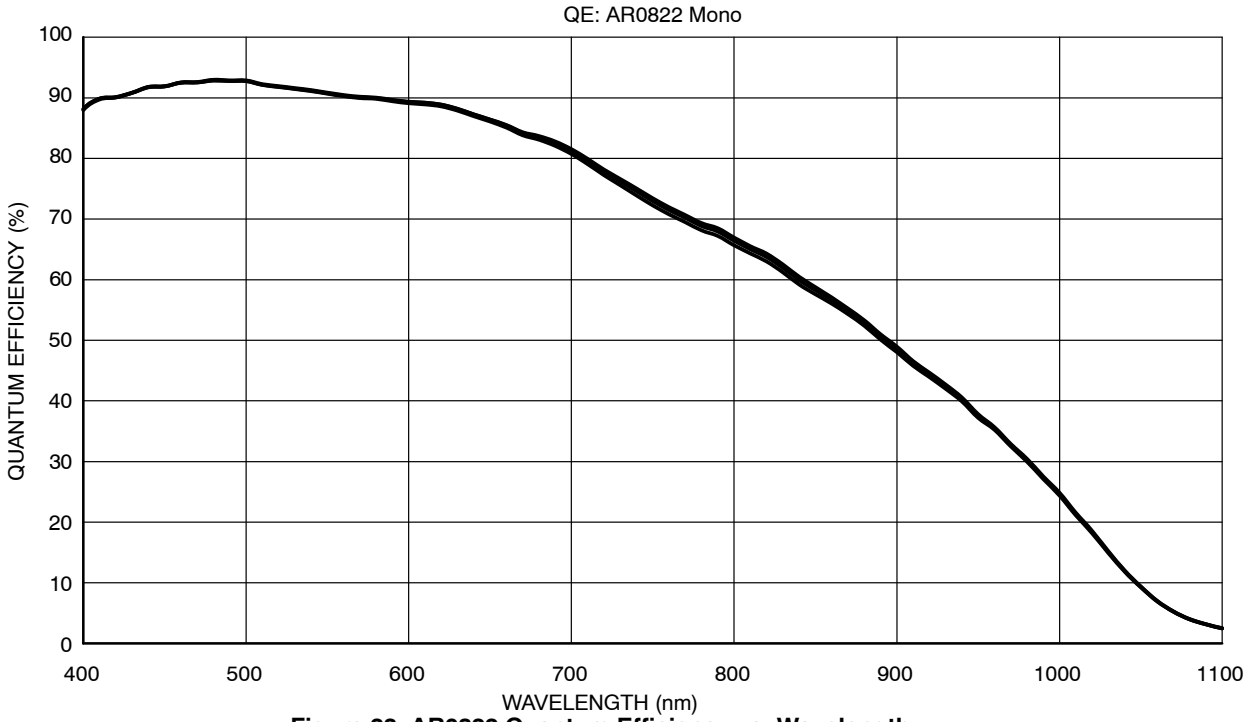


Figure 23. AR0822 Quantum Efficiency vs. Wavelength

CRA vs. Image Height Plot

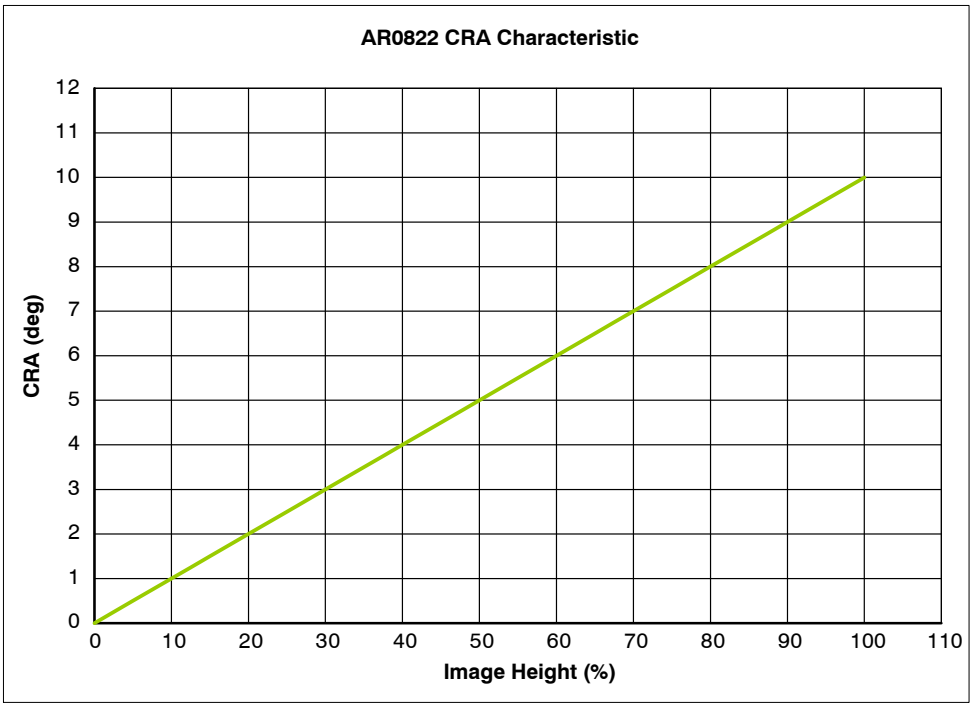


Figure 24. Chief Ray Angle – 10°

Image Height		CRA
(%)	(mm)	(deg)
0	0	0
5	0.220	0.50
10	0.441	1.00
15	0.661	1.50
20	0.881	2.00
25	1.101	2.50
30	1.322	3.00
35	1.542	3.50
40	1.762	4.00
45	1.983	4.50
50	2.203	5.00
55	2.423	5.50
60	2.643	6.00
65	2.864	6.50
70	3.084	7.00
75	3.304	7.50
80	3.525	8.00
85	3.745	8.50
90	3.965	9.00
95	4.186	9.50
100	4.406	10.00

Table 11. I/O TIMING CHARACTERISTICS (1.8 V V_{DD}_IO)

Symbol	Definition	Condition	VDD_IO = 1.8 V			Unit
			Min	Typ	Max	
f_{EXTCLK}	Input clock frequency	PLL Enabled	6	–	50	MHz
t_{EXTCLK}	Input clock period	PLL Enabled	20	–	166	ns
t_{JITTER}	Input clock jitter		–	–	1	ns

Table 12. MIPI HIGH−SPEED TRANSMITTER DC ELECTRICAL CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max	Unit
VDD	HS transmit digital voltage		140	–	270	mV
VCMTX	HS transmit static common mode voltage		150	–	250	mV
A VOD	VOD mismatch when output is Differential−1 or Differential−0		–	–	14	mV
A VCMTX(1,0)	VCMTX mismatch when output is Differential−1 or Differential−0		–	–	5	mV
VOHHS	HS output HIGH voltage		–	–	360	V
ZOS	Single−ended output impedance		40	–	62.5	fi
A ZOS	Single−ended output impedance mismatch		–	–	10	%

Table 13. MIPI HIGH−SPEED TRANSMITTER AC ELECTRICAL CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max	Unit
	Data bit rate		–	–	1971	Mb/s
trise	20–80% rise time		–	185	–	ps
tfall	20–80% fall time		–	176	–	ps

Table 14. MIPI LOW−POWER TRANSMITTER DC ELECTRICAL CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max	Unit
VOL	Thevenin output low level		–	–	50	mV
VOH	Thevenin output high level		0.85	1	1.3	V
ZOLP	Output impedance of LP transmitter		110	–	–	

Table 15. LOW−POWER TRANSMITTER AC ELECTRICAL CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max	Unit
trise	15–85% rise time		–	–	25	ns
tfall	15–85% fall time		–	–	25	ns
Slew	Slew rate (CLOAD 5–20 pF)		–	–	200	mV/ns
Slew	Slew rate (CLOAD 20–70 pF)		–	–	150	mV/ns

Table 16. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Minimum	Maximum	Unit
VSUPPLY (2.8 V)	Power supply voltage 2.8 V	−0.3	3.5	V
VSUPPLY (1.8 V)	Power supply voltage 1.8 V	−0.3	2.6	V

Table 16. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Minimum	Maximum	Unit
VSUPPLY (1.05 V)	Power supply voltage 1.05 V	−0.3	1.7	V
ISUPPLY	Total power supply current	–	1500	mA
IGND	Total ground current	–	1500	mA
VIN	DC input voltage	−0.3	VDD_IO + 0.3	V
VOUT	DC output voltage	−0.3	VDD_IO + 0.3	V
TSTG (Note 11)	Storage temperature	−40	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
11. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
12. To keep dark current and shot noise artifacts from impacting image quality, keep operating temperature at a minimum.

Table 17. DC_ELECTRICAL DEFINITIONS AND CHARACTERISTICS

fEXTCLK = 27 MHz; VAA2V8_ANA = 2.8 V; VAA2V8_PIX = 2.8 V; DVDD = 1.05 V; DVDD_MEM = 1.05 V; DVDD_ANA = 1.05 V; DVDDPHY = 1.05 V; VDDIO2V8R1V8 = 1.8 V; TJ = 25C for typical; T_J = 60°C for max.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VDDIO	I/O Digital Voltage		1.7	1.8	1.9	V
VAA, VAA_PIX	Analog, Pixel Voltage		2.7	2.8	2.9	V
VDD_PHY, VDD	PHY/Digital Voltage		1.0	1.05	1.1	V
OPERATING CURRENT						
IDD_IO	I/O Digital Current	3840x2160 3−exp eHDR @30fps	−	21.2	−	mA
IAA/IAA_PIX	Analog/Pixel Current		−	91.2	−	mA
IDD_PHY/IDD	PHY/Digital Current		−	234.5	−	mA
IDD_IO	I/O Digital Current	3840x2160 Linear mode @60fps	−	15.7	65	mA
IAA/IAA_PIX	Analog/Pixel Current		−	74.3	125	mA
IDD_PHY/IDD	PHY/Digital Current		−	151.8	290	mA
IDD_IO	I/O Digital Current	3840x2160 Linear mode @30fps	−	9.6	−	mA
IAA/IAA_PIX	Analog/Pixel Current		−	40.93	−	mA
IDD_PHY/IDD	PHY/Digital Current		−	86.78	−	mA
IDD_IO	I/O Digital Current	1920x1080 Binning Linear mode @120fps	−	15.6	−	mA
IAA/IAA_PIX	Analog/Pixel Current		−	69.5	−	mA
IDD_PHY/IDD	PHY/Digital Current		−	115.3	−	mA
IDD_IO	I/O Digital Current	3840x2160 2−exp LI−HDR mode @30fps	−	15.8	−	mA
IAA/IAA_PIX	Analog/Pixel Current		−	68.0	−	mA
IDD_PHY/IDD	PHY/Digital Current		−	189.4	−	mA
IDD_IO	I/O Digital Current	3840x2160 eDR 3−exp mode @30fps	−	15.59	−	mA
IAA/IAA_PIX	Analog/Pixel Current		−	70.16	−	mA
IDD_PHY/IDD	PHY/Digital Current		−	266.2	−	mA
IDD_IO	I/O Digital Current	3840x2160 LI−eDR mode @30fps	−	19.1	−	mA
IAA/IAA_PIX	Analog/Pixel Current		−	88.0	−	mA
IDD_PHY/IDD	PHY/Digital Current		−	242.9	−	mA
IDD_IO	I/O Digital Current	480x270 (no streaming) Motion Detection Mode	−	0.4	−	mA
IAA/IAA_PIX	Analog/Pixel Current		−	1.62	−	mA
IDD_PHY/IDD	PHY/Digital Current		−	11.82	−	mA
IDD_IO	I/O Digital Current	480x270 (streaming) Motion Detection Mode		0.38		mA
IAA/IAA_PIX	Analog/Pixel Current			2.59		mA
IDD_PHY/IDD	PHY/Digital Current			11.95		mA
IDD_IO	I/O Digital Current	eDR_3840x2160_30fps		15.59		mA
IAA/IAA_PIX	Analog/Pixel Current			70.16		mA
IDD_PHY/IDD	PHY/Digital Current			243.25		mA
STANDBY CURRENT						
IDD_IO	I/O Digital Current	Reset_N Low & XSHUTDOWN Signal High (EXT_CLK on)	−	0.05	2	mA
IAA/IAA_PIX	Analog/Pixel Current		−	0.06	5	mA
IDD_PHY/IDD	PHY/Digital Current		−	2.53	57	mA

Table 17. DC_ELECTRICAL DEFINITIONS AND CHARACTERISTICS

fEXTCLK = 27 MHz; VAA2V8_ANA = 2.8 V; VAA2V8_PIX = 2.8 V; DVDD = 1.05 V; DVDD_MEM = 1.05 V; DVDD_ANA = 1.05 V; DVDDPHY = 1.05 V; VDDIO2V8R1V8 = 1.8 V; TJ = 25C for typical; T_J = 60°C for max.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
STANDBY CURRENT						
IDD_IO	I/O Digital Current	Reset_N & XSHUTDOWN Signal Low (EXT_CLK on)	–	0.05	0.15	mA
IAA/IAA_PIX	Analog/Pixel Current		–	0.06	0.35	mA
IDD_PHY/IDD	PHY/Digital Current		–	0.02	0.48	mA
IDD_IO	I/O Digital Current	Standby Current When asserting R0x301A[2] = 0 (EXT_CLK off)	–	0.02	5	mA
IAA/IAA_PIX	Analog/Pixel Current		–	1.08	2	mA
IDD_PHY/IDD	PHY/Digital Current		–	1.6	27	mA
IDD_IO	I/O Digital Current	Standby Current When asserting R0x301A[2] = 0 (EXT_CLK on)	–	0.04	2	mA
IAA/IAA_PIX	Analog/Pixel Current		–	1.08	5	mA
IDD_PHY/IDD	PHY/Digital Current		–	6.24	60	mA

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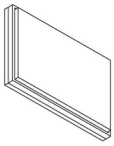
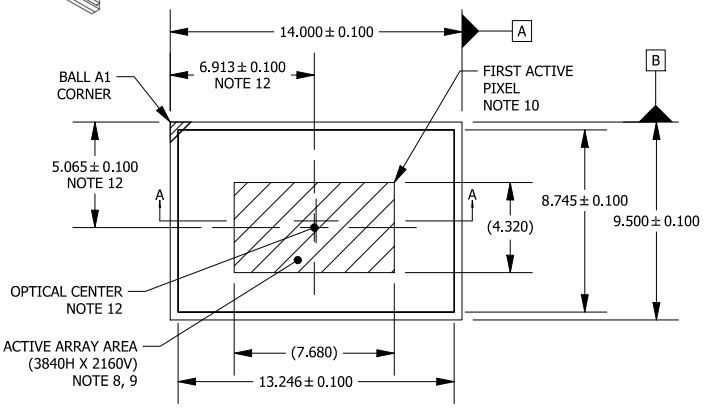
ISSUE O

DATE 12 MAY 2020

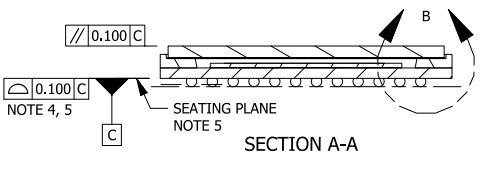




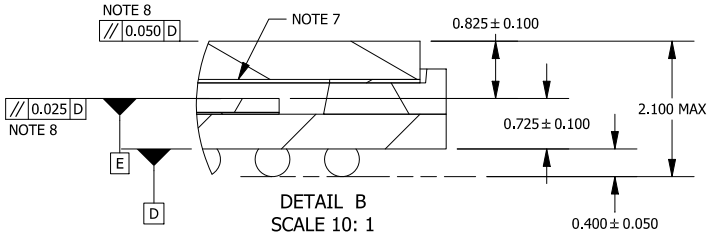
TOP VIEW

NOTES:

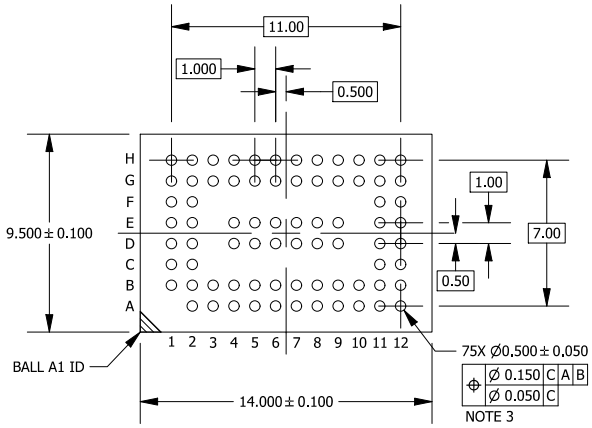
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS [mm].
3. SOLDER BALL DIAMETER IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. GLASS: 0.550 THICKNESS; REFRACTIVE INDEX = 1.52.
7. AIR GAP BETWEEN GLASS AND PIXEL ARRAY: 0.275 THICKNESS.
8. PARALLELISM APPLIES ONLY TO THE ACTIVE ARRAY.
9. MAXIMUM ROTATION OF ACTIVE ARRAY RELATIVE TO DATUMS A AND B IS ± 1°.
10. REFER TO THE DEVICE DATA SHEET FOR TOTAL PIXEL ARRAY DEFINITIONS.
11. PACKAGE CENTER (X, Y) = (0.000, 0.000).
12. OPTICAL CENTER RELATIVE TO PACKAGE CENTER (X, Y) = (-0.087, -0.315).



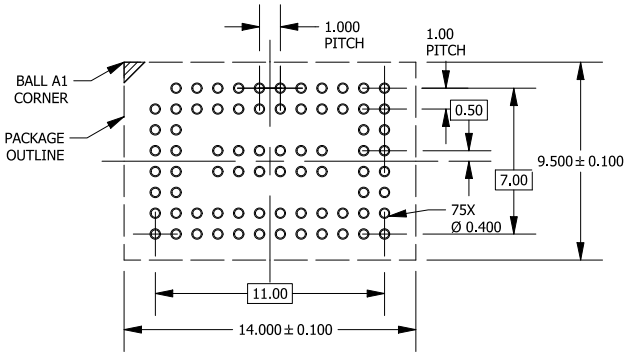
SECTION A-A



DETAIL B
SCALE 10: 1



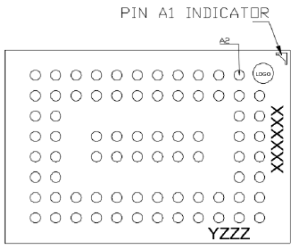
BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
Y = Year
ZZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**PBGA75 14x9.5**	**PAGE 1 OF 1**

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