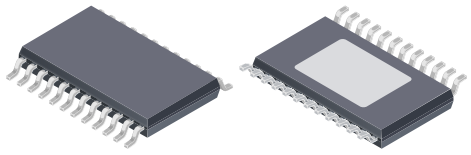
A4958 and A4959

50 Volt, 5 Amp DC Motor Driver

FEATURES AND BENEFITS

- Low (90 mΩ) $R_{DS(on)}$ outputs
- Integrated current limit circuit (OCL)
- Configurable for industry-standard input formats
  - □ A4959 – Phase, Enable, Mode
  - □ A4958 – IN1, IN2
- Low-power standby mode
- Fault output
- Adjustable current limit
- Scaled current output
- Synchronous rectification
- Internal UVLO
- Crossover-current protection

PACKAGE: 24-Lead TSSOP (suffix “LP”)



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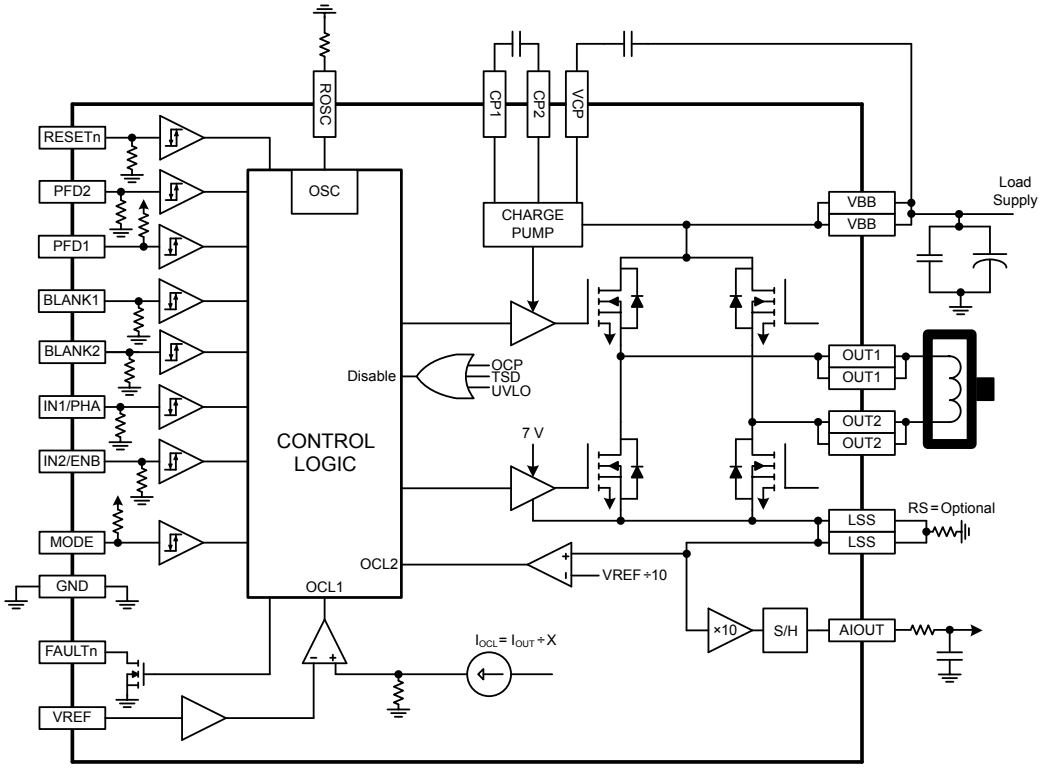
DESCRIPTION

Designed for pulse-width-modulated (PWM) control of DC motors, the A4958 and A4959 are capable of peak output currents to ±5 A and operating voltages to 50 V.

Input terminals are provided for use in controlling the speed and direction of a DC motor with externally applied PWM control signals. Internal synchronous rectification control circuitry is provided to lower power dissipation during PWM operation.

Internal circuit protection includes overcurrent limit, thermal shutdown with hysteresis, undervoltage monitoring of VBB, and crossover-current protection.

The A4958 and A4959 are supplied in a low-profile 24-lead TSSOP package (suffix “LP”) with exposed power tab.



Typical Application

SPECIFICATIONS

SELECTION GUIDE

Part Number	Temperature Range	Packing
A4958GLPTR-T	–40°C to 105°C	4000 pieces per 13 inch reel
A4959GLPTR-T	–40°C to 105°C	4000 pieces per 13 inch reel

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BB}		50	V
Motor Outputs	V_{OUT}		–2 to 52	V
LSS	V_{LSS}		±0.5	V
		t_W < 500 ns	±2.5	V
Output Current	I_{OUT}	Continuous [1]	6	A
		t_W < 500 ns	12	A
VREF	V_{REF}		–0.3 to 6	V
Logic Input Voltage Range	V_{IN}		–0.3 to 6	V
Junction Temperature	T_J		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C
Operating Temperature Range	T_A	Range G	–40 to 105	°C

[1] Power dissipation and thermal limits must be observed.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	24-lead TSSOP (package LP), on JEDEC High-K board	28	°C/W
		24-lead TSSOP (package LP), on 2-sided PCB 1-in.^{2} copper	38	°C/W

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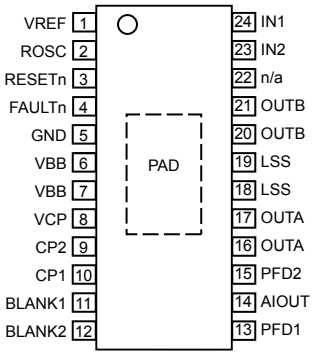
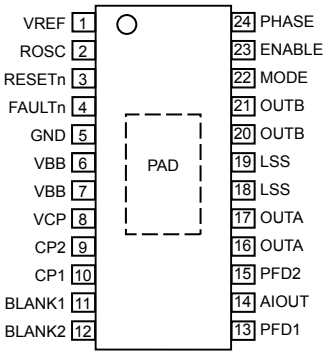
PINOUT DIAGRAM AND TERMINAL LIST TABLE



A4958LP Package Pinouts



A4959LP Package Pinouts

A4958 Terminal List Table

Terminal Number	Name	Function
1	VREF	Set current limit
2	ROSC	Set fixed off-time
3	RESETn	Standby mode when low
4	FAULTn	Fault condition when low
5	GND	Ground
6	VBB	Power supply
7	VBB	Power supply
8	VCP	Charge pump capacitor
9	CP2	Charge pump capacitor
10	CP1	Charge pump capacitor
11	BLANK1	Set BLANK time
12	BLANK2	Set BLANK time
13	PFD1	Set decay mode for fixed off-time
14	AIOUT	Current monitor output
15	PFD2	Set decay mode for fixed off-time
16	OUTA	Motor output
17	OUTA	Motor output
18	LSS	Low-side source connection
19	LSS	Low-side source connection
20	OUTB	Motor output
21	OUTB	Motor output
22	n/a	Unused
23	IN2	Control input
24	IN1	Control input
PAD	PAD	Exposed pad for enhanced thermal dissipation

A4959 Terminal List Table

Terminal Number	Name	Function
1	VREF	Set current limit
2	ROSC	Set fixed off-time
3	RESETn	Standby mode when low
4	FAULTn	Fault condition when low
5	GND	Ground
6	VBB	Power supply
7	VBB	Power supply
8	VCP	Charge pump capacitor
9	CP2	Charge pump capacitor
10	CP1	Charge pump capacitor
11	BLANK1	Set BLANK time
12	BLANK2	Set BLANK time
13	PFD1	Set decay mode for fixed off-time
14	AIOUT	Current monitor output
15	PFD2	Set decay mode for fixed off-time
16	OUTA	Motor output
17	OUTA	Motor output
18	LSS	Low-side source connection
19	LSS	Low-side source connection
20	OUTB	Motor output
21	OUTB	Motor output
22	MODE	Control input
23	ENABLE	Control input
24	PHASE	Control input
PAD	PAD	Exposed pad for enhanced thermal dissipation

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ELECTRICAL CHARACTERISTICS [1]: Valid at T_A = 25°C, V_{BB} = 5.5 to 50 V, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL						
VBB Supply Current	I_{BB}	Outputs off	–	10	15	mA
		Standby mode	–	–	15	µA
VREF Input Current	I_{VREF}		–5	<1	5	µA
VREF Input Range	V_{REF}	External sense resistor	0	–	4	V
		Internal mode (R_{SENSE} = 0)	0	–	2	V
Current Sense Accuracy – Internal	I_{OCL}	V_{REF} = 2 V	4.25	5	5.75	A
		V_{REF} = 200 mV, T_A= 25°C	300	500	625	mA
Current Sense Accuracy – External	A_V	V_{REF} / V_{LSS}, V_{REF} = 200 mV to 4 V	9.5	10	10.5	V/V
	V_{OS}	Offset	1	4.5	9	mV
AIOUT Gain	A_V	I = 200 µA, V_{LSS} = 50 to 400 mV	8.5	10	11.5	V/V
Sample/Hold Droop Rate	V_{DR}		–	–	1	mV/µs
AIOUT Output Impedance	R_{AIOUT}		–	1	–	kΩ
Power-Up Delay	t_{PU}		–	200	400	µs
OUTPUT DRIVERS						
Total Driver On-Resistance (Sink + Source)	$R_{DS(ON)}$	I = 4 A, T_J = 25°C, V_{BB} = 8 V	–	180	220	mΩ
		I = 4 A, T_J = 125°C, V_{BB} = 8 V	–	280	350	mΩ
		I = 4 A, T_J = 25°C, V_{BB} = 5.5 V	–	200	–	mΩ
		I = 4 A, T_J = 125°C, V_{BB} = 5.5 V	–	300	–	mΩ
Output Leakage Current	I_{LK}		–10	–	10	µA
Rise Time	t_r	V_{BB} = 12 V	40	80	200	ns
Fall Time	t_f	V_{BB} = 12 V	40	100	200	ns
LOGIC INPUT AND OUTPUT						
Logic Output Voltage	V_O	I = 2 mA, fault asserted	–	0.2	0.5	V
Output Leakage	I_{FLTn}	V = 5 V	–	–	5	µA
Logic Input Voltage High	V_{IH}		2.0	–	–	V
Logic Input Voltage Low	V_{IL}		–	–	0.8	V
Logic Input Voltage Standby Mode	$V_{IN(STANDBY)}$	Standby mode	–	–	0.4	V
Input Hysteresis	V_{HYS}		–	250	550	mV
Input Pull-Up Resistor	R_{PU}	PFD1, MODE (to 5 V_{INT})	30	50	70	kΩ
Input Pull-Down Resistor	R_{PD}	RESETn, PFD2, BLANK1, BLANK2, ENB, IN1, IN2, PHA	30	50	70	kΩ
PWM TIMING						
Blank Time	t_{BLK}	BLANKx = 00 and 11, relative to target	–20	0	20	%
		BLANKx = 01 and 10, relative to target	–30	0	30	%
Fixed Off-Time	t_{OFF}	Relative to target, R_{OSC} = 8 to 80 kΩ	–20	0	20	%
PROTECTION CIRCUITS						
UVLO Enable Threshold	V_{UVLO}	V_{BB} rising	5.1	–	5.4	V
UVLO Hysteresis	$V_{UVLOHYS}$		200	275	350	mV
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	155	170	185	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = $T_{JTSD} - \Delta T_J$	–	30	–	°C

[1] Specified limits are tested at a single temperature and assured over operating temperature range by design and characterization.

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FUNCTIONAL DESCRIPTION

Device Operation

The A4958/9 is designed to operate DC motors. The output drivers are capable of 50 V and 5 A peak operating currents. Actual 100% steady-state DC current capability depends on thermal capability of the package, PCB, and ambient temperature. N-channel DMOS drivers feature internal synchronous rectification to reduce power dissipation. Peak current can be regulated by fixed off-time pulse-width-modulated (PWM) control circuitry.

Protection circuitry includes thermal shutdown, and protection against shorted loads, or against output shorts to ground or supply. Undervoltage lockout prevents damage by keeping the outputs off until the driver has enough power supply voltage to operate normally.

Internal PWM Current Control

Peak current is set by sensing the current through the high-side MOSFET or by monitoring the voltage on an external sense resistor.

Using high side monitor:

$$I_{OCL} = V_{REF} \times (2.5\ A/V)$$

Using external sense resistor:

$$I_{OCL} = V_{REF} / (A_V \times R_{SENSE}) + V_{OS} / R_{SENSE}$$

When the peak current is exceeded, the source driver turns off to chop the current according to mode selected by PFD pin.

The high-side monitor is always active. If using external sense resistor, make sure the resistor value is chosen so that the I_{PEAK} trip level is below that of high-side monitor.

Blank Function

The internal current sense circuit is ignored at the beginning of PWM transitions so as not to falsely sense overcurrent events due to motor capacitance. The blank time can be adjusted as follows, allowing high or low capacitive loads to be optimized. This blanking time sets the minimum on-time of the PWM.

BLANK2	BLANK1	T (us)
0	0	3
0	1	1
1	0	2
1	1	6

R_{OSC}

Resistor tied to ground will set the fixed off-time that occurs during current limit operation. Off-Time is set by the following equation:

$$t_{off} = R_{OSC} / 825\ (where\ t_{off}\ is\ in\ microseconds)$$

R_{OSC} is allowed in the range 8 to 80 kΩ.

If R_{OSC} is connected to GND or >3.5 V then t_{OFF} will default to 25 µs.

PFD Function

Percent Fast Decay is determined by the state of PFD logic inputs as shown below. After a current limit event, load current will recirculate in slow decay, fast decay, or mixed decay mode.

PFD2	PFD1	PFD
0	0	0%
0	1	15%
1	0	50%
1	1	100%

Standby Mode

Low-power standby mode is activated when RESETn input is set low. Low-power standby mode disables most of the internal circuitry, including the charge pump and the regulator. When the A4958/9 is coming out of standby mode, the charge pump should be allowed to reach its regulated voltage (a maximum delay of 200 µs) before any PWM commands are issued to the device.

TSD

If the die temperature increases to approximately T_{TSD}, the full bridge outputs will be disabled until the internal temperature falls below a hysteresis level of T_{HYS}.

FAULTn Output

The fault pin is driven low to indicate overtemperature (TSD) status. The fault pin is not used for normal current limit or supply undervoltage.

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Control Logic

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RESETn	IN1	IN2	I > IOCL	OUT1	OUT2	Function
1	0	0	0	Z	Z	Coast
1	0	1	0	L	H	Reverse
1	1	0	0	H	L	Forward
1	1	1	0	L	L	Brake (slow decay)
1	1	1	1	L	L	Brake (slow decay)
1	0	1	1	H/L	L	Chop (decay set by PFD pins) [1]
1	1	0	1	L	H/L	Chop (decay set by PFD pins) [1]
0	X	X	X	Z	Z	Standby Mode

[1] Outputs change to High-Z state when load current approaches zero.

A4959

RESETn	PHASE	ENABLE	MODE	I > IOCL	OUT1	OUT2	Function
1	1	1	X	0	H	L	Forward
1	0	1	X	0	L	H	Reverse
1	X	0	1	0	L	L	Brake (slow decay)
1	1	0	0	0	L	H	Fast Decay SR [1]
1	0	0	0	0	H	L	Fast Decay SR [1]
1	1	1	X	1	L	H/L	Chop (decay set by PFD pins) [1]
1	0	1	X	1	H/L	L	Chop (decay set by PFD pins) [1]
0	X	X	X	X	Z	Z	Standby Mode

[1] Outputs change to High-Z state when load current approaches zero.

AIOUT

An analog output can be used to monitor peak current through an external sense resistor (if used). The voltage on the sense resistor is amplified by 10. The circuit uses a tracking sample/hold to allow AIOUT to represent peak load current. Representation of load current depends on the operational mode as described in below table.

Operational MODE	AIOUT Function
PWM via ENABLE; Mode = SLOW decay	Track during on-time after blank, hold during off-time
PWM via ENABLE; Mode = FAST decay	Track after blank; AIOUT proportional to load current only when V_{SENSE} > 0
PWM via PHASE (ENB = 1)	Track after blank; AIOUT proportional to load current only when V_{SENSE} > 0
Chopping by internal current control (VREF and RS)	Track after blank; Hold during off-time

Note: If ENABLE held low for 250 µs, AIOUT will be discharged to GND.

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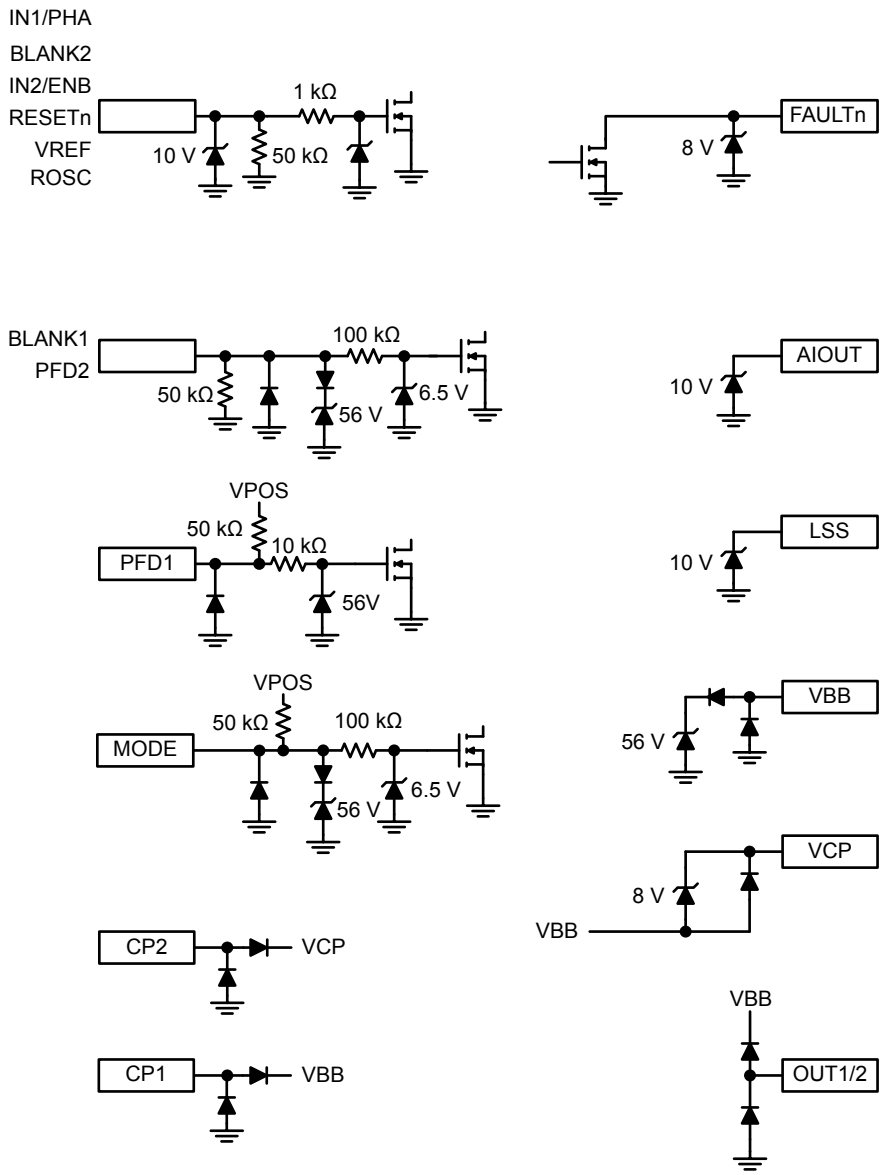
PIN DIAGRAMS



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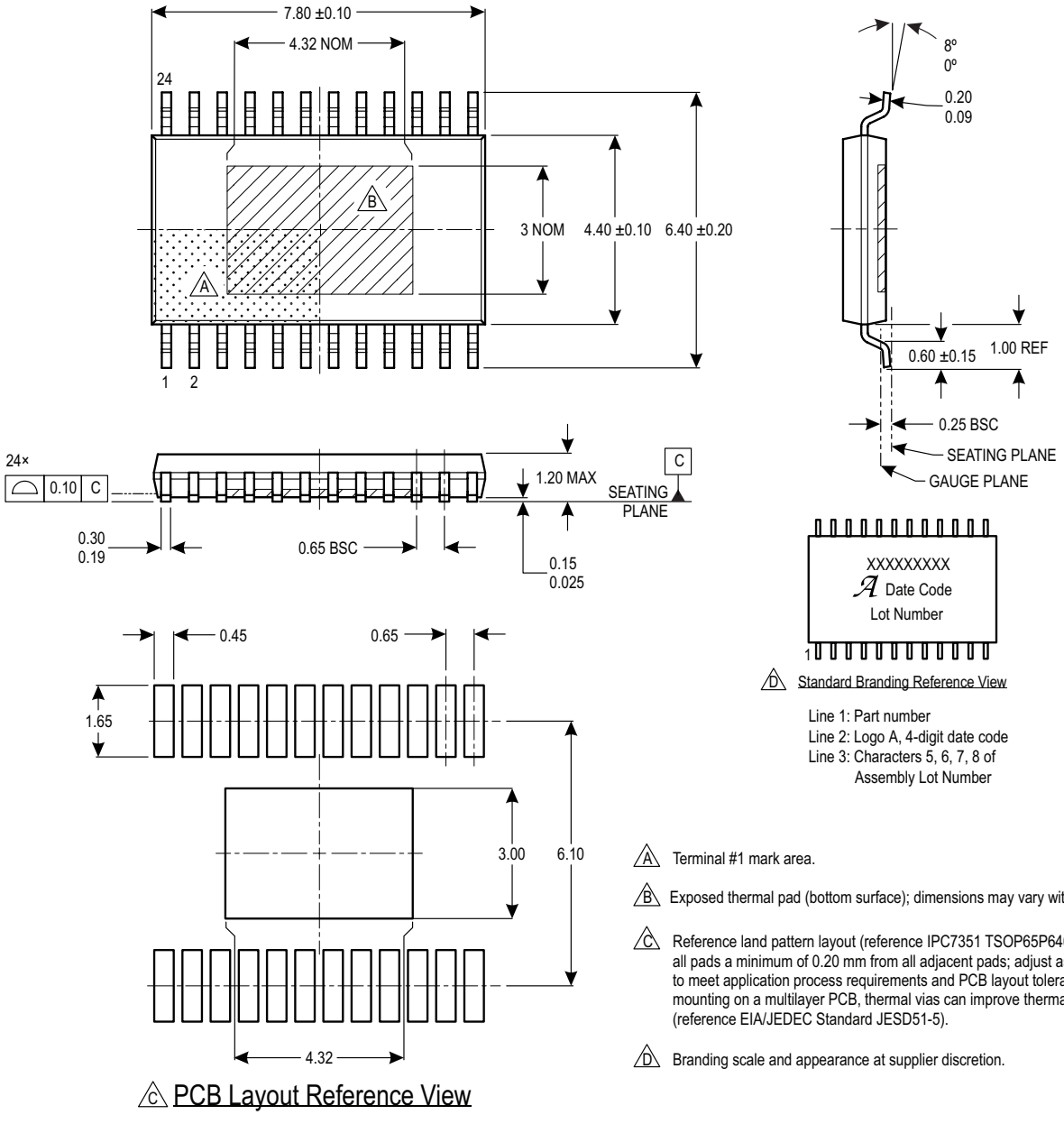
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use
(Reference Allegro DWG-0000379, Rev. 3 and JEDEC MO-153ADT)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



D Standard Branding Reference View

Line 1: Part number
Line 2: Logo A, 4-digit date code
Line 3: Characters 5, 6, 7, 8 of
Assembly Lot Number

C PCB Layout Reference View

A Terminal #1 mark area.

B Exposed thermal pad (bottom surface); dimensions may vary with device.

C Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5).

D Branding scale and appearance at supplier discretion.

LP Package, 24-Pin TSSOP with Exposed Thermal Pad

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Revision History

Number	Date	Description
–	July 13, 2021	Initial release
1	July 27, 2022	Updated package drawing (page 8)

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