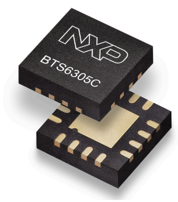
BTS6305C

High linearity pre-driver amplifier with differential input 4.4 GHz - 5 GHz

Rev. 7 — 15 June 2023 **Product data sheet**



1 General description

The BTS6305C is a high linearity, pre-driver amplifier with differential input for 5G massive MIMO infrastructure applications, with fast on-off switching to support TDD systems. The amplifier is designed to operate between 4.4 GHz and 5 GHz. The BTS6305C is housed in a 3 mm x 3 mm x 0.85 mm 16-terminal HVQFN package.

2 Features and benefits

- High saturated output power $P_{o(sat)}$ = 27.5 dBm
- High power-gain G_p = 35.5 dB
- High linearity performance ACLR = -42 dBc
- Unconditionally stable
- Fast switching to support TDD systems
- 5 V single supply, quiescent current 100 mA
- Small 16-terminal leadless package 3 mm x 3 mm x 0.85 mm
- ESD protection on all terminals
- Moisture sensitivity level 1

3 Applications

- Wireless infrastructure 5G NR mMIMO
- High linearity pre-driver
- TDD systems

4 Quick reference data

Table 1. Quick reference data

f = 4.4 GHz; V_{CC} = 5 V; T_{amb} = 25 °C; input 100 Ω, and output 50 Ω; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	ON state, P_o = 15 dBm	-	120	150	mA
		ON state, quiescent	-	100	125	mA
		OFF state	-	1.2	2.5	mA
G_p	power gain	On state	-	35.5	-	dB
		OFF state	-	-49	-	dB
$P_{o(sat)}$	saturated output power	[1]	-	27.5	-	dBm
ACLR	adjacent channel leakage ratio	CP-OFDM with 100 MHz channel BW, QPSK modulation, and 60 kHz SCS, fully allocated, P_o = 15 dBm	-	-42	-	dBc

[1] Connector and Printed-Circuit Board (PCB) losses have been de-embedded, 3 dB gain compression

5 Ordering information

Table 2. Ordering information

Type number	Orderable part number	Package		
		Name	Description	Version
BTS6305C	BTS6305CJ	HVQFN16	3 mm x 3 mm x 0.85 mm, 16 terminals no leads	SOT758-1

6 Marking

Table 3. Marking

Type number	Marking code
BTS6305C	35C

7 Functional diagram

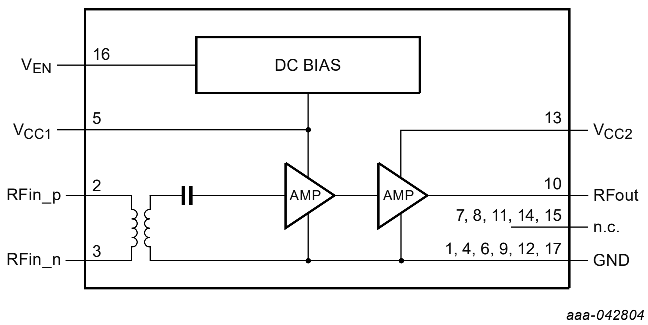


Figure 1. BTS6305C functional diagram

8 Pinning information

8.1 Pin diagram

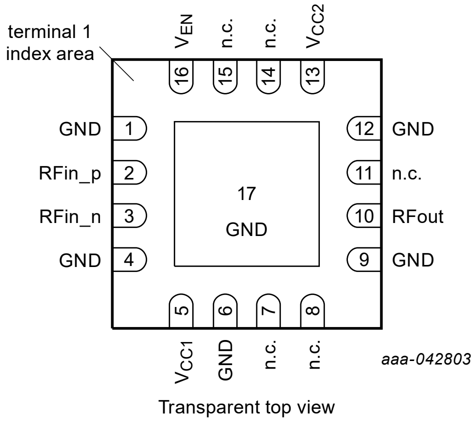


Figure 2. BTS6305C pin configuration

8.2 Pin description

Table 4. Pin description

Pin	Symbol	Description
1, 4, 6, 9,12, and 17	GND	PCB ground
2	RFin_p	RF input
3	RFin_n	RF input
5	V_{CC1}	supply voltage
7, 8, 11, 14, and 15	n.c. [1]	not connected
10	RFout	RF output
13	V_{CC2}	supply voltage
16	V_{EN}	voltage enable; LOW = OFF state; HIGH = ON state

[1] n.c. means that pin is not connected inside package, and may be left floating in application

9 Functional description

Table 5. Shutdown control

V_{en}	voltage applied at pin V_{en} [1]	State	Condition
LOW	$0 < V(V_{en}) < V_{IL(max)}$	OFF	bias active, amplifier not active
HIGH	$V_{IH(min)} < V(V_{en}) < V_{I(max)}$	ON	bias active, amplifier active

[1] V_{EN} can only be made HIGH, after supply voltage has been applied to pin V_{CC1}

10 Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.3	6	V
V_{EN}	enable voltage		-0.3	4	V
$P_{i(RF)CW}$	continuous waveform RF input power	ON state, OFF state	-	10	dBm
T_{stg}	storage temperature		-50	150	°C
T_j	junction temperature		-	175	°C
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM) According to ANSI/ESDA/JEDEC standard JS-001	-	+/-2	kV
		Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	-	+/-500	V

11 Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	[1]	4.75	5	5.25	V
V_{IL}	LOW-level input voltage		0	-	0.6	V
V_{IH}	HIGH-level input voltage		1.2	-	3.6	V
$V_{I(max)}$	maximum input voltage		-	-	3.6	V
Z_0	characteristic impedance differential input		-	100	-	Ω
	characteristic impedance output		-	50	-	Ω
T_{case}	case temperature		-40	-	120	°C

[1] supply voltage at V_{CC1} must be applied before, or at the same time as applying supply voltage to pin V_{CC2}

12 Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	junction to case thermal resistance	[1] [2]	50	K/W

[1] case is ground solder pad.

[2] Thermal resistance determined with device mounted, and device bottom case kept at constant temperature.

13 Characteristics

Table 9. Characteristics

V_{CC} = 5 V; T_{amb} = 25 °C; input 100 Ω, and output 50 Ω; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	ON state, P_o = 15 dBm, f = 4.4 GHz	-	120	150	mA
		ON state, quiescent	-	100	125	mA
		OFF state	-	1.2	2.5	mA
G_p	power gain	ON state				
		f = 4.4 GHz	32.5	35.5	38.5	dB
		f = 5 GHz	31	34	37	dB
		OFF state	-	-49	-	dB
G_{flat}	gain flatness	f = 4.4 GHz to 4.6 GHz	-	0.5	-	dB
		f = 4.6 GHz to 4.8 GHz	-	0.7	-	dB
		f = 4.8 GHz to 5 GHz	-	1.3	-	
$t_{d(grp)}$	group delay time	f = 4.4 GHz to 4.7 GHz	-	0.4	-	ns
		f = 4.7 GHz to 5 GHz	-	0.4	-	ns
$P_{o(sat)}$	saturated output power	f = 4.4 GHz [1]	-	27.5	-	dBm
		f = 5 GHz [1]	-	27.5	-	dBm
$P_{L(1dB)}$	output power at1 dB gain compression	f = 4.4 GHz	-	26.5	-	dBm
		f = 5 GHz	-	26.5	-	dBm
$IP3_o$	output third-order intercept point	2-tone; tone spacing = 100 MHz; P_o = 15 dBm, f = 4.4 GHz	-	36	-	dBm
CMRR	common mode rejection ratio	f = 4.4 GHz	-	20.5	-	dB
		f = 5 GHz	-	20	-	dB
RL_i	input return loss	f = 4.4 GHz	10	12.5	-	dB
		f = 5 GHz	9	11.5	-	dB
RL_o	output return loss	f = 4.4 GHz	10	17	-	dB
		f = 5 GHz	10	20	-	dB
ISL_r	reverse isolation		-	65	-	dB
NF	noise figure	f = 4.4 GHz [2]	-	4.5	-	dB
		f = 5 GHz [2]	-	4.5	-	dB
$t_{s(pon)}$	power-on settling time	$V_{EN}$from LOW to HIGH to gain settled within 0.1 dB of final value and phase settled to within 1 degree of final value	-	0.7	0.8	µs
$t_{s(poff)}$	power-off settling time	V_{EN} from HIGH to LOW to gain settled to be < 5 % of gain in ON state	-	0.05	0.1	µs
K	Rollett stability factor	1 MHz to 15 GHz	1.8	-	-	

Table 9. Characteristics*...continued*

V_{CC} = 5 V; T_{amb} = 25 °C; input 100 Ω, and output 50 Ω; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ACLR	adjacent channel leakage ratio	CP-OFDM with 100 MHz channel BW, QPSK modulation, and 60 kHz SCS, fully allocated, P_o = 15 dBm	-	-42	-	dBc

[1] Connector and Printed-Circuit Board (PCB) losses have been de-embedded, 3 dB gain compression

[2] Connector and Printed-Circuit Board (PCB) losses have been de-embedded.

14 Graphs

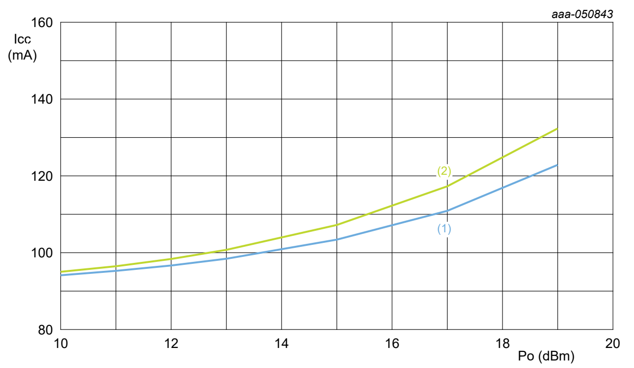


Figure 3. I_{cc} versus P_{out} over frequency at 25 °C

(1) f = 4.4 GHz

(2) f = 5 GHz

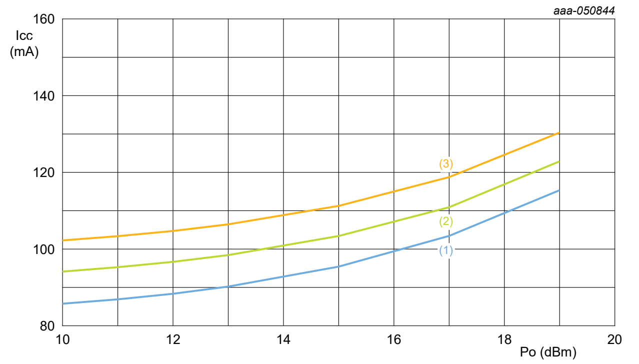


Figure 4. I_{cc} versus P_{out} over temperature at 4.4 GHz

(1) T_{case} = -40 °C

(2) T_{case} = 25 °C

(3) T_{case} = 115 °C

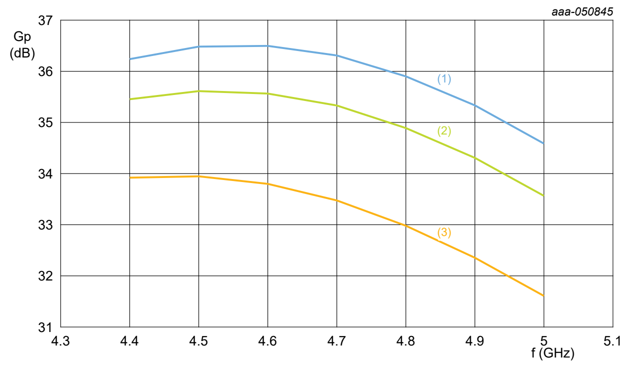


Figure 5. Gain versus frequency over temperature

(1) T_{case} = -40 °C

(2) T_{case} = 25 °C

(3) T_{case} = 115 °C

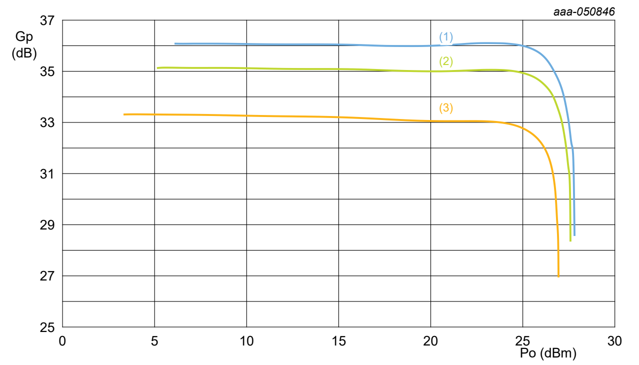


Figure 6. Gain versus P_{out} over temperature at 4.4 GHz

(1) T_{case} = -40 °C

(2) T_{case} = 25 °C

(3) T_{case} = 115 °C

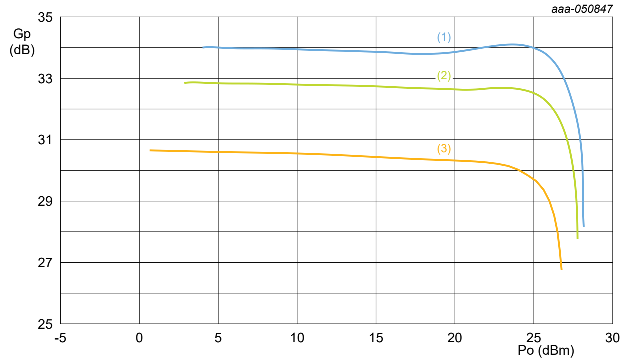


Figure 7. Gain versus P_{out} over temperature at 5 GHz

(1) T_{case} = -40 °C

(2) T_{case} = 25 °C

(3) T_{case} = 115 °C

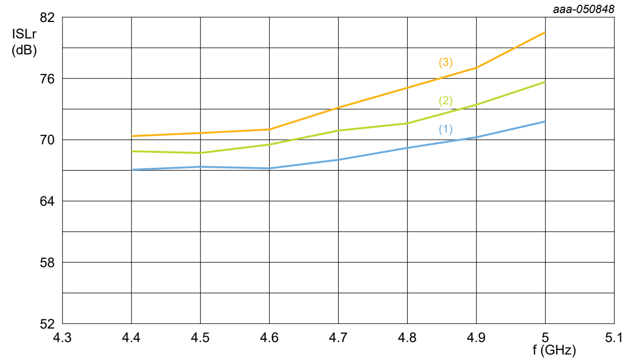


Figure 8. Isolation versus frequency over temperature

(1) T_{case} = -40 °C

(2) T_{case} = 25 °C

(3) T_{case} = 115 °C

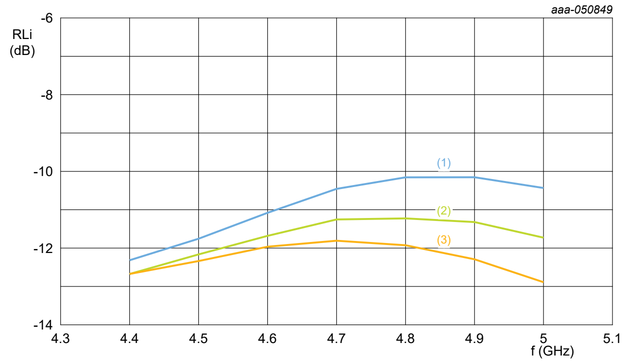


Figure 9. RL_i versus frequency over temperature

(1) T_{case} = -40 °C

(2) T_{case} = 25 °C

(3) T_{case} = 115 °C

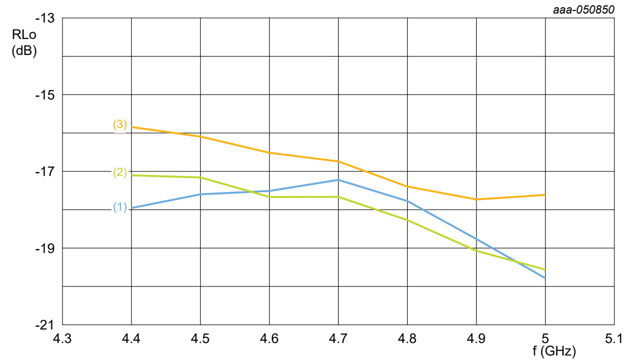


Figure 10. RL_o versus frequency over temperature

(1) T_{case} = -40 °C

(2) T_{case} = 25 °C

(3) T_{case} = 115 °C

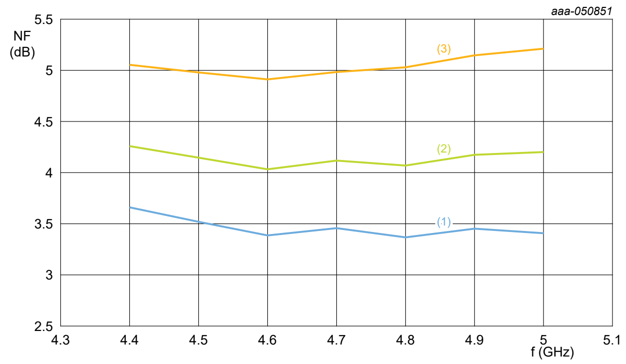


Figure 11. NF versus frequency over temperature

(1) T_{case} = -40 °C

(2) T_{case} = 25 °C

(3) T_{case} = 115 °C

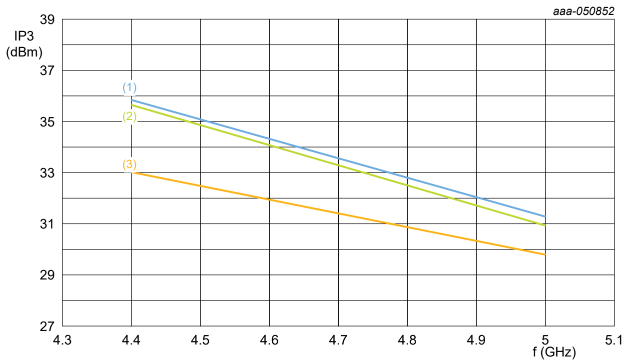


Figure 12. IP_3 versus frequency over temperature

(1) T_{case} = -40 °C

(2) T_{case} = 25 °C

(3) T_{case} = 115 °C

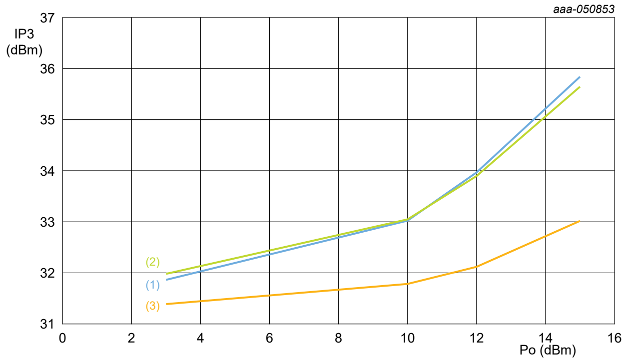


Figure 13. IP3 versus P_{out} over temperature at 4.4 GHz

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 115 °C

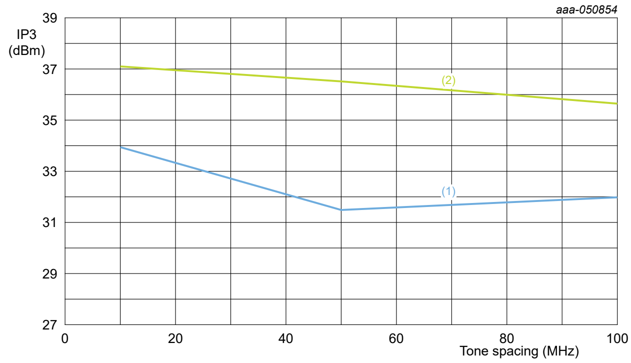


Figure 14. IP3 versus Tone spacing over P_{out}

(1) P_o = 3dBm
(2) P_o = 15 dBm

15 Application information

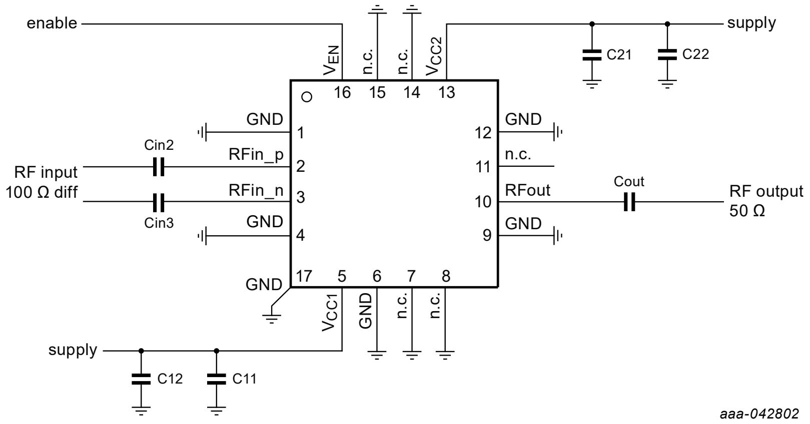


Figure 15. BTS6305Cschematic of application board

Note: *pins n.c. (not connected) may be left floating*

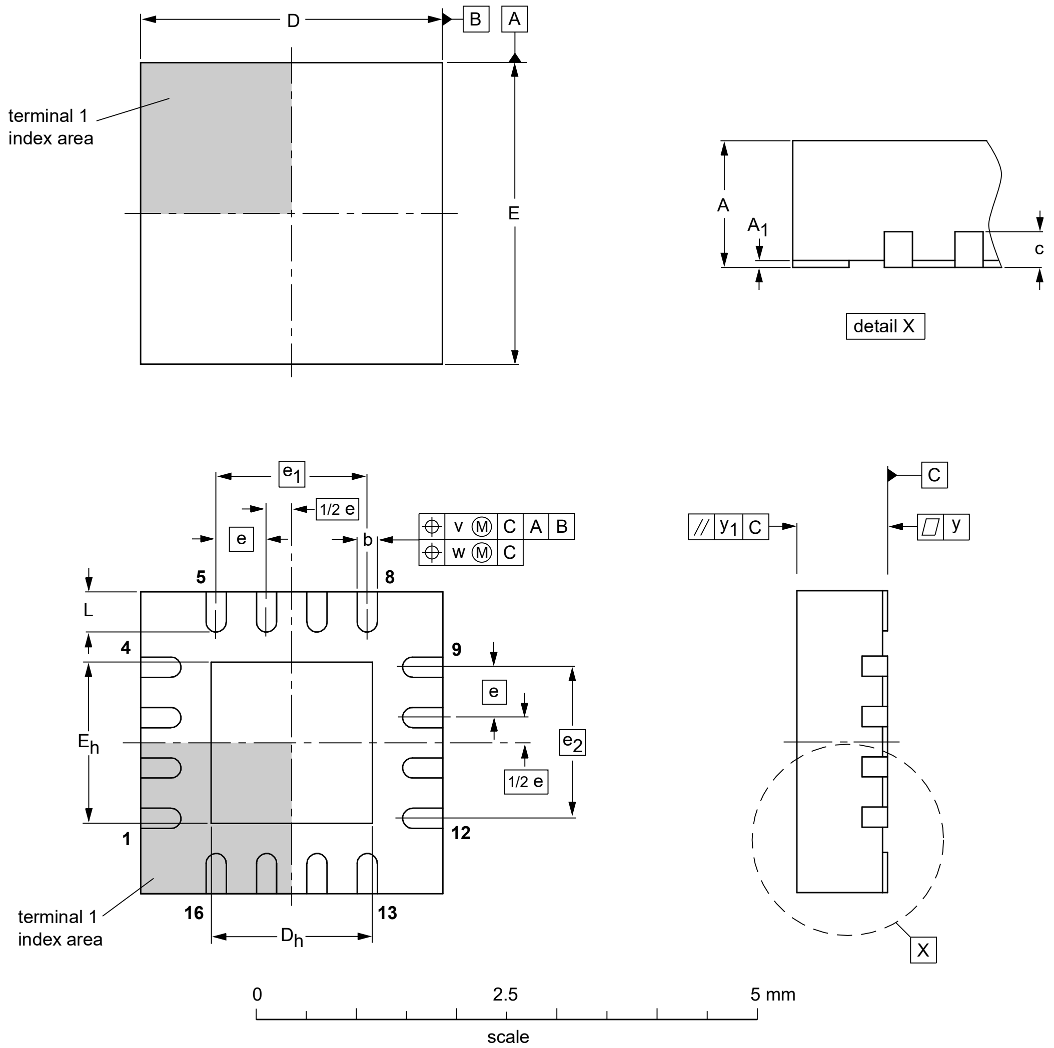
Table 10. List of components

See Figure 15 for schematics.

Component	Description	Value	Remarks
Cin2, and Cin3	capacitor	18 pF	in a 50 Ω PCB track
C_{out}	capacitor	3.9 pF	in a 50 Ω PCB track
C11, and C21	capacitor	10 nF	recommended
C12, and C22	capacitor	1 µF	optional

16 Package outline

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.85 mm **SOT758-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.75 1.45	3.1 2.9	1.75 1.45	0.5	1.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

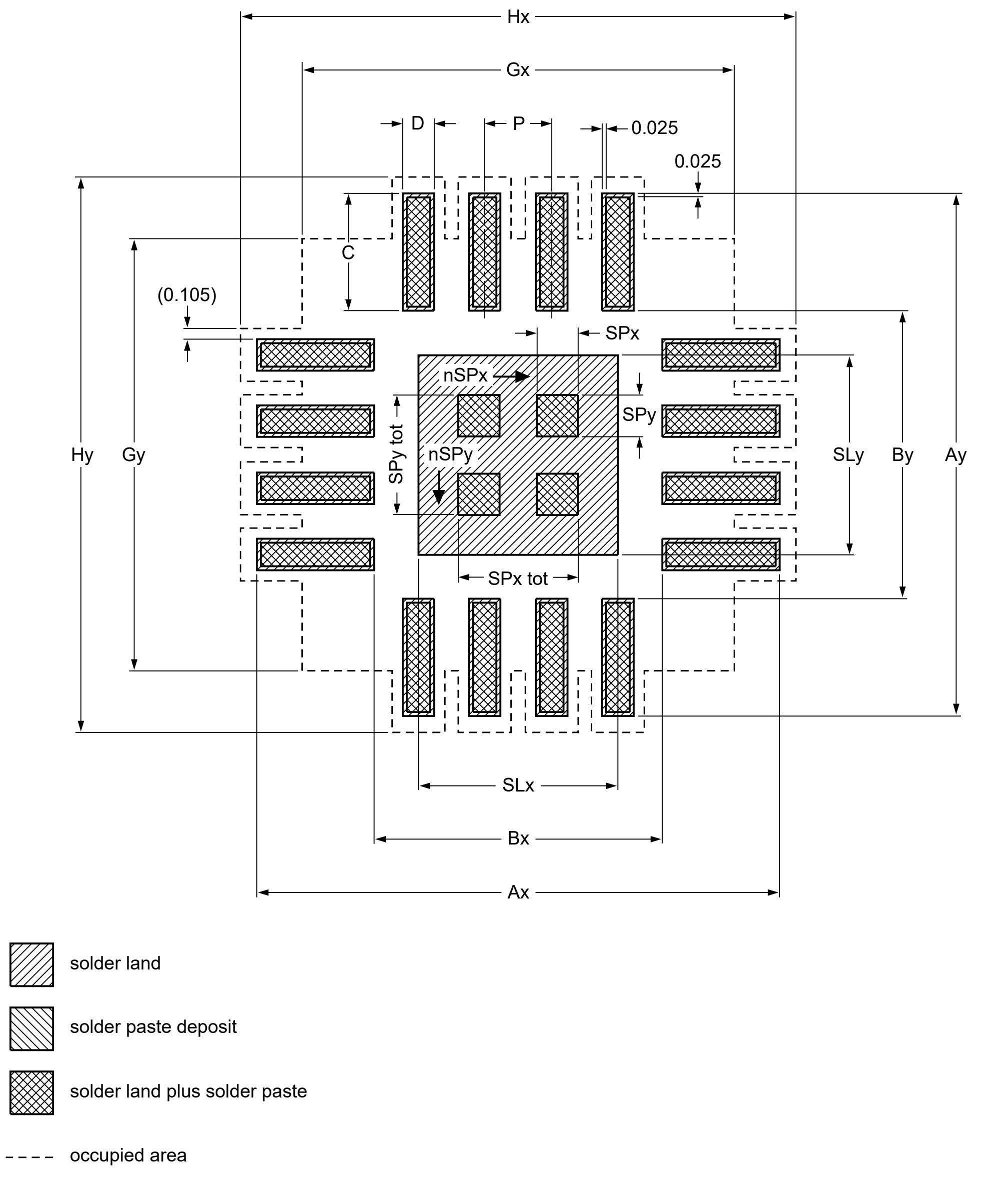
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT758-1	- - -	MO-220	- - -			~~02-03-25~~ 02-10-21

Figure 16. Package outline SOT758-1 (HVQFN16)

16.1 Footprint and solder information

Footprint information for reflow soldering of HVQFN16 package **SOT758-1**



nSPx	nSPy
2	2

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.50	4.00	4.00	2.20	2.20	0.90	0.24	1.50	1.50	0.90	0.90	0.30	0.30	3.30	3.30	4.25	4.25

Issue date ~~12-03-07~~ 12-03-08

sot758-1_fr

Figure 17. Footprint information

17 Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.
Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

18 Abbreviations

Table 11. Abbreviations

Acronym	Description
5G NR	5th generation new radio
ACLR	adjacent channel leakage ratio
CP-OFDM	cyclic prefix orthogonal frequency division multiplexing
CMMR	common mode rejection ratio
ESD	electrostatic discharge
mMIMO	massive multiple-input multiple-output
PA	power amplifier
RF	radio frequency
TDD	time-division duplexing

19 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BTS6305C v.7	20230615	Product data sheet	-	BTS6305C v.6
modification	• Changed max case temperature from 115^{o}C to 120^{o}C			
BTS6305C v.6	20230323	Product data sheet	-	BTS6305C v.5
modification	• updated table 10 List of components			
BTS6305C v.5	20230323	Product data sheet	-	BTS6305C v.4
modification	• updated table 1 quick reference data • updated figure 2 pin configuration • updated table 9 characteristics • updated table 4 pin description • updated figure 15 application board			

20 Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Contents

Date of release: 15 June 2023