BTS6305U

High linearity pre-driver amplifier with differential input 2.3 GHz - 4.2 GHz

Rev. 9 — 15 June 2023 Product data sheet

1 General description

The BTS6305U is a wideband high linearity pre-driver amplifier with differential input 2.3 GHz - 4.2 GHz for 5G massive MIMO infrastructure applications, with fast on-off switching to support TDD systems. The amplifier is designed to operate between 2.3 GHz and 4.2 GHz. The BTS6305U is housed in a 3 mm x 3 mm x 0.85 mm 16-terminal HVQFN package.

2 Features and benefits

- High saturated output power $P_{o(sat)}$ = 29 dBm
- High power-gain G_p = 39.5 dB
- High linearity performance ACLR = -42 dBc
- Unconditionally stable
- Fast switching to support TDD systems
- 5 V single supply, quiescent current 100 mA
- Small 16-terminal leadless package 3 mm x 3 mm x 0.85 mm
- ESD protection on all terminals
- Moisture sensitivity level 1

3 Applications

- Wireless infrastructure 5G NR mMIMO
- High linearity pre-driver
- TDD systems

4 Quick reference data

Table 1. Quick reference data

f = 3.5 GHz; V_{CC} = 5 V; T_{amb} = 25 °C; input 100 Ω, and output 50 Ω; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	ON state, P_o = 15 dBm	-	122	150	mA
		ON state, quiescent	-	100	125	mA
		OFF state	-	1.2	2.5	mA
G_p	power gain	On state	37	39.5	42	dB
		OFF state	-	-49	-47	dB
$P_{o(sat)}$	saturated output power	[1]	26	29	-	dBm
ACLR	adjacent channel leakage ratio	CP-OFDM with 100 MHz channel BW, QPSK modulation, and 60 kHz SCS, fully allocated, P_o = 15 dBm	-	-42	-	dBc

[1] Connector and Printed-Circuit Board (PCB) losses have been de-embedded, 3 dB gain compression

5 Ordering information

Table 2. Ordering information

Type number	Orderable part number	Package		
		Name	Description	Version
BTS6305U	BTS6305UJ	HVQFN16	3 mm x 3 mm x 0.85 mm, 16 terminals no leads	SOT758-1

6 Marking

Table 3. Marking

Type number	Marking code
BTS6305U	35U

7 Functional diagram

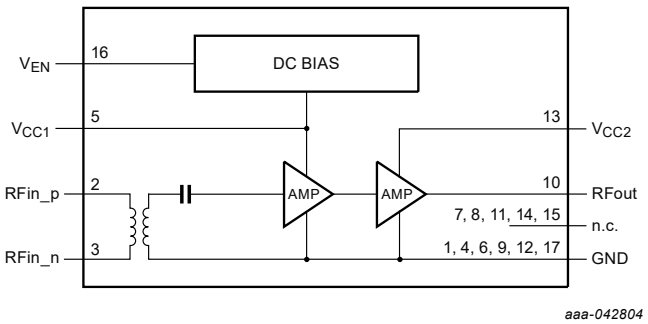
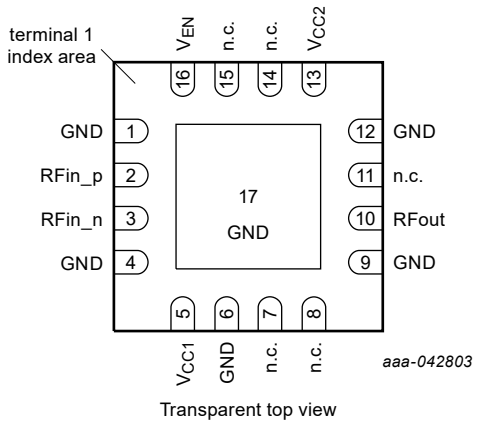


Figure 1. BTS6305U functional drawing

8 Pinning information

8.1 Pin diagram



Transparent top view

Figure 2. Pin configuration

8.2 Pin description

Table 4. Pin description

Pin	Symbol	Description
1, 4, 6, 9,12, and 17	GND	PCB ground
2	RFin_p	RF input
3	RFin_n	RF input
5	V_{CC1}	supply voltage
7, 8, 11, 14, and 15	n.c. [1]	not connected
10	RF_{out}	RF output
13	V_{CC2}	supply voltage
16	V_{EN}	voltage enable; LOW = OFF state; HIGH = ON state

[1] n.c. means that pin is not connected inside package, and may be left floating in application

9 Functional description

Table 5. Shutdown control

V_{en}	voltage applied at pin V_{en} [1]	State	Condition
LOW	$0 < V(V_{en}) < V_{IL(max)}$	OFF	bias active, amplifier not active
HIGH	$V_{IH(min)} < V(V_{en}) < V_{I(max)}$	ON	bias active, amplifier active

[1] V_{EN} can only be made HIGH, after supply voltage has been applied to pin V_{CC1}

10 Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.3	6	V
V_{EN}	enable voltage		-0.3	4	V
$P_{i(RF)CW}$	continuous waveform RF input power	ON state, OFF state	-	10	dBm
T_{stg}	storage temperature		-50	150	°C
T_j	junction temperature		-	175	°C
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM) According to ANSI/ESDA/JEDEC standard JS-001	-	+/-2	kV
		Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	-	+/-500	V

11 Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	[1]	4.75	5	5.25	V
V_{IL}	LOW-level input voltage		0	-	0.6	V
V_{IH}	HIGH-level input voltage		1.2	-	3.6	V
$V_{I(max)}$	maximum input voltage		-	-	3.6	V
Z_0	characteristic impedance differential input		-	100	-	Ω
	characteristic impedance output		-	50	-	Ω
T_{case}	case temperature		-40	-	120	°C

[1] supply voltage at V_{CC1} must be applied before, or at the same time as applying supply voltage to pin V_{CC2}

12 Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}case)}$	junction to case thermal resistance	[1] [2]	50	K/W

[1] case is ground solder pad
[2] thermal resistance determined with device mounted, and device bottom case kept at constant temperature

13 Characteristics

Table 9. Characteristics

V_{CC} = 5 V; T_{amb} = 25 °C; input 100 Ω, and output 50 Ω; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	ON state, P_o = 15 dBm	-	122	150	mA
		ON state, quiescent	-	100	125	mA
		OFF state	-	1.2	2.5	mA
G_p	power gain	ON state				
		f = 2.6 GHz,	36	38.5	41	dB
		f = 3.5 GHz,	37	39.5	42	dB
		f = 4.2 GHz,	34	36.5	39	dB
		OFF state	-	-49	-47	dB
G_{flat}	gain flatness	f = 2.4 GHz to 2.7 GHz	-	1.4	-	dB
		f = 3.3 GHz to 3.8 GHz	-	1.3	-	dB
		f = 3.8 GHz to 4.2 GHz	-	1.9	-	dB
$t_{d(grp)}$	group delay time	f = 2.4 GHz to 2.7 GHz	-	0.4	0.5	ns
		f = 3.3 GHz to 3.8 GHz	-	0.4	0.5	ns
		f = 3.8 GHz to 4.2 GHz	-	0.4	0.5	ns
$P_{o(sat)}$	saturated output power	f = 2.6 GHz [1]	-	29	-	dBm
		f = 3.5 GHz [1]	26	29	-	dBm
		f = 4.2 GHz [1]	-	28.5	-	dBm
$P_{L(1dB)}$	output power at1 dB gain compression	f = 2.6 GHz	-	28	-	dBm
		f = 3.5 GHz	-	28.5	-	dBm
		f = 4.2 GHz	-	27.5	-	dBm
$IP3_o$	output third-order intercept point	2-tone; tone spacing = 100 MHz; P_o = 15 dBm	-	33	-	dBm
CMRR	common mode rejection ratio	f = 2.6 GHz	22	28	-	dB
		f = 3.5 GHz	22	31	-	dB
		f = 4.2 GHz	22	31.5	-	dB
RL_i	input return loss	f = 2.6 GHz	10	13	-	dB
		f = 3.5 GHz	10	13.5	-	dB
		f = 4.2 GHz	10	14	-	dB
RL_o	output return loss	f = 2.6 GHz	10	21	-	dB
		f = 3.5 GHz	10	14	-	dB
		f = 4.2 GHz	10	15	-	dB
ISL_r	reverse isolation		-	80	-	dB

Table 9. Characteristics...*continued*

V_{CC} = 5 V; T_{amb} = 25 °C; input 100 Ω, and output 50 Ω; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
NF	noise figure	f = 2.6 GHz [2]	-	4	-	dB
		f = 3.5 GHz [2]	-	4	-	dB
		f = 4.2 GHz [2]	-	3.5	-	dB
$t_{s(pon)}$	power-on settling time	V_{EN} from LOW to HIGH to gain settled within 0.1 dB of final value and phase settled to within 1 degree of final value	-	0.7	0.8	µs
$t_{s(poff)}$	power-off settling time	V_{EN} from HIGH to LOW to gain settled to be < 5 % of gain in ON state	-	0.05	0.1	µs
K	Rollett stability factor	1 MHz to 15 GHz	1.8	-	-	
ACLR	adjacent channel leakage ratio	CP-OFDM with 100 MHz channel BW, QPSK modulation, and 60 kHz SCS, fully allocated, P_o = 15 dBm	-	-42	-	dBc

[1] Connector and Printed-Circuit Board (PCB) losses have been de-embedded, 3 dB gain compression
[2] Connector and Printed-Circuit Board (PCB) losses have been de-embedded.

14 Graphs

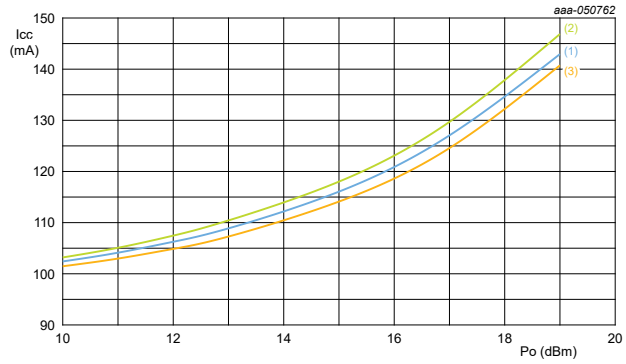


Figure 3. I_{cc} versus P_{out} over frequency at 25 °C

(1) f = 2.6 GHz
(2) f = 3.5 GHz
(3) f = 4.2 GHz

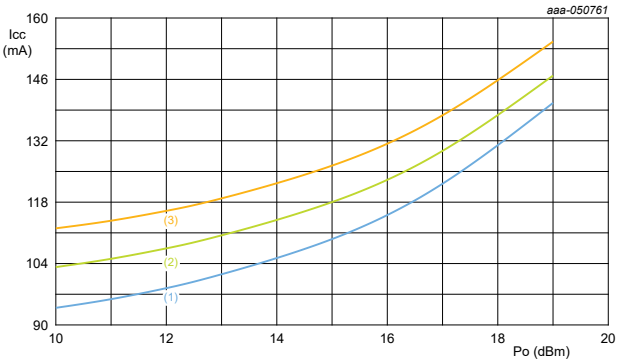


Figure 4. I_{cc} versus P_{out} over temperature at 3.5 GHz

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 115 °C

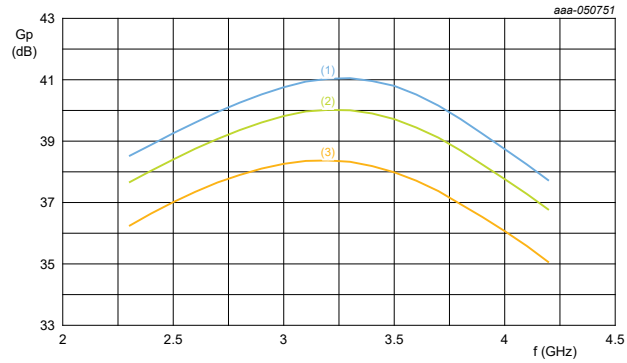


Figure 5. Gain versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 115 °C

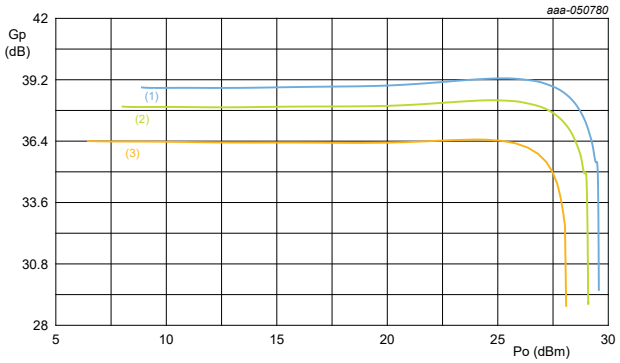


Figure 6. Gain versus P_{out} over temperature at 2.6 GHz

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 115 °C

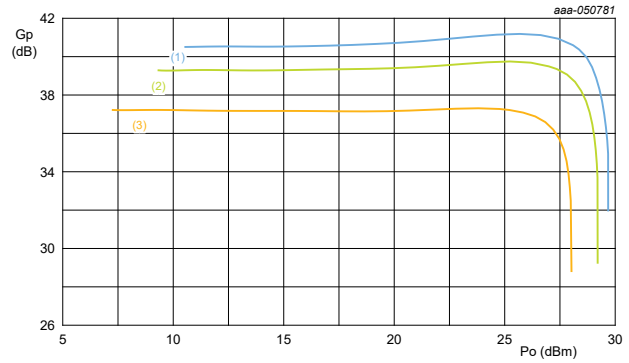


Figure 7. Gain versus P_{out} over temperature at 3.5 GHz

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 115 °C

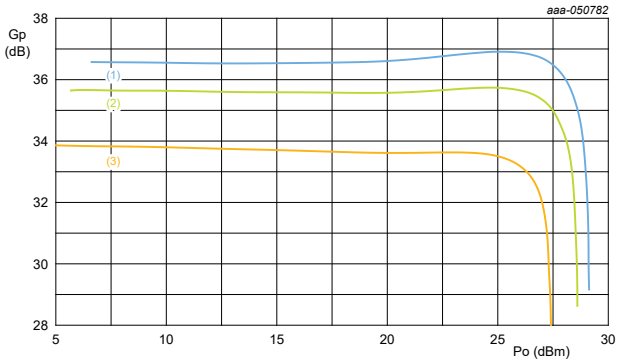


Figure 8. Gain versus P_{out} over temperature at 4.2 GHz

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 115 °C

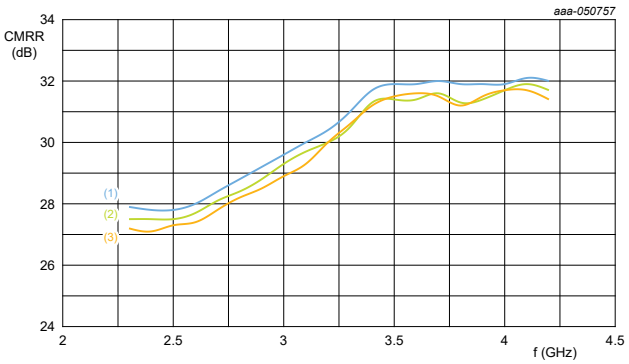


Figure 9. CMRR versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 115 °C

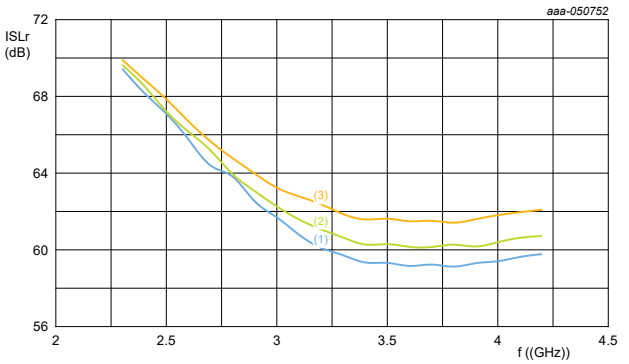


Figure 10. Isolation versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 115 °C

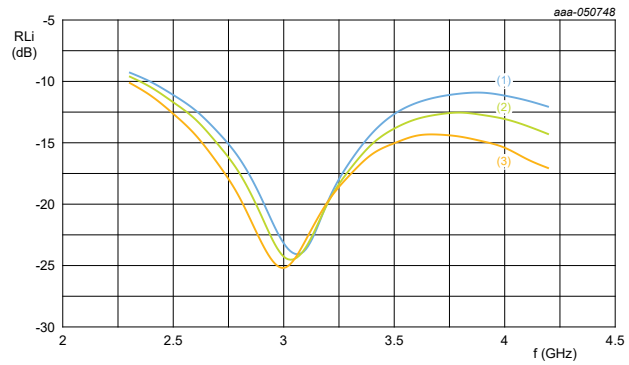


Figure 11. S_{11} versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 115 °C

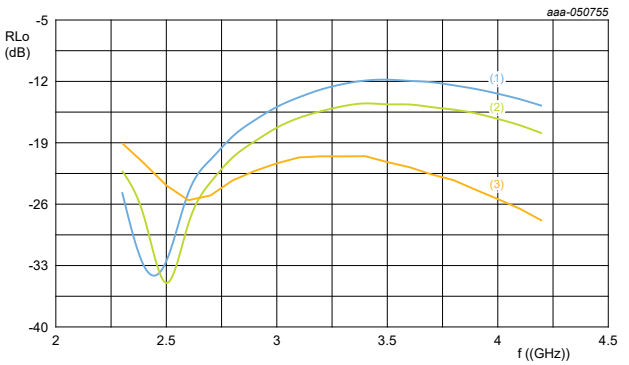


Figure 12. S_{22} versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 115 °C

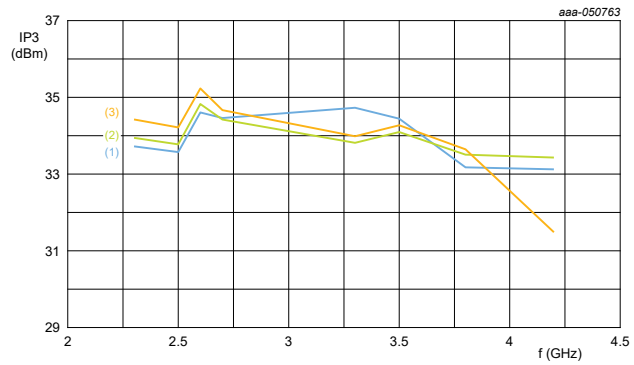


Figure 13. IP3 versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 115 °C

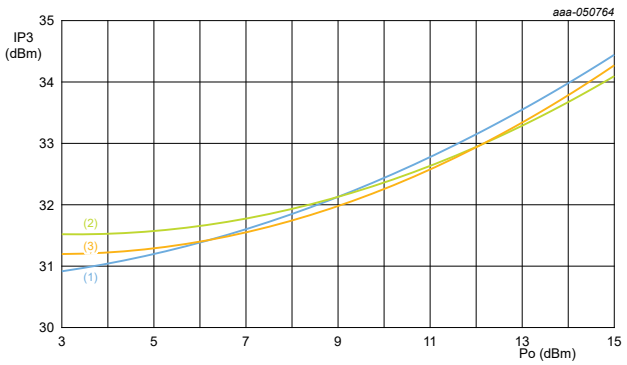


Figure 14. IP3 versus P_{out} over temperature at 3.5 GHz

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 115 °C

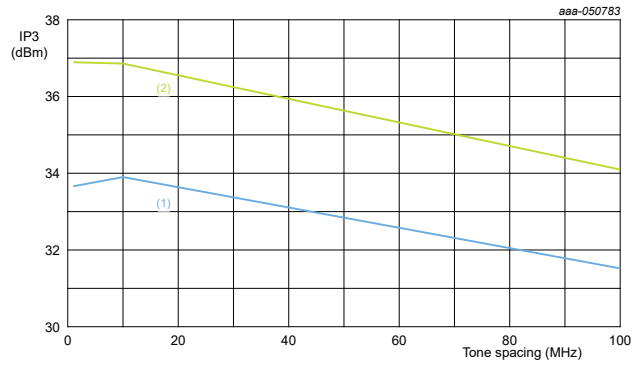


Figure 15. IP3 versus tone spacing over P_{out}

(1) Po = 3 dBm
(2) Po = 15 dBm

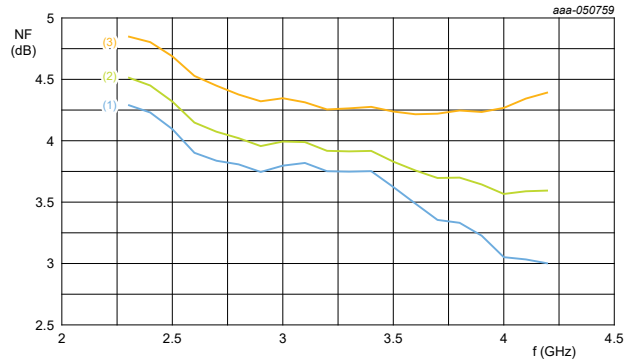


Figure 16. NF versus frequency over temperature

(1) T_{case} = -40 °C
(2) T_{case} = 25 °C
(3) T_{case} = 115 °C

15 Application information

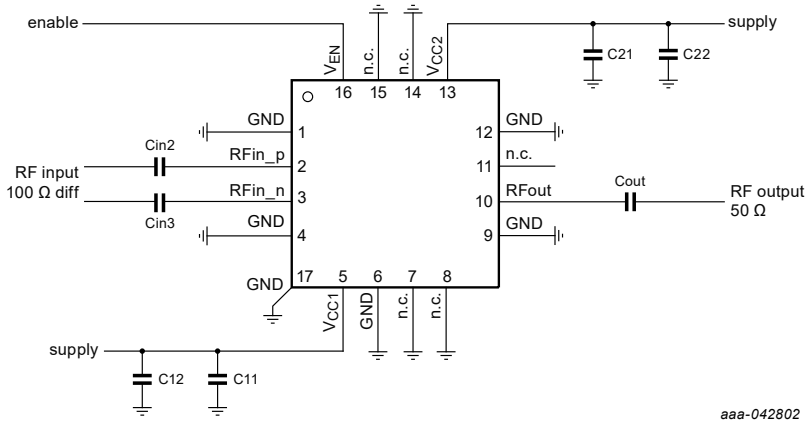


Figure 17. BTS6305U schematic of application board

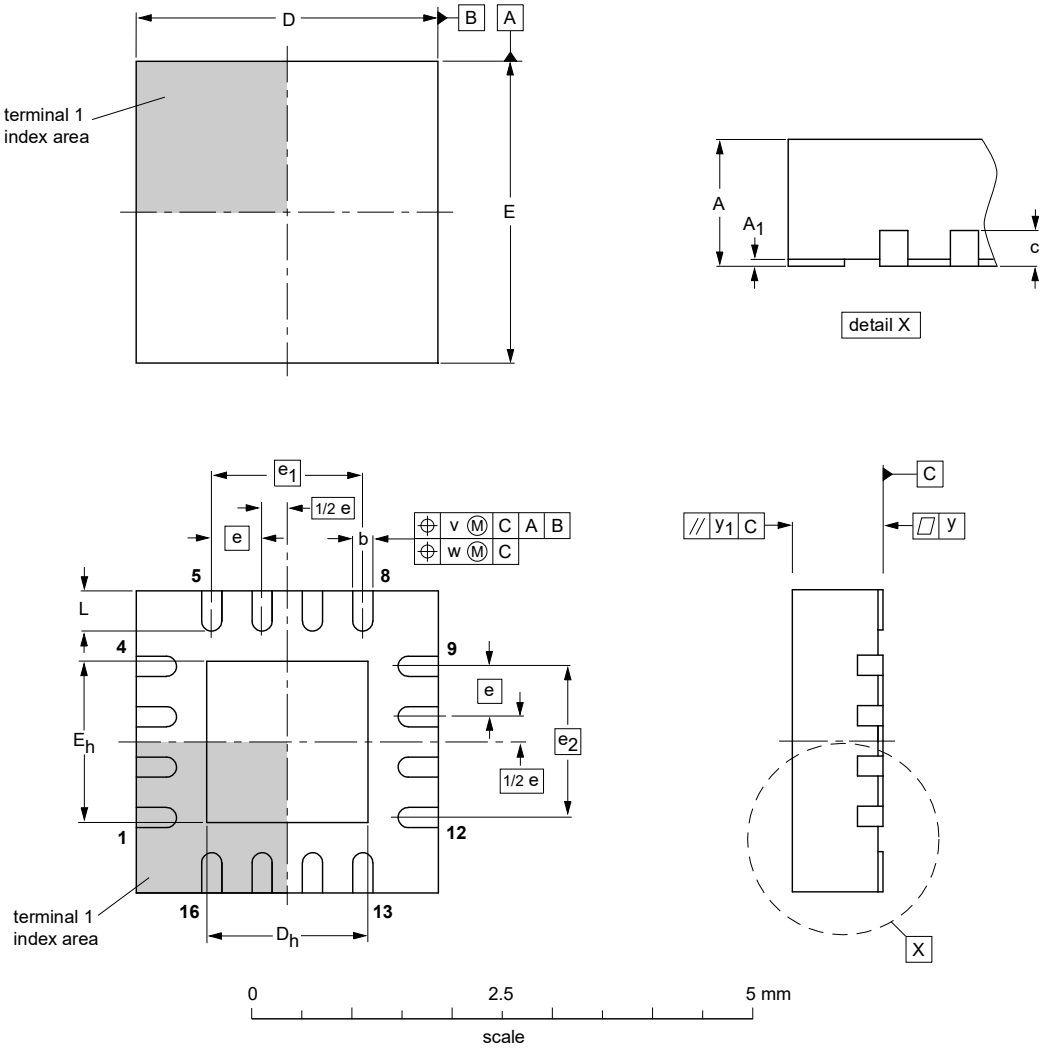
Note: *pins n.c. (not connected) may be left floating*

Table 10. List of components

Component	Description	Value	Remarks
Cin2, and Cin3	capacitor	18 pF	in a 50 Ω PCB track
C_{out}	capacitor	3.9 pF	in a 50 Ω PCB track
C11, and C21	capacitor	10 nF	recommended
C12, and C22	capacitor	1 µF	optional

16 Package outline

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.85 mm **SOT758-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.75 1.45	3.1 2.9	1.75 1.45	0.5	1.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

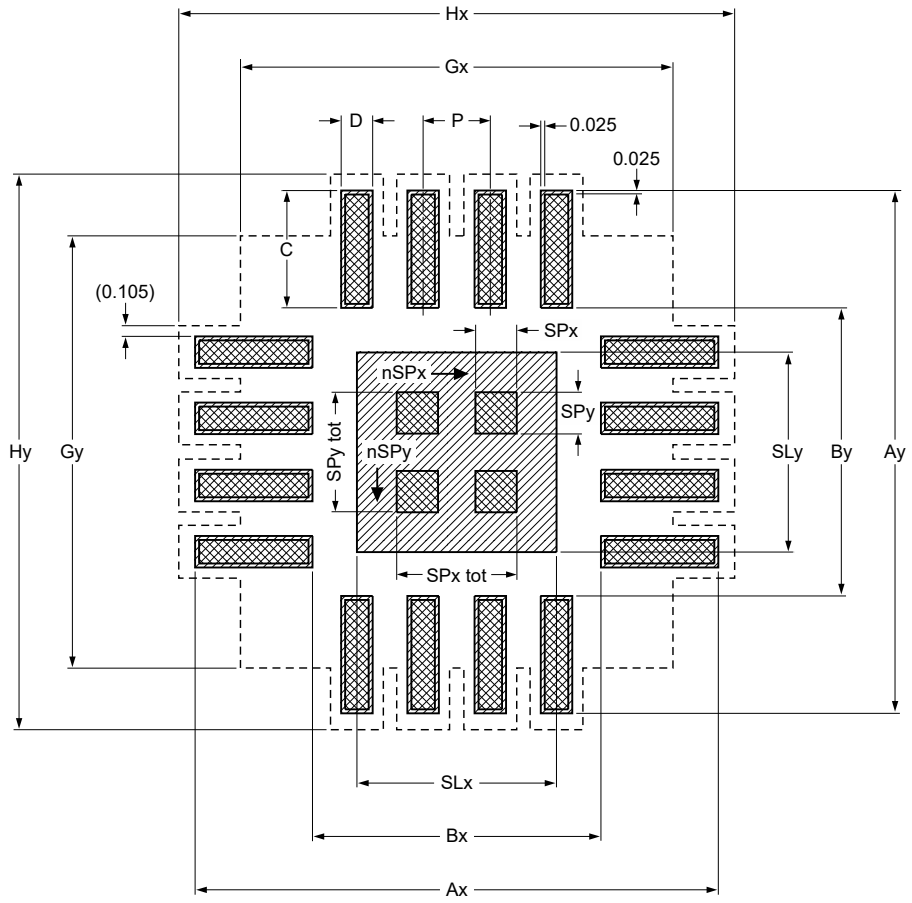
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT758-1	- - -	MO-220	- - -			~~02-03-25~~ 02-10-21

Figure 18. Package outline SOT758-1 (HVQFN16)

16.1 Footprint and solder information

Footprint information for reflow soldering of HVQFN16 package **SOT758-1**



solder land

solder paste deposit

solder land plus solder paste

occupied area

nSPx	nSPy
2	2

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.50	4.00	4.00	2.20	2.20	0.90	0.24	1.50	1.50	0.90	0.90	0.30	0.30	3.30	3.30	4.25	4.25

Issue date ~~12-03-07~~ 12-03-08 *sot758-1_fr*

Figure 19. Footprint information

17 Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

18 Abbreviations

Table 11. Abbreviations

Acronym	Description
5G NR	5th generation new radio
ACLR	adjacent channel leakage ratio
CP-OFDM	cyclic prefix orthogonal frequency division multiplexing
CMMR	common mode rejection ratio
ESD	electrostatic discharge
mMIMO	massive multiple-input multiple-output
PA	power amplifier
RF	radio frequency
TDD	time-division duplexing

19 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BTS6305U v.9	20230615	Product data sheet	-	BTS6305U v.8
modification	• Changed max case temperature from 115^{o}C to 120^{o}C			
BTS6305U v.8	20230321	Product data sheet	-	BTS6305U v.7
modification	• Updated table 4 pin description			
BTS6305U v.7	20230315	Product data sheet	-	BTS6305U v.6
modification	• Updated min value storage temperature			
BTS6305U v.6	20230310	Product data sheet	-	BTS6305U v.5
modification	• Updated graphs			

20 Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

20.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

20.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

20.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Contents

For more information, please visit: http://www.nxp.com

Date of release: 15 June 2023
Document number: