nanoANQ EM ER

1.2

NA-18-0371-0008

Document Information

Document Title:	nanoANQ EM ER
Document Version:	1.2
Current Date:	2021-10-26
Print Date:	2021-10-26
Document ID:	NA-18-0371-0008
Document Author:	MBO

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1. Introduction

The *nanoANQ EM ER* (Embedded Enhanced Resolution) acts as an anchor in Nanotron's UWB Real Time Locating System (RTLS).

The module can be integrated into any communication substation by interfacing directly with an Ethernet MAC or PHY via MII/RMII. It precisely detects the time of arrival (ToA) and deduces a peseudo received signal strength (RSSI) of tag blinks required for TDOA location applications. The module is able to range with other embedded anchor modules to automatically determine anchor separation distances – a key capability to enable automatic system set-up and maintenance.

Together with nanoLOC-based tags and nanotron's Location Server, the embedded anchor module forms the basis for high throughput tracking and monitoring applications in harsh environments. The credit card size design supports any UWB antenna through its U.FL connectors. There is one connector for each of the two independent radio channels.

Through its Ethernet port that could be used in either MII or RMII mode the module utilizes IP-based data and management protocols and features a built-in DHCP client. Thus it can be configured remotely through its API over the network.

Bidirectional payload exchange between the Location Server and individual tags is supported over the air.

To be compliant to national regulations, the output power is adjustable from −35 dBm /MHz to -62 dBm / MHz.

Via Ethernet MAC interface the Embedded Anchor Module can communicate with peripherals designed by the user.

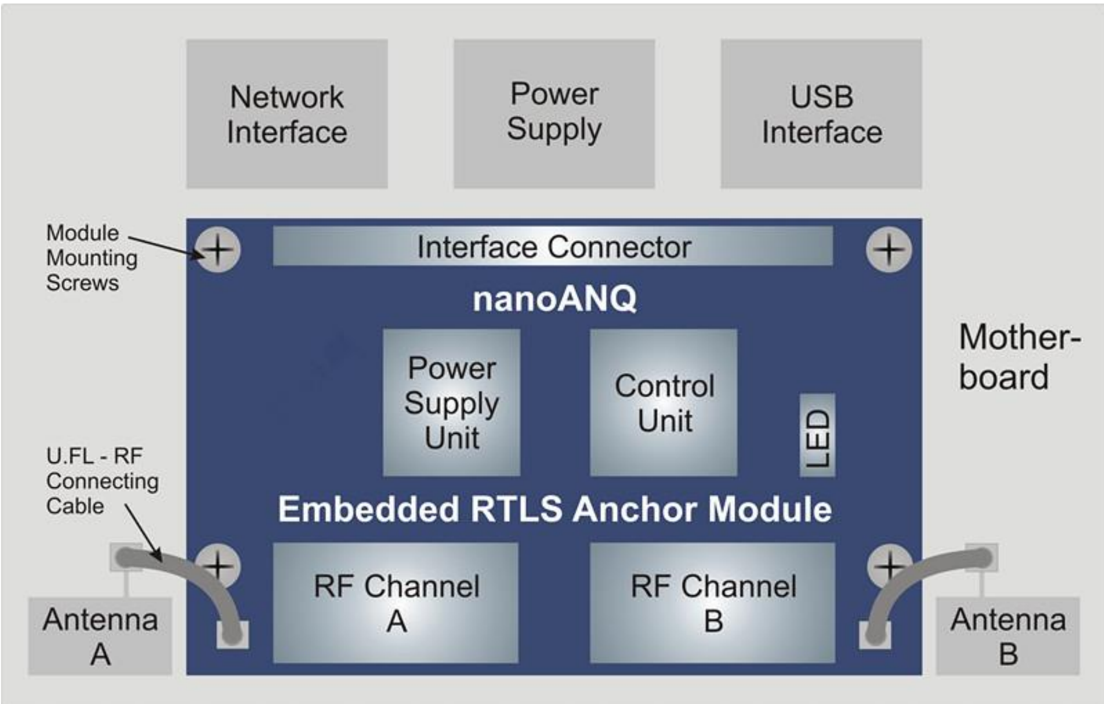

Figure 1-1: Block diagram of nanoANQ EM ER on motherboard

2. Features

Key Frequency Bands.. 6 bands with center frequencies from 3.5 to 6.5 GHz

Radio Data Rates.. 110 Kbps, 850 Kbps, 6.8 Mbps

Transmit power density adjustable... −35 dBm /MHz to -62 dBm / MHz

RF sensitivity @ 110 Kbps..-96 dBm typ. *

RF sensitivity @ 6.8 Mbps .... -84 dBm typ. *

RF interface ....50 Ohm RF Port

RF interface ....2 U-FL connectors

Data interface... Ethernet MAC interface, MII or RMII mode
....USB, full speed 12 Mbit/s,
....4 General purpose outputs
....4 General purpose inputs
....2 Transmitting indicator for RF channels
....Digital voltage reference output

Supply voltage .... +3.0 V ± 0.1 V

Maximum supply voltage ripple...20 mVpp

Current consumption..0.35 A average current measured with firmware 1.0.2-rc10

Power consumption ....1.16 W 600 mW average power consumption measured with firmware 1.0.2-rc10

Connectors ....1 Pin connector 2 x 30 pins, spacing 2mm

Operating temperature...-30°C to +85°C

Dimensions ....85.6 mm x 54.0 mm x 8.8 mm

Weight...18 g
* mode dependent

3. Functional Description

3.1. Dual Channel Core Locating Unit

The core locating unit consists of two independent RF channels and the control unit. It captures incoming UWB tag broadcasts and determines their time of arrival (ToA).

3.2. Antenna Connectors

Each of the two RF channels features an U.FL connector to allow any other external antenna connector to be used with the Embedded Anchor Module.

3.3. Interface Connector

Except for the antennas all signals including power supply are connected through a 2 x 30 pole connector with 2 mm spacing. In this document it is referred to as Interface Connector.

3.4. Status LEDs

Four onboard Status LEDs are used to signal different operation modes of the Embedded Anchor Module such as transmit or receive. The assignment of the LEDs to certain operating states is done by software (cf. nanoANQ EM User Guide). For placement of LED1...LED4 see Figure 1-1.

3.5. Power Supply and Clock Sources

A single 3.3V supply voltage is required to operate the Embedded Anchor Module. All other supply voltages required are derived internally from the power supply unit. All clocks are generated on board. Only the Ethernet network interface uses an external clock signal.

However to get the required performance nanotron recommends to observe following rules:

- Supply Voltage 3.3V ± 0.1V
- Generate the supply voltage as short as possible to the pins 59 and 60 of the header connector X5
- Ensure a good connection between the grounds of the nanoANQ EM ER and the host board. Use all ground pins of the header connector X5 and the 4 mounting holes
- Use an LDO to generate the 3.3 V, follow the design recommendations of the LDO manufacturer, use an output capacitor with high capacity (i.e. 22uF)
- Maximum ripple voltage: 40 mVss
- The average current of the nanoANQ EM ER is typical 350 mA
- The LDO should have a minimum current output capability of 500mA and be able to handle the power dissipation
- Don’t use the 3.3 V to feed other circuities on a host board
- Use a higher input voltage(i.e. 5 V) for the host board, take all needed supply voltages (Ethernet PHY, Oscillator, …) from this voltage

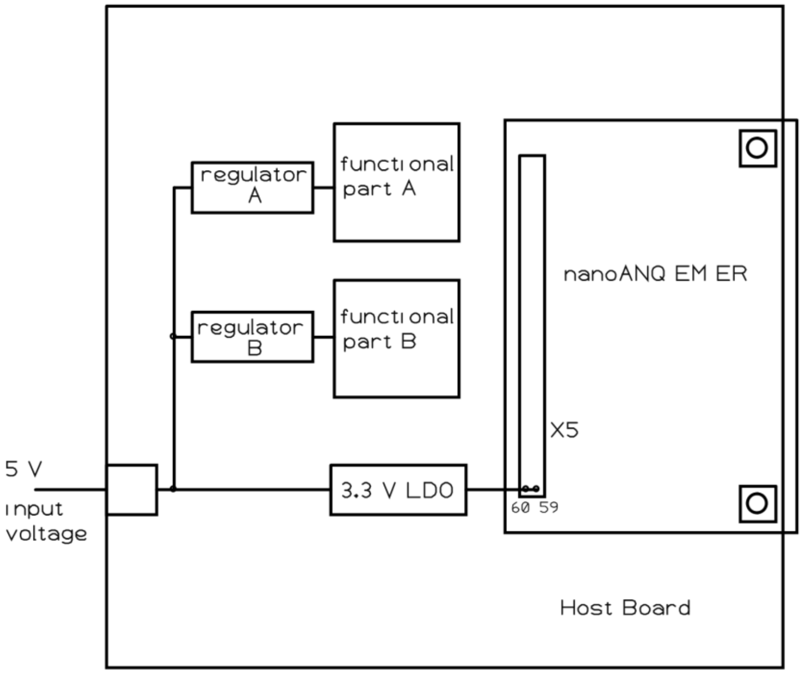

Figure 3-1: Block diagram

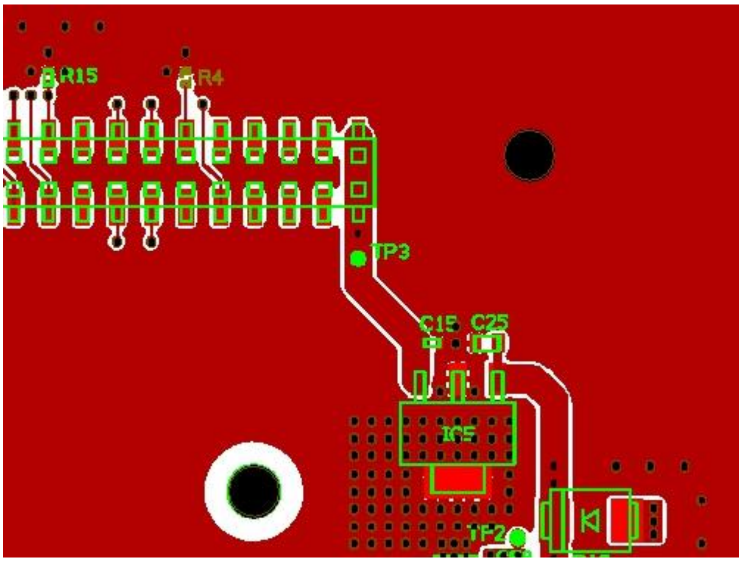

Figure 3-2: Design example

3.6. Interfaces and API

The Embedded Anchor Module is equipped with the required nanoANQ RTLS firmware to enable the module to operate in Nanotron's RTLS solution. The firmware can be updated via the module's Ethernet interface using the pre-flashed anchor firmware bootloader. For detailed information on how to upgrade Embedded Anchor Module firmware see the nanoANQ user guide [4].

3.6.1. RF interface

The RF interface for channel 0 (A) and channel 1 (B) consists of U.FL connectors. The maximal output power of -41.3 dB/MHz is provided into a 50 Ω load impedance. Deviating loads can cause lower output power and higher operating current. Directly connected antennas should have a reflection factor not higher than 2.

The RF ports of the Embedded Anchor Module are single-ended and have an impedance of 50 Ohm. It is decoupled from DC. This RF ports must be connected to an external antenna. Different types of antenna can be used.

The TX output power is not fixed to -41.3 dBm/MHz in all modes. Only mode 15 (channel 5, 6.8 Mbps) is calibrated to -41.3 dBm/MHz at the RF port and doesn't include any antenna gain or loss. Therefore it must be adjusted to match the national regulations. All other channels are not calibrated and will vary from module to module. To comply with regional regulations it is necessary to adjust the RF-power of each device accordingly, including antenna. How to set the different channels with the associated transmission rates and the output power is explained in the application AN [5].

3.6.2. Ethernet interface RMII

The Embedded Anchor Module provides a 10/100Mbit /s Ethernet MAC interface, which operates in RMII mode with Ethernet transceiver. **The clock source for RMII (50MHz) is not part of the Embedded Anchor Module and has to be placed on the motherboard.**

The figure below shows the operation in RMII mode with an external Ethernet transceiver.

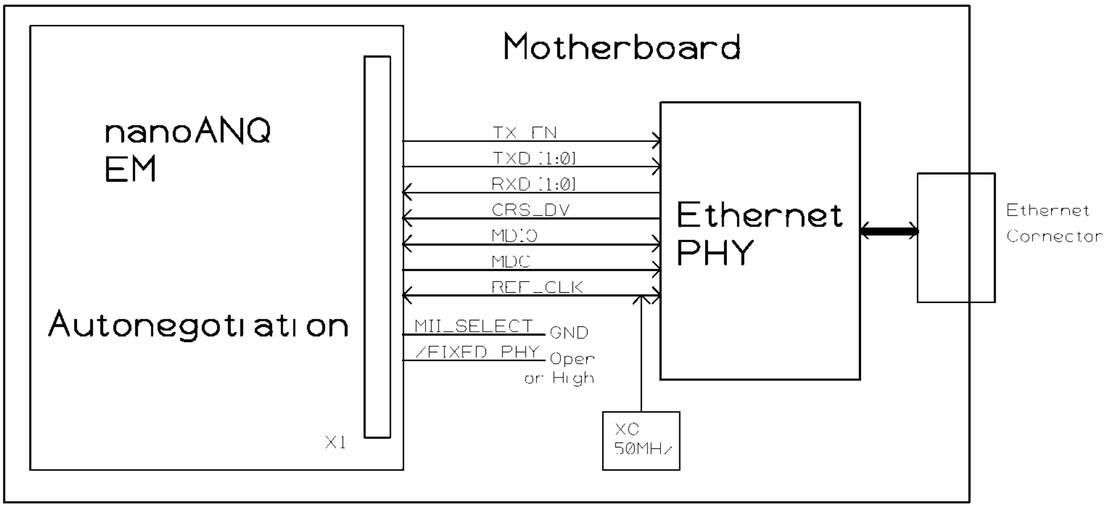

Figure 3-3: Embedded Anchor Module Ethernet connection in RMII mode with Ethernet PHY

Figure 3-3 shows the MAC Interface from the Embedded Anchor Module to an external Ethernet PHY in accordance with the RMII standard.

Table 3-1: RMII Standard Ethernet MAC Interface

Pin No.	Pin Name	Pin type	Pin Description	Electrical Conditions
7	ETH_MII_RX_DV /ETH_RMII_CRS_DV	I	Ethernet	buffered with a 33 Ω serial resistor
9	ETH_MII_RXD1/ETH_RMII_RXD1	I	Ethernet	buffered with a 33 Ω serial resistor
10	ETH_MII_RXD0/ETH_RMII_RXD0	I	Ethernet	buffered with a 33 Ω serial resistor
13	ETH_MII_TXD1 / ETH_RMII_TXD1	O	Ethernet	buffered with a 33 Ω serial resistor

Pin No.	Pin Name	Pin type	Pin Description	Electrical Conditions
14	ETH_MII_TXD0 / ETH_RMII_TXD0	O	Ethernet	buffered with a 33 Ω serial resistor
16	ETH_MII_TX_EN / ETH_RMII_TX_EN	O	Ethernet	buffered with a 33 Ω serial resistor
17	ETH_MII_RX_CLK / ETH_RMII_REF_CLK	I	Ethernet	buffered with a 33 Ω serial resistor
25	ETH_MDIO	I/O	Ethernet	buffered with a 33 Ω serial resistor
26	ETH_MDC	O	Ethernet	buffered with a 33 Ω serial resistor

Table 3-2 shows the pin assembly of special Ethernet signals, which are used to establish an RMII Ethernet MAC connection

Table 3-2: Special Ethernet signals for RMII Ethernet MAC connection

Pin No.	Pin Name	Pin type	Pin Description	Electrical Conditions
34	MII_SELECT	I	Ethernet mode selection, high = MII (default), low = RMII	buffered with a 100 Ω serial resistor, internal pull-up resistor
46	INT_PHY	I	Interrupt from Ethernet PHY	buffered with a 100 Ω serial resistor, low active
48	RESET_PHY	O	reset for Ethernet PHY	buffered with a 100 Ω serial resistor, low active
49	/FIXED_PHY	I	Ethernet is set to fixed PHY mode depending on the state of this pin	buffered with a 100 Ω serial resistor, high = external PHY or no PHY (default, internal Pull-up), low = fixed PHY mode

MII-Select: The state of this signal informs the control unit of the Embedded Anchor Module whether RMII or MII operating mode is wanted. An internal pull-up resistor sets the default state to MII.
INT_PHY: An interrupt signal generated by the PHY, which is used to detect if the Ethernet line is disconnected and reconnected. In this case the control unit is initializing the PHY for a new MAC to PHY connection.
RESET_PHY: This reset signal is generated by the control unit when its initialising is finished after power up. After this reset the PHY finds a fully operating control unit for communication.
/FIXED_PHY: The state of this signal gives the control unit the information to enter into an fixed PHY mode. In this mode 100Mbps and full-duplex are set as fix parameters. This mode is used for MAC to MAC connections.

3.6.3. Ethernet interface MII

The Embedded Anchor Module provides a 10/100Mbit /s Ethernet MAC interface, which can operate also in MII mode with an Ethernet transceiver.

The figure below shows the operation in MII mode with an external Ethernet transceiver.

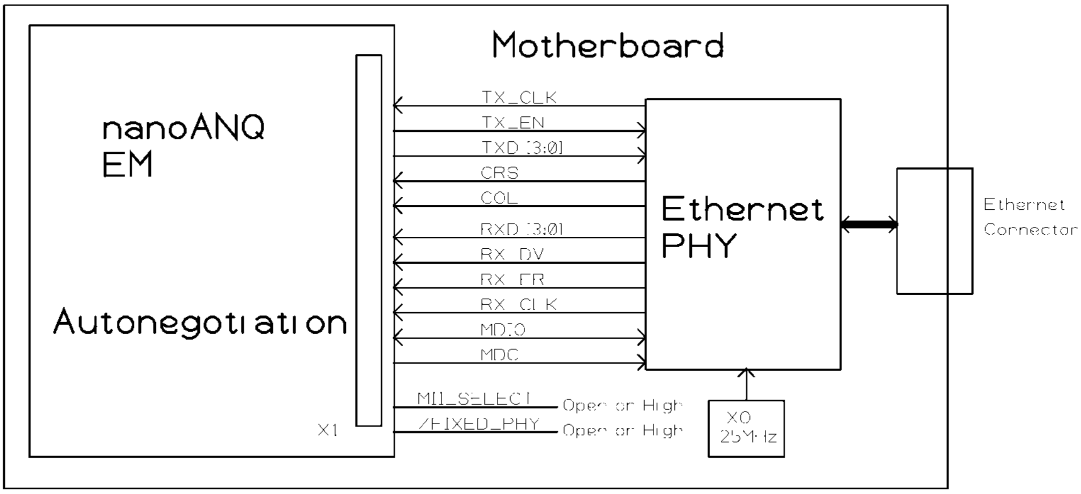

Figure 3-4: Embedded Anchor Module Ethernet connection in MII mode with Ethernet PHY

Table 3-3 shows the MAC Interface from the Embedded Anchor Module to an external Ethernet PHY in accordance to the MII standard. Some Pins of the Embedded Anchor Module are used alternatively for MII or RMII mode. Therefore these pin names contain the MII function and the RMII function i.e. "ETH_MII_TX_EN / ETH_RMII_TX_EN".

Table 3-3: MII Standard Ethernet MAC Interface

Pin No.	Pin Name	Pin type	Pin Description	Electrical Conditions
7	ETH_MII_RX_DV /ETH_RMII_CRS_DV	I	Ethernet	buffered with a 33 Ω serial resistor
9	ETH_MII_RXD1/ETH_RMII_RXD1	I	Ethernet	buffered with a 33 Ω serial resistor
10	ETH_MII_RXD0/ETH_RMII_RXD0	I	Ethernet	buffered with a 33 Ω serial resistor
11	ETH_MII_RXD3	I	Ethernet	buffered with a 33 Ω serial resistor
12	ETH_MII_RXD2	I	Ethernet	buffered with a 33 Ω serial resistor
13	ETH_MII_TXD1 / ETH_RMII_TXD1	O	Ethernet	buffered with a 33 Ω serial resistor
14	ETH_MII_TXD0 / ETH_RMII_TXD0	O	Ethernet	buffered with a 33 Ω serial resistor
15	ETH_MII_RX_ER	I	Ethernet	buffered with a 33 Ω serial resistor
16	ETH_MII_TX_EN / ETH_RMII_TX_EN	O	Ethernet	buffered with a 33 Ω serial resistor
17	ETH_MII_RX_CLK / ETH_RMII_REF_CLK	I	Ethernet	buffered with a 33 Ω serial resistor
18	ETH_MII_TXD3	O	Ethernet	buffered with a 33 Ω serial resistor
19	ETH_MII_TX_CLK	I	Ethernet	buffered with a 33 Ω serial resistor
21	ETH_MII_COL	I	Ethernet	buffered with a 33 Ω serial resistor

Pin No.	Pin Name	Pin type	Pin Description	Electrical Conditions
23	ETH_MII_TXD2	O	Ethernet	buffered with a 33 Ω serial resistor
24	ETH_MII_CRS_WKUP	I	Ethernet	buffered with a 33 Ω serial resistor
25	ETH_MDIO	I/O	Ethernet	buffered with a 33 Ω serial resistor
26	ETH_MDC	O	Ethernet	buffered with a 33 Ω serial resistor

Table 3-4 shows the pin assembly of special Ethernet signals, which are used to establish a MII Ethernet MAC connection.

Table 3-4: Special Ethernet signals for MII Ethernet MAC connection

Pin No.	Pin Name	Pin type	Pin Description	Electrical Conditions
34	MII_SELECT	I	Ethernet mode selection, high = MII (default), low = RMII	buffered with a 100 Ω serial resistor, internal pull-up resistor
46	INT_PHY	I	interrupt from Ethernet PHY	buffered with a 100 Ω serial resistor, low active
48	RESET_PHY	O	reset for Ethernet PHY	buffered with a 100 Ω serial resistor, low active
49	/FIXED_PHY	I	Ethernet is set to fixed PHY mode depending on the state of this pin	buffered with a 100 Ω serial resistor, high = external PHY or no PHY (default, internal Pull-up), low = fixed PHY mode

MII-Select: The state oft this signal informs the control unit of the Embedded Anchor Module whether RMII or MII operating modus is wanted. An internal pull-up resistor sets the default state to MII.
INT_PHY: An interrupt signal generated by the PHY, which is used for detection if the Ethernet line is disconnected and reconnected. In this case the control unit is initializing the PHY for a new MAC to PHY connection.
RESET_PHY: This reset signal is generated by the control unit when its initialising is finished after power up. After this reset the PHY finds a fully operating control unit for communication.
/FIXED_PHY: The state of this signal gives the control unit the information to enter in an fixed PHY mode. In this mode 100Mbps and full-duplex are set as fix parameters. This mode is used for MAC to MAC connections.

3.6.4. Ethernet MAC to MAC mode

The figure below shows the Ethernet MAC to MAC connection without Ethernet PHY.

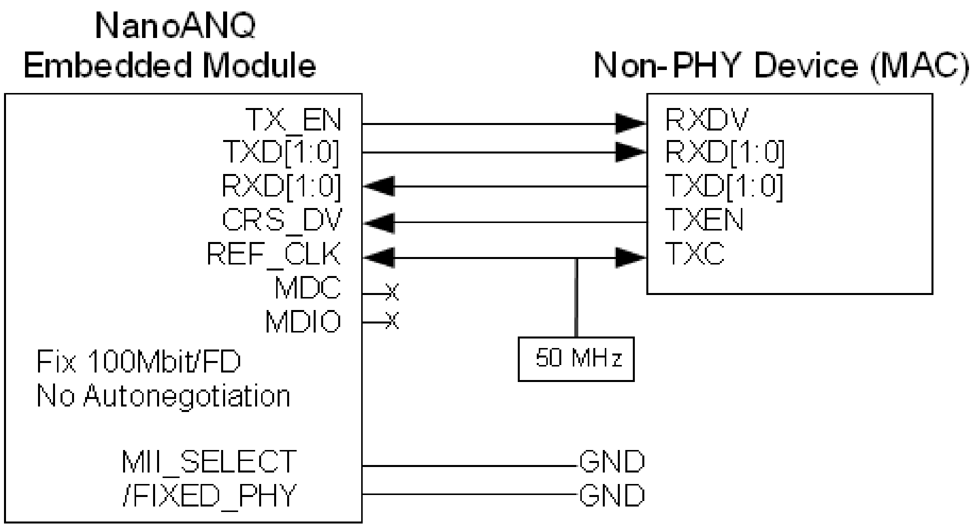

Figure 3-5: Embedded Anchor Module Ethernet MAC to MAC connection, RMII mode

In this mode the nanoANQ Embedded Module is set to fix Ethernet parameters 100Mbps and full-duplex. No autonegotiation with a counterpart takes place. The data lines MDIO and MDC are not used.

3.6.5. nanoANQ EM ER networking modes

The following modes of network operation are implemented:

- Mode 1: Wired, with link state detection
- Mode 2: Wireless, without any wired networking
- Mode 3: Wired, with fixed PHY

Mode 1:

This is the mode with PHY connected to MDIO / MDC lines and with MII / RMII interface. In this mode a pull-up resistor that can overdrive the STM32's built-in pull-down resistor should be connected to the MDIO line. In this case the anchor uses autonegotiation to establish link parameters (10 / 100 Mbps, full- / half-duplex). It operates in CSS wireless backbone mode if the Ethernet link is down. The mode line /FIXED_PHY should be left open. The value of the STM32's internal pull-down resistor is 30 – 50 kΩ.

Mode 2:
If the /FIXED_PHY line is not pulled down and a PHY could not be detected by probing the MDIO line (should be left open), then the module enters into wireless mode and does not attempt to use MII / RMII interface. Only connecting the power supply is needed for operating in CSS wireless backbone mode.

Mode 3:

If the module's /FIXED_PHY line is pulled down, then the module enters into the fixed PHY mode. The Ethernet interface is configured to operate in 100 Mbps / full-duplex mode. The MDIO / MDC lines are not used. No link state detection is possible. This mode is used for MAC to MAC connection.

3.6.6. A Sample Ethernet implementation with the Ethernet PHY KSZ8721

As a sample implementation the application of the Ethernet PHY KS8721 from Micrel is shown. For the usage of the KSZ8721 cf. [1], [2].

The following figures show the **Ethernet RMII configuration** of the Ethernet PHY KS8721 as implemented on the Embedded Anchor Module test board.

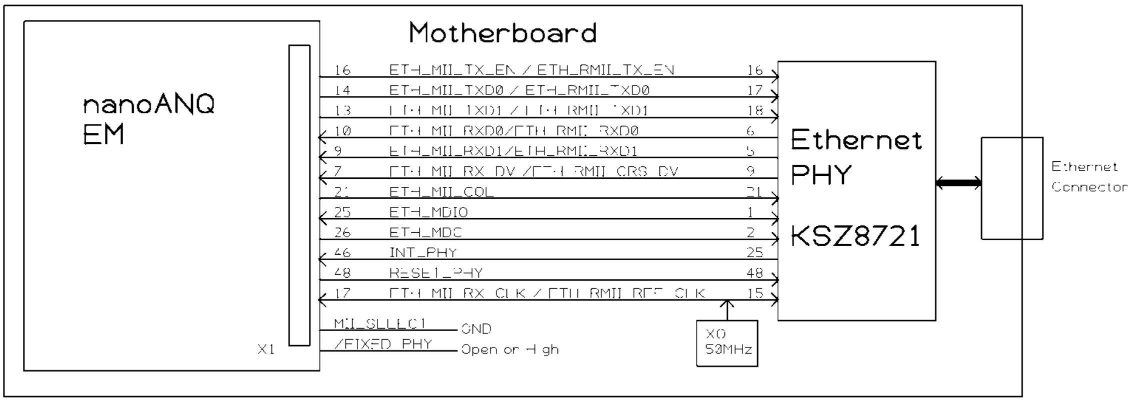

Figure 3-6: Embedded Anchor Module Ethernet RMII connection with Ethernet PHY KSZ8721

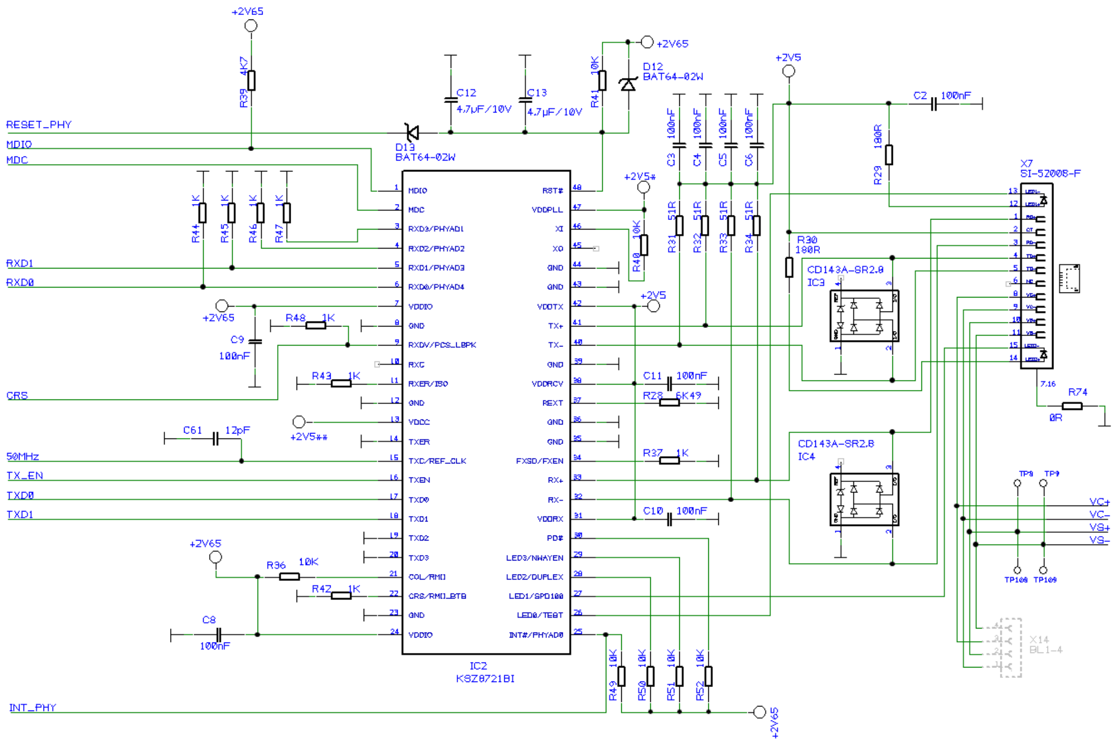

Figure 3-7: Recommended circuitry for Embedded Anchor Module RMII Ethernet connection

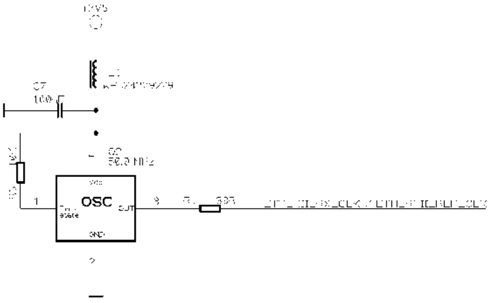

Figure 3-8: Clock source 50 MHz for RMII mode on Embedded Anchor Module

The following figures show the **Ethernet MII configuration** of the Ethernet PHY KS8721 as implemented on the Embedded Anchor Module test board.

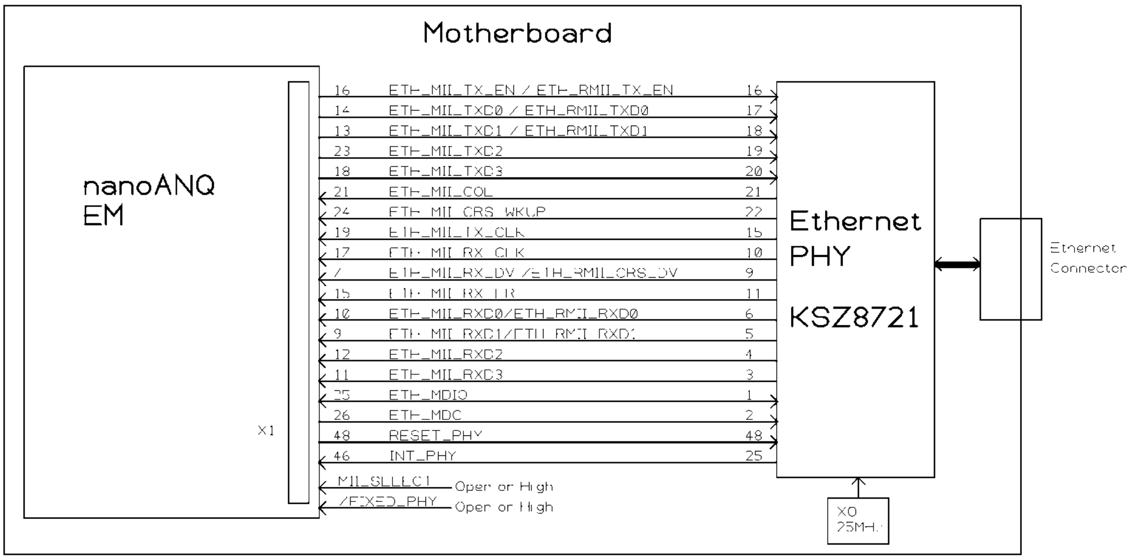

Figure 3-9: Embedded Anchor Module Ethernet MII connection with Ethernet PHY KSZ8721

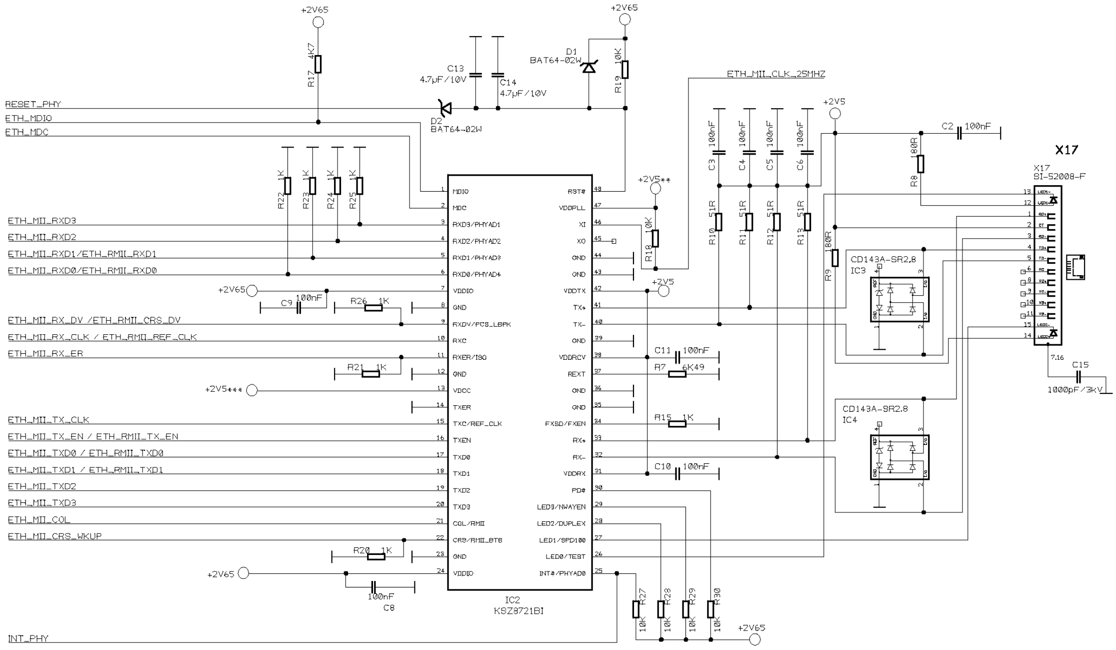

Figure 3-10: Recommended circuitry for Embedded Anchor Module MII Ethernet connection

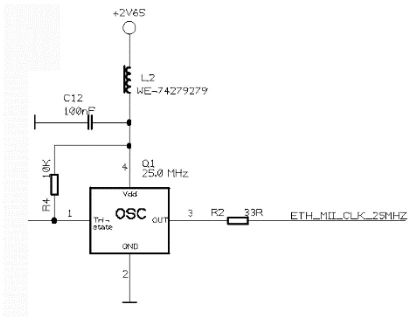

Figure 3-11: Clock source 25 MHz for MII mode on Embedded Anchor Module

Differences of MII and RMII mode using the KSZ8721

The Ethernet PHY KSZ8721 can be used for operation with the Embedded Anchor Module in MII or RMII mode. The differences between MII and RMII mode are the state of the “ETH_MII_COL“ signal during the start up of the KSZ8721 and the clock sourcing. Additionally the nanoANQ Embedded Module needs the information whether MII or RMII is wanted. The state of the signal MII_SELECT gives this information.

- State of “MII_SELECT”:
MII mode is requested: MII_SELECT must be set to high or let open
RMII mode is requested: MII_SELECT must be set to low (GND)

- State of “ETH_MII_COL” (pin 21 of KSZ8721) during start-up:
MII mode: must be set to low
This is the default mode with an internal pull-down resistor of the KSZ8721.

RMII mode: must be set to high
Is set by an external pull-up resistor.

- Clock sourcing
MII mode: The KSZ8721 provides the TX clock and the RX clock for the Embedded Anchor Module. The clock signal inputs of the Embedded Anchor Module are “ETH_MII_TX_CLK” (X 1 / pin 19) and “ETH_MII_RX_CLK / ETH_RMII_REF_CLK” (X 1 / pin 17)

X 1 / pin 17 (clock input) has to be connected to pin 10 of the KSZ8721 (clock output)
X 1 / pin 19 (clock input) has to be connected to pin 15 of the KSZ8721 (clock output)
The MII mode operation is shown in Figure 3-10.

RMII mode: An external clock source provides the REF clock for the the Embedded Anchor Module and the KSZ8721. The clock signal input of the Embedded Anchor Module is “ETH_MII_RX_CLK / ETH_RMII_REF_CLK” (X 1 / pin 17)

X 1 / pin 17 (clock input) has to be connected to pin 15 of the KSZ8721 (clock input).
X 1 / pin 19 and pin 10 of the KSZ8721 are not used.
The RMII mode operation is shown inFigure 3-7.

NB: The signal “ETH_MII_RX_CLK / ETH_RMII_REF_CLK” on X 1 / pin 17 of the Embedded Anchor Module has to be connected to pin 15 of the KSZ8721 in RMII mode and to pin 10 in MII mode.

3.6.7. USB interface

The Embedded Anchor Module includes a USB 2.0 full speed interface in device mode for **maintenance purposes only**. Therefore a mini / micro USB B connector with no connection of the ID pin (pin 6 on the Embedded Anchor Module interface connector) is recommended for the motherboard.
Except for optional protection circuits the USB interface needs no additional components on a motherboard.

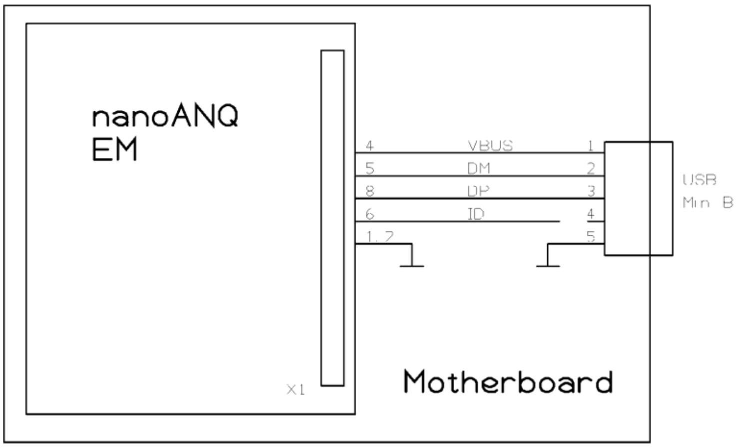

Figure 3-12: An example for connecting the USB interface

Table 3-5 shows the pin functions of the USB interface.

Table 3-5: USB signals, pin description

Pin No.	Pin Name	Pin type	Pin Description	Electrical Conditions
1	GND	-	circuit ground	
4	USB_OTG_FS_VBUS	I	USB Bus voltage	
5	USB_OTG_FS_DM	I/O	USB differential serial data line	buffered with a 10 Ω serial resistor
6	USB_OTG_FS_ID	I	USB connector identification	buffered with a 100 Ω serial resistor
8	USB_OTG_FS_DP	I/O	USB differential serial data line	buffered with a 10 Ω serial resistor

3.6.8. GPIO

The Embedded Anchor Module includes four general purpose inputs and four general purpose outputs. All pins are buffered with a 100 Ω serial resistor to limit the maximum current drain.

Table 3-6: GPIO signals, pin description

Pin No.	Pin Name	Pin type	Pin Description	Electrical Conditions
35	OUT_3	O	general purpose output	buffered with a 100 Ω serial resistor
36	OUT_4	O	general purpose output	buffered with a 100 Ω serial resistor
37	OUT_1	O	general purpose output	buffered with a 100 Ω serial resistor
38	OUT_2	O	general purpose output	buffered with a 100 Ω serial resistor
39	IN_3	I	general purpose input	buffered with a 100 Ω serial resistor

Pin No.	Pin Name	Pin type	Pin Description	Electrical Conditions
40	IN_4	I	general purpose input	buffered with a 100 Ω serial resistor
41	IN_1	I	general purpose input	buffered with a 100 Ω serial resistor
42	IN_2	I	general purpose input	buffered with a 100 Ω serial resistor

The general function pins 35…42 are split into 4 outputs (pins 35 …38) and 4 inputs (39…42).

Note:
For inputs the minimum input high level V_{IH} is 1.8V.
For inputs the maximum input low level V_{IL} is 0.8V.
For outputs the minimum output high level V_{OH} is about 2.25V depending on the total load of the microcontroller, cf. [1].
For outputs the maximum output low level V_{OL} is about 0.4V depending on the total load of the microcontroller, cf.[1].
For absolute maximum voltage ratings with respect to the used operating voltage of 2.65 V ± 0.05 V cf.[1].
For outputs the voltage drop across the serial buffer resistors must be taken into consideration.

The maximum source or sink current of outputs must not exceed 25mA per port. For the maximum total current consumption of the microcontroller cf.[1].

3.7. Over-the-Air Anchor Synchronization

The embedded anchor module supports nanotron's patent pending synchronization method (EP 2525236 A1) required for operating the device as part of a TDOA localization solution in conjunction with the appropriate location engine and server software.

3.8. Detection of Location Broadcasts

Tags that are part of the nanotron RTLS platform can send out location broadcasts periodically in eighteen different modes. Six different channels having three different bitrates. The modes having 6.8 Mbpds are recommended to allow the highest tag densities.

The time of arrival (ToA) of tag broadcasts are captured by the anchor module with better than 1 ns resolution and detection rate of more than 1025 per second. Through air radio waves travel 30 cm in 1 ns. ToAs from different anchor modules are used to calculate the time difference of arrival (TDoA). Several TDoAs results are combined to estimate the tag position.

4. Pin Information

The Embedded Anchor Module interface connector is a 2 x 30 pole through hole pin connector with 2mm spacing.

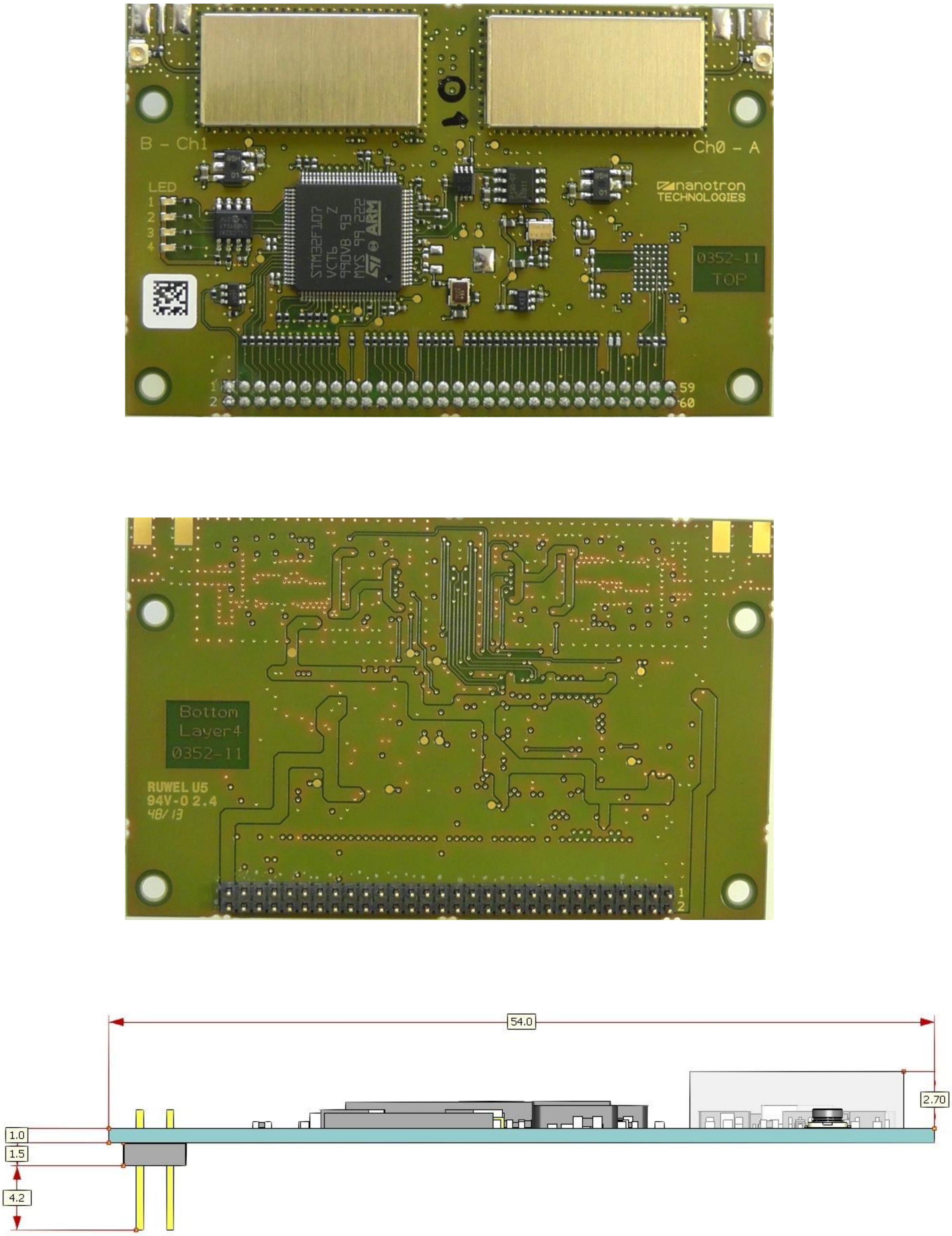

Figure 4-1: nanoANQ EM ER (with U.FL connector, no flash memory)

Table 4-1: Interface connector, pin description

Pin No.	Pin Name	Pin type[1])	Pin Description	Electrical Conditions
1	GND	-	circuit ground	
2	GND	-	circuit ground	
3	+2V65	O	2.65V digital voltage reference output	maximum load current 30mA
4	USB_OTG_FS_VBUS	I	USB Bus voltage	
5	USB_OTG_FS_DM	I/O	USB differential serial data line	buffered with a 10 Ω serial resistor
6	USB_OTG_FS_ID	I	USB connector identification	buffered with a 100 Ω serial resistor
7	ETH_MII_RX_DV /ETH_RMII_CRS_DV	I	Ethernet[2)]	buffered with a 33 Ω serial resistor
8	USB_OTG_FS_DP	I/O	USB differential serial data line	buffered with a 10 Ω serial resistor
9	ETH_MII_RXD1/ETH_RMII_RXD1	I	Ethernet[2)]	buffered with a 33 Ω serial resistor
10	ETH_MII_RXD0/ETH_RMII_RXD0	I	Ethernet[2)]	buffered with a 33 Ω serial resistor
11	ETH_MII_RXD3	I	Ethernet[2)]	buffered with a 33 Ω serial resistor
12	ETH_MII_RXD2	I	Ethernet[2)]	buffered with a 33 Ω serial resistor
13	ETH_MII_TXD1 / ETH_RMII_TXD1	O	Ethernet[2)]	buffered with a 33 Ω serial resistor
14	ETH_MII_TXD0 / ETH_RMII_TXD0	O	Ethernet[2)]	buffered with a 33 Ω serial resistor
15	ETH_MII_RX_ER	I	Ethernet[2)]	buffered with a 33 Ω serial resistor
16	ETH_MII_TX_EN / ETH_RMII_TX_EN	O	Ethernet[2)]	buffered with a 33 Ω serial resistor
17	ETH_MII_RX_CLK / ETH_RMII_REF_CLK	I	Ethernet[2)]	buffered with a 33 Ω serial resistor
18	ETH_MII_TXD3	O	Ethernet[2)]	buffered with a 33 Ω serial resistor
19	ETH_MII_TX_CLK	I	Ethernet[2)]	buffered with a 33 Ω serial resistor
20	GND		circuit ground	
21	ETH_MII_COL	I	Ethernet[2)]	buffered with a 33 Ω serial resistor
22	GND	-	circuit ground	
23	ETH_MII_TXD2	O	Ethernet[2)]	buffered with a 33 Ω serial resistor
24	ETH_MII_CRS_WKUP	I	Ethernet[2)]	buffered with a 33 Ω serial resistor
25	ETH_MDIO	I/O	Ethernet[2)]	buffered with a 33 Ω serial resistor
26	ETH_MDC	O	Ethernet[2)]	buffered with a 33 Ω serial resistor
27	Reserved	-	-	must be left open
28	Reserved	-	-	must be left open
29	Reserved	-	-	must be left open
30	Reserved	-	-	must be left open
31	Reserved	-	-	must be left open
32	Reserved	-	-	must be left open
33	Reserved	-	-	must be left open
34	MII_SELECT	I	Ethernet mode selection, high = MII (default), low = RMII	buffered with a 100 Ω serial resistor, internal pull-up resistor
35	OUT_3	O	general purpose output	buffered with a 100 Ω serial resistor

Pin No.	Pin Name	Pin type[1]	Pin Description	Electrical Conditions
36	OUT_4	O	general purpose output	buffered with a 100 Ω serial resistor
37	OUT_1	O	general purpose output	buffered with a 100 Ω serial resistor
38	OUT_2	O	general purpose output	buffered with a 100 Ω serial resistor
39	IN_3	I	general purpose input	buffered with a 100 Ω serial resistor
40	IN_4	I	general purpose input	buffered with a 100 Ω serial resistor
41	IN_1	I	general purpose input	buffered with a 100 Ω serial resistor
42	IN_2	I	general purpose input	buffered with a 100 Ω serial resistor
43	Reserved	-	-	must be left open
44	Reserved	-	-	must be left open
45	Reserved	-	-	must be left open
46	INT_PHY	I	interrupt from Ethernet PHY	buffered with a 100 Ω serial resistor, low active
47	RESET	I	reset for microcontroller	buffered with a 100 Ω serial resistor, low active
48	RESET_PHY	O	reset for external Ethernet PHY	buffered with a 100 Ω serial resistor, low active
49	/FIXED_PHY	I	Ethernet is set to fixed PHY mode depending on the state of this pin	buffered with a 100 Ω serial resistor, high = external PHY or no PHY (default, internal Pull-up), low = fixed PHY mode
50	Reserved	-	-	must be left open
51	/TX_ON_1	O	transmitting indicator for RF channel B	buffered with a 1k serial resistor, low active
52	Reserved	-	-	must be left open
53	Reserved	-	-	must be left open
54	/TX_ON_0	O	transmitting indicator for RF channel A	buffered with a 1k serial resistor, low active
55	Reserved	-	-	must be left open
56	Reserved	-	-	must be left open
57	Reserved	-	-	must be left open
58	Reserved	-	-	must be left open
59	+3V3	I	power supply, nominal 3.3V	supply range +3.0V ...+3.6V, Imax = 0.42A
60	+3V3	I	power supply, nominal 3.3V	supply range +3.0V ...+3.6V, Imax = 0.42A

1) I = Input
O = Output
I/O = Input / Output bidirectional
\- = not defined

2) For detailed description of the Ethernet pins see the datasheet of the microcontroller STM32F107xx used in the Embedded Anchor Module, which can be downloaded from the STMicroelectronics website. The Ethernet pin names are adopted from the STM32F107xx datasheet [1].

Except for the USB Pins 4, 5, 6, 8 all digital signals refer to the Embedded Anchor Module core voltage of 2.65V ± 0.05V.

Note:
For inputs the minimum input high level V_{IH} is 1.8V.
For inputs the maximum input low level V_{IL} is 0.8V.
For outputs the minimum output high level V_{OH} is about 2.25V depending on the total load of the microcontroller, cf. [1].
For outputs the maximum output low level V_{OL} is about 0.4V depending on the total load of the microcontroller, cf. [1].

For outputs the voltage drop across the serial buffer resistors must be taken into consideration.

The maximum source or sink current of outputs must not exceed 25mA per port. For the maximum total current consumption of the microcontroller cf. [1].

5. Mechanical Dimensions

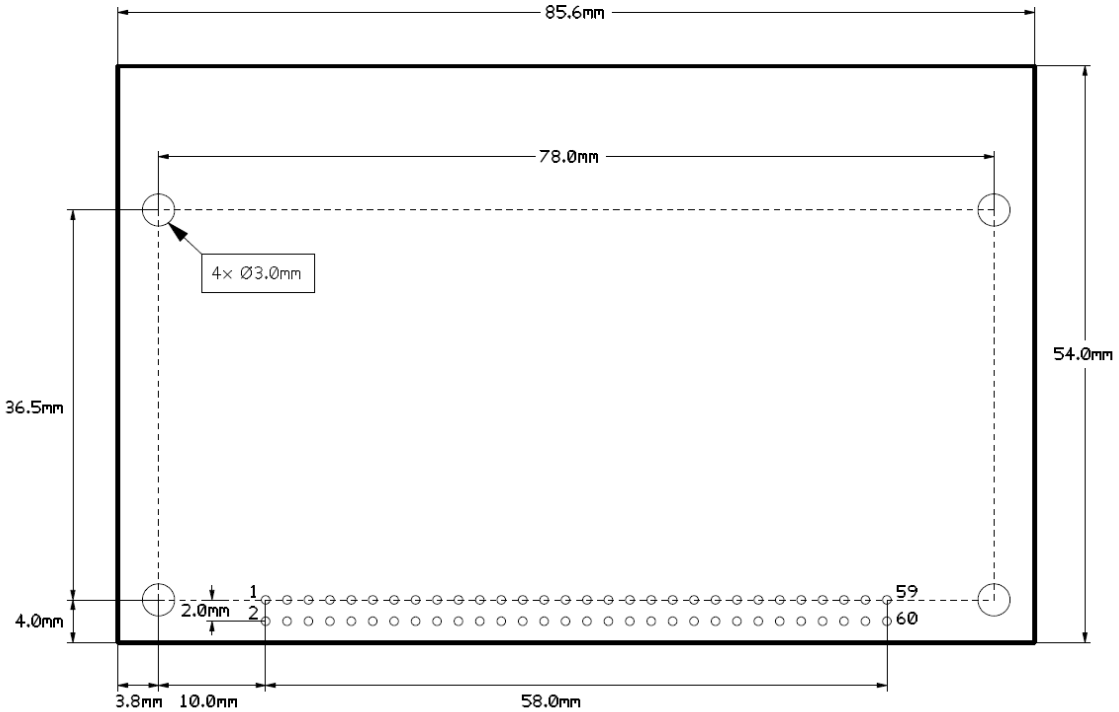

Figure 5-1: Dimension and pin counting, top view (Anchor Module with U.FL connector)

6. References

[1] STMicroelectronics, Datasheet STM32F105xx/STM32F107xx, Doc ID 15274 Rev.6, August 2011
[2] Micrel, Inc., Datasheet KS7821 B/BT, Rev 2.3, March 2006
[3] Micrel, Inc., Datasheet KS7821 BL/SL, Rev 1.3, June 2009
[4] Nanotron nanoANQ User Guide, October 2013
[5] Application Note Doc ID NA-19-0371-0004

Document History

Date	Authors	Version	Description
2018-11-23	MBO	1.0	Initial Version
2019-02-19	MBO	1.1	Adapted values to current measurements
2019-09-09	MBO	1.2	Added Ordering Information in header

Life Support Policy

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