MASWSS0192



GaAs SPDT Switch DC - 3.0 GHz

Rev. V1

Features

- Test and Measurement and Low/Medium Power Telecommunication Applications
- Low Insertion Loss: 0.18 dB @ 1 GHz
- Moderate Isolation: 25 dB @ 1 GHz
- Low Power Consumption: < 2 μA @ 2.5 V
- · Fast Settling for Low Gate Lag Requirements
- Lead-Free SC-70 (SOT-363) Package
- 100% Matte Tin Plating over Copper
- Halogen-Free "Green" Mold Compound
- RoHS* Compliant and 260°C Reflow Compatible

Description

M/A-COM's MASWSS0192 is a GaAs PHEMT MMIC SPDT switch in a lead-free SC-70 (SOT-363) surface mount plastic package. The MASWSS0192 is ideally suited for applications where very small size and low cost are required.

The MASWSS0192 can be used for low / medium power, low loss requirements in all systems operating up to 3 GHz, including PCS, GSM, DCS, Blue Tooth, T&M, and other receive chain applications.

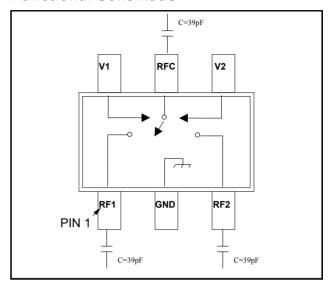
The MASWSS0192 is fabricated using a 0.5 micron gate length GaAs PHEMT process. The process features full passivation for performance and reliability.

Ordering Information ¹

Part Number	Package	
MASWSS0192	Bulk Packaging	
MASWSS0192TR-3000	3000 piece reel	
MASWSS0192SMB	Sample Board	

^{1.} Reference Application Note M513 for reel size information.

Functional Schematic



Pin Configuration

Pin No.	Pin Name	Description		
1	RF1	RF Port 1		
2	GND	Ground		
3	RF2	RF Port 2		
4	V2	Control 2		
5	RFC	RF Input		
6	V1	Control 1		

Absolute Maximum Ratings ^{2,3}

Parameter	Absolute Maximum		
Input Power (0.5 - 3.0 GHz)			
2.5 V Control	+25 dBm		
5.0 V Control	+34 dBm		
Operating Voltage	+8.5 volts		
Operating Temperature	-40 °C to +85 °C		
Storage Temperature	-65 °C to +150 °C		

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- M/A-COM does not recommend sustained operation near these survivability limits.

^{*} Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.



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Electrical Specifications: $T_A = 25^{\circ}C$, $V_C = 0 \text{ V} / 2.5 \text{ V}^4$, $P_{IN} = +10 \text{ dBm}$, $Z_0 = 50 \Omega^5$

Parameter	Test Conditions	Units	Min.	Тур.	Max.
Insertion Loss ⁶	DC - 1.0 GHz DC - 3.0 GHz	dB dB	_	0.18 0.35	0.40 0.60
Isolation	DC - 1.0 GHz DC - 3.0 GHz	dB dB	20.0 9.5	24.0 13.5	_
VSWR	DC - 1.0 GHz DC - 3.0 GHz	Ratio Ratio	_	1.1:1 1.2:1	_
IP2	1 GHz, Two Tone, +7 dBm / tone, 20 MHz Spacing, 3 V	dBm	_	93	_
IP3	1 GHz, Two Tone, +7 dBm / tone, 20 MHz Spacing, 3 V	dBm	_	53	_
P1dB	V _C = 0.2 V / 2.7 V V _C = 0.2 V / 3.0 V	dBm dBm	_	27.5 28.5	_
Trise, Tfall	10% to 90% RF and 90% to 10% RF	nS	_	22	_
Ton, Toff	50% control to 90% RF, 50% control to 10% RF	nS	_	5	_
Transients	In-band	mV	_	36	_
Control Current	_	μA	_	0.20	5
R _{oN}	t > 90 mS after OFF to ON Switching (settled)	Ω	_	2.50	4.7
Gate Lag	ΔRon between 15 μS and 90 mS after OFF to ON Switching	Ω	_	0.15	0.7

^{4.} Alternate voltage operation of V_C = 0 V / 5 V or -5 V / 0 V will yield similar insertion loss, isolation, VSWR, switching, R_{oN}, and gate lag results.

Truth Table 7,8

Control V1	Control V2	RFC-RF1	RFC-RF2
1	0	On	Off
0	1	Off	On

Differential voltage, V (state 1) - V (state 0), must be 2.5 V minimum, but must not exceed 8.5 V.

Qualification

Qualified to M/A-COM specification REL-201, Process Flow –2.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

^{5.} For positive voltage control, external DC blocking capacitors are required on all RF ports.

^{6.} Insertion loss can be optimized by varying the DC blocking capacitor value, e.g. 1000 pF for 100 MHz - 1 GHz, 39 pF for 0.5 - 3 GHz.

^{8. 0 = 0} V to 0.5 V; 1 = 2.5 V to 5 V or 0 = -5 V to -2.5 V, 1 = -0.5 to 0 V.

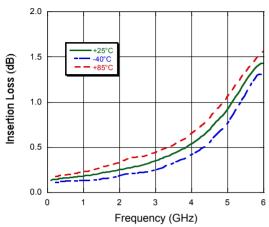


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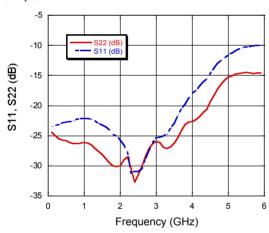
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Typical Performance Curves

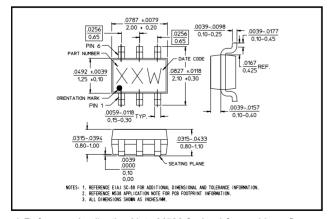




S11, S22



Lead-Free SC-70 (SOT-363)[†]

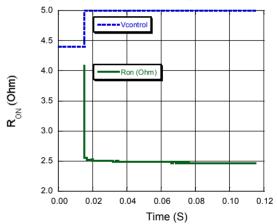


† Reference Application Note M538 for lead-free solder reflow recommendations.

15 | 10 | 1 | 2 | 3 | 4 | 5 | 6

Gate Lag (R_{ON} vs. Time) Including V_{CTL}, 0-3 V Step

Frequency (GHz)



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