# ISOCOM COMPONENTS

## ICPL316J

## DESCRIPTION

The ICPL316J is a 5A Gate Drive Optocoupler with Integrated Desaturation Detection and an optically isolated Fault Status Feedback. It contains an AlGaAs LED optically coupled to an integrated circuit with a power output stage. It is ideally suited for driving power IGBTs and MOSFET used in motor control inverter applications with ratings up to 1200 V and 150 A.

ICPL316J is housed in SO16 package.

## FEATURES

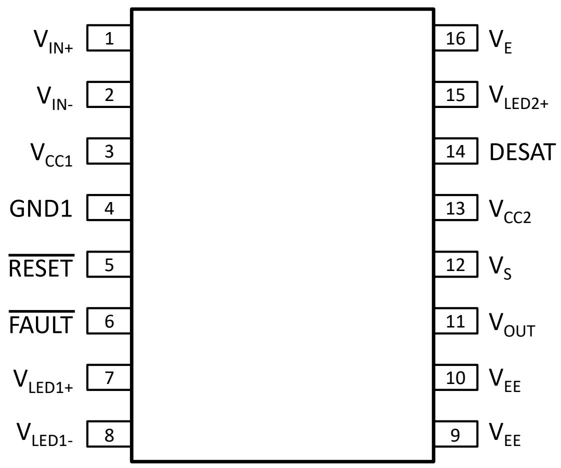
- 5.0A maximum Peak Output Current
- Integrated Fail-safe IGBT Protection
  - Desaturation ($V_{CE}$) Detection
  - Under Voltage Lock Out (UVLO) with Hysteresis
- Optically isolation Fault Status Feedback
- Wide Operating Voltage Range
  $V_{CC}$ 15 to 30 V
- Guaranteed performance over Temperature range - 40°C to +100°C
- Very high Common Mode Rejection (CMR)
  15kV/µs minimum at $V_{CM}$ 1500V
- Lead Free and RoHS Compliant
- UL File E91231

## APPLICATIONS

- Isolated IGBT / MOSFET Gate Drive
- Industrial Inverters

## ORDER INFORMATION

- Supplied in Tape and Reel




**CAUTION :**
It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

| | | |
|---|---|---|
| 1 | $V_{IN+}$ | Non-inverting $V_{OUT}$ Control Input |
| 2 | $V_{IN-}$ | Inverting $V_{OUT}$ Control Input |
| 3 | $V_{CC1}$ | Positive Input Supply Voltage |
| 4 | GND1 | Input Ground |
| 5 | $\overline{RESET}$ | FAULT Reset Input |
| 6 | $\overline{FAULT}$ | FAULT Output |
| 7 | $V_{LED+}$ | LED 1 Anode |
| 8 | $V_{LED-}$ | LED 2 Cathode |
| 9 | $V_{EE}$ | Negative Output Supply Voltage |
| 10 | $V_{EE}$ | Negative Output Supply Voltage |
| 11 | $V_{OUT}$ | Gate Drive Voltage Output |
| 12 | $V_S$ | Output Pull Up MOSFET Source |
| 13 | $V_{CC2}$ | Positive Output Supply Voltage |
| 14 | DESAT | Desaturation Voltage Input |
| 15 | $V_{LED2+}$ | LED 2 Anode |
| 16 | $V_E$ | Common Output Supply Voltage (IGBT Emitter) |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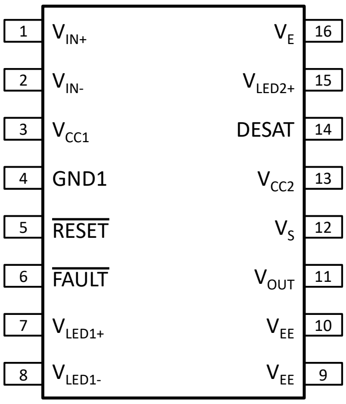


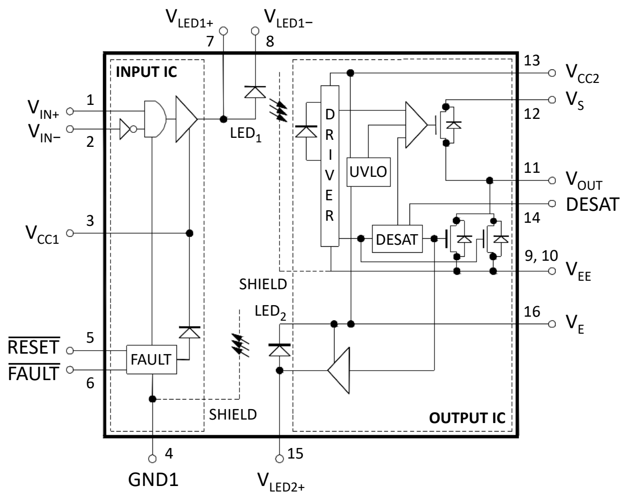


| | | |
|---|---|---|
| 1 | $V_{IN+}$ | Non-inverting Gate Drive Control ($V_{OUT}$) Input |
| 2 | $V_{IN-}$ | Inverting Gate Drive Control ($V_{OUT}$) Input |
| 3 | $V_{CC1}$ | Positive Input Supply Voltage (4.5 V to 5.5 V) |
| 4 | GND1 | Input Ground |
| 5 | $\overline{\text{RESET}}$ | $\overline{\text{FAULT}}$ Reset Input<br>A logic low input for at least 0.1µs, asynchronously resets $\overline{\text{FAULT}}$ output high and enables $V_{IN}$. Synchronous control of $\overline{\text{RESET}}$ relative to $V_{IN}$ is required. $\overline{\text{RESET}}$ is not affected by UVLO. Asserting $\overline{\text{RESET}}$ while $V_{OUT}$ is high does not affect $V_{OUT}$. |
| 6 | $\overline{\text{FAULT}}$ | Fault Output<br>$\overline{\text{FAULT}}$ changes from a high impedance state to a logic low output within 5µs of the voltage on the DESAT pin exceeding an internal reference voltage of 7V. $\overline{\text{FAULT}}$ output remains low until $\overline{\text{RESET}}$ is brought low. $\overline{\text{FAULT}}$ output is an open collector which allows the $\overline{\text{FAULT}}$ outputs from all ICPL316Js in a circuit to be connected together in a “wired OR” forming a single fault bus for interfacing directly to the micro-controller. |
| 7 | $V_{LED1+}$ | LED 1 Anode<br>This pin must be left unconnected for guaranteed data sheet performance (for Optical Coupling Testing only). |
| 8 | $V_{LED1-}$ | LED 1 Cathode<br>This pin must be connected to Ground. |
| 9 | $V_{EE}$ | Negative Output Supply Voltage |
| 10 | $V_{EE}$ | Negative Output Supply Voltage |
| 11 | $V_{OUT}$ | Gate Drive Voltage Output |
| 12 | $V_S$ | Output Pull Up MOSFET Source<br>It is connected to $V_{CC2}$ directly or through a resistor to limit output turn-on current. |
| 13 | $V_{CC2}$ | Positive Output Supply Voltage |
| 14 | DESAT | Desaturation Voltage Input<br>When the voltage on DESAT exceeds an internal reference voltage of 7V while the IGBT is on, $\overline{\text{FAULT}}$ output is changed from a high impedance state to a logic low state within 5µs. |
| 15 | $V_{LED2+}$ | LED 2 Anode<br>This pin must be left unconnected for guaranteed data sheet performance (for Optical Coupling Testing only). |
| 16 | $V_E$ | Common Output Supply Voltage (IGBT Emitter) |


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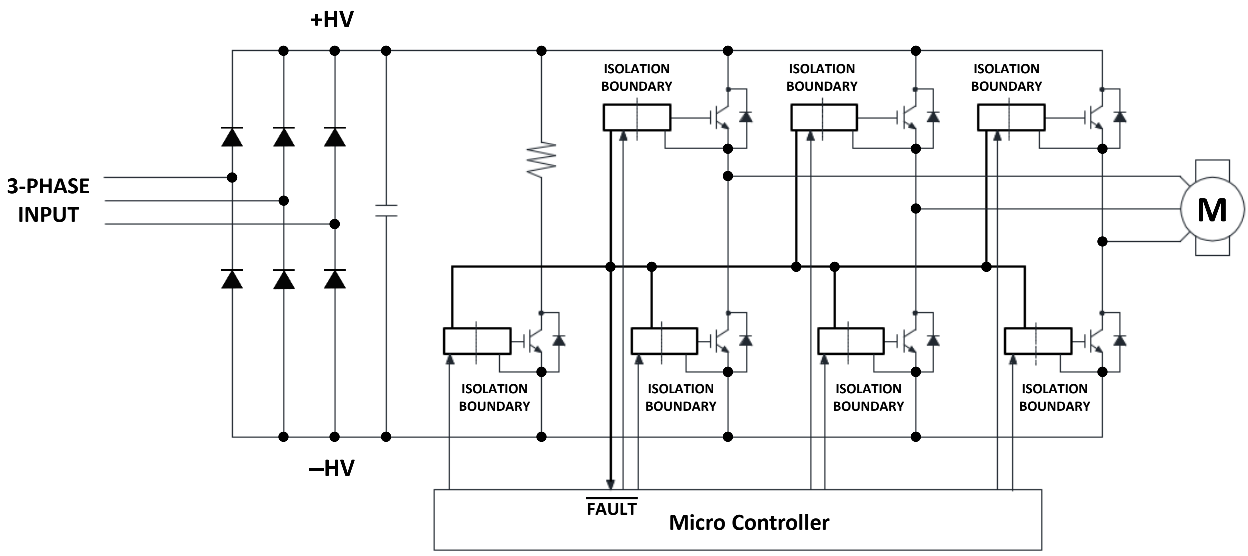
## FAULT Protected IGBT Gate Drive

The ICPL316J is an easy-to-use, intelligent gate driver which makes IGBT $V_{CE}$ fault protection compact, affordable, and easy-to-implement. Features such as user configurable inputs, integrated $V_{CE}$ detection, under voltage lockout (UVLO), "soft" IGBT turn-off and isolated fault feed back provide maximum design flexibility and circuit protection.

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## Overview

The ICPL316J is a highly integrated power control device that incorporates all the necessary components for a complete, isolated IGBT gate drive circuit with fault protection and feedback into one SO16 package.

TTL input logic levels allow direct interface with a microcontroller, and an optically isolated power output stage drives IGBTs with power ratings of up to 150 A and 1200 V. A high speed internal optical link minimizes the propagation delays between the microcontroller and the IGBT while allowing the two systems to operate at very large common mode voltage differences that are common in industrial motor drives and other power switching applications.

An output IC provides local protection for the IGBT to prevent damage during over-currents, and a second optical link provides a fully isolated fault status feedback signal for the microcontroller. A built in “watchdog” circuit monitors the power stage supply voltage to prevent IGBT caused by insufficient gate drive voltages.

This integrated IGBT gate driver is designed to increase the performance and reliability of a motor drive without the cost, size, and complexity of a discrete design.

Two light emitting diodes and two integrated circuits housed in the same SO16 package provide the input control circuitry, the output power stage, and two optical channels.

The input Buffer IC is designed on a bipolar process, while the output Detector IC is designed manufactured on a high voltage BiCMOS/Power DMOS process. The forward optical signal path, as indicated by LED1, transmits the gate control signal. The return optical signal path, as indicated by LED2, transmits the fault status feedback signal. Both optical channels are completely controlled by the input and output ICs respectively, making the internal isolation boundary transparent to the microcontroller.

Under normal operation, the input gate control signal directly controls the IGBT gate through the isolated output detector IC. LED2 remains off and a fault latch in the input buffer IC is disabled. When an IGBT fault is detected, the output detector IC immediately begins a “soft” shutdown sequence, reducing the IGBT current to zero in a controlled manner to avoid potential IGBT damage from inductive over-voltages. Simultaneously, this fault status is transmitted back to the input buffer IC via LED2, where the fault latch disables the gate control input and the active low fault output alerts the microcontroller.

During power-up, the Under Voltage Lockout (UVLO) feature prevents the application of insufficient gate voltage to the IGBT, by forcing the ICPL316J’s output low. Once the output is in the high state, the DESAT ($V_{CE}$) detection feature of the ICPL316J provides IGBT protection.

Thus, UVLO and DESAT work in conjunction to provide constant IGBT protection.

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## Description of Operation during Fault Condition

1. DESAT terminal monitors the IGBT $V_{CE}$ voltage through $D_{DESAT}$.
2. When the voltage on the DESAT terminal exceeds 7 volts, the IGBT gate voltage ($V_{OUT}$) is slowly lowered.
3. $\overline{\text{FAULT}}$ output goes low, notifying the microcontroller of the fault condition.
4. Microcontroller takes appropriate action.

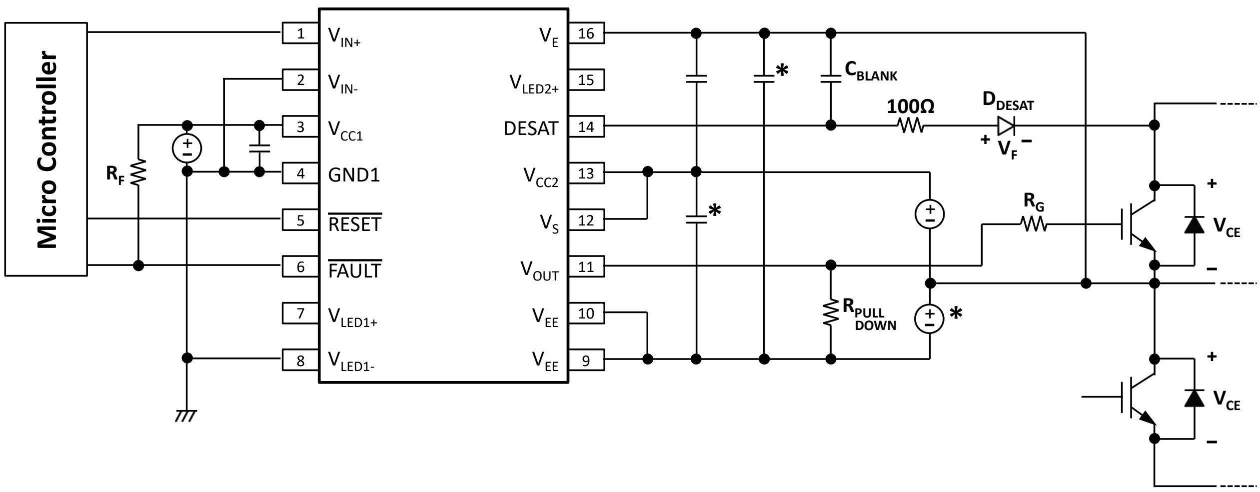
## Output control

The outputs ($V_{OUT}$ and $\overline{\text{FAULT}}$) of the ICPL316J are controlled by the combination of $V_{IN}$, UVLO and a detected IGBT Desat condition. The ICPL316J can be configured as inverting or non-inverting using the $V_{IN+}$ or $V_{IN-}$ inputs respectively.

When an inverting configuration is desired, $V_{IN+}$ must be held high and $V_{IN-}$ toggled.
When a non-inverting configuration is desired, $V_{IN-}$ must be held low and $V_{IN+}$ toggled.

Once UVLO is not active ($V_{CC2}–V_E > V_{UVLO}$), $V_{OUT}$ is allowed to go high, and the DESAT (pin 14) detection feature of the ICPL316J will be the primary source of IGBT protection. UVLO is needed to ensure DESAT is functional. Once $V_{UVLO+} > 11.6$ V, DESAT will remain functional until $V_{UVLO-} < 12.4$ V.

Thus, the DESAT detection and UVLO features of the ICPL316J work in conjunction to ensure constant IGBT protection.




* : These components are needed only when negative gate drive is implemented.

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## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C)

**Stresses exceeding the absolute maximum ratings can cause permanent damage to the device. Exposure to absolute maximum ratings for long periods of time can adversely affect reliability.**

| | | |
|---|---|---|
| **Input IC** | | |
| Positive Input Supply Voltage | $V_{CC1}$ | -0.5V to 5.5V |
| Input Pins Voltages | $V_{IN+}$, $V_{IN-}$ , $V_{\overline{RESET}}$ | -0.5V to $V_{CC1}$ |
| $\overline{\text{FAULT}}$ Output Current | $I_{\overline{FAULT}}$ | 8mA |
| Power Dissipation | $P_I$ | 150mW |
| **Output IC** | | |
| Total Output Supply Voltage | $V_{CC2} - V_{EE}$ | -0.5V to 35V |
| Positive Output Supply Voltage | $V_{CC2} - V_E$ | -0.5V to 35V–($V_E$–$V_{EE}$) |
| Negative Output Supply Voltage | $V_E - V_{EE}$ | -0.5V to 15V |
| Gate Drive Output Voltage | $V_{O(PEAK)}$ | -0.5V to $V_{CC2}$ |
| Source Voltage | $V_S$ | $V_{EE}$+5V to $V_{CC2}$ |
| DESAT Voltage | $V_{DESAT}$ | $V_E$ to $V_E$+10V |
| "H" Peak Output Current<br>PW 10µs max, Duty Cycle 0.2% | $I_{OH(PEAK)}$ | -5A |
| "L" Level Peak Output Current<br>PW 10µs max, Duty Cycle 0.2% | $I_{OL(PEAK)}$ | 5A |
| Power Dissipation | $P_O$ | 600mW |
| Junction Temperature | $T_J$ | 125°C |
| **Total Package** | | |
| Isolation Voltage | $V_{ISO}$ | 5000$V_{RMS}$ |
| Operating Temperature | $T_{OP}$ | -40 to 100 °C |
| Storage Temperature | $T_S$ | -55 to 125 °C |
| Lead Soldering Temperature (10s) | | 260°C |

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## Truth Table

| $V_{IN+}$ | $V_{IN-}$ | UVLO ($V_{CC2} - V_E$) | DESAT | $\overline{FAULT}$ | $V_{OUT}$ |
|---|---|---|---|---|---|
| X | X | Active | X | X | Low |
| X | X | X | Yes | Low | Low |
| Low | X | X | X | X | Low |
| X | High | X | X | X | Low |
| High | Low | Not Active | No | High | High |

## Recommended Operating Conditions

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating Temperature | $T_A$ | -40 | 100 | °C |
| Input Supply Voltage | $V_{CC1}$ | 4.5 | 5.5 | V |
| Total Output Supply Voltage | $V_{CC2} - V_{EE}$ | 15 | 30 | V |
| Positive Output Supply Voltage | $V_{CC2} - V_E$ | 15 | $30 - (V_E - V_{EE})$ | V |
| Negative Output Supply Voltage | $V_E - V_{EE}$ | 0 | 15 | V |
| Source Voltage | $V_S$ | $V_{EE} + 6$ | $V_{CC2}$ | V |

## ELECTRICAL CHARACTERISTICS (Over Recommended Operating Conditions unless Otherwise Specified. All Typical Values at $V_{CC1}$ = 5V, $V_{CC2} - V_{EE}$ = 30V, $V_E - V_{EE}$ = 0V, $T_A$ = 25°C unless otherwise specified.)

### INPUT IC

| Parameter | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Logic Low Input Voltages | $V_{IN+L}$, $V_{IN-L}$, $V_{\overline{RESET}L}$ | | | | 0.8 | V |
| Logic High Input Voltages | $V_{IN+H}$, $V_{IN-H}$, $V_{\overline{RESET}H}$ | | 2.0 | | | V |
| Logic Low Input Currents | $I_{IN+L}$, $I_{IN-L}$, $I_{\overline{RESET}L}$ | $V_{IN}$ = 0.4V | -0.5 | | | mA |
| $\overline{FAULT}$ Logic Low Input Current | $I_{\overline{FAULT}L}$ | $V_{\overline{FAULT}}$ = 0.4V | 5.0 | | | mA |
| $\overline{FAULT}$ Logic High Input Current | $I_{\overline{FAULT}H}$ | $V_{\overline{FAULT}} = V_{CC1}$ | -40 | | | µA |
| High Level Input Supply Current | $I_{CC1H}$ | $V_{IN+} = V_{CC1}$ = 5.5V, $V_{IN-}$ = 0V | | | 22 | mA |
| Low Level Input Supply Current | $I_{CC1L}$ | $V_{IN+} = V_{IN-}$ = 0V, $V_{CC1}$ = 5.5V | | | 11 | mA |

**ELECTRICAL CHARACTERISTICS** (Over Recommended Operating Conditions unless Otherwise Specified. All Typical Values at $V_{CC1}$ = 5V, $V_{CC2} - V_{EE}$ = 30V, $V_E - V_{EE}$ = 0V $T_A$ = 25°C unless otherwise specified.)

## OUTPUT IC

| Parameter | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| High Level Output Current | $I_{OH}$ | $V_{OUT} = V_{CC2} - 4V$ | -2.5 | | | A |
| | | $V_{OUT} = V_{CC2} - 15V$ | -5 | | | A |
| Low Level Output Current | $I_{OL}$ | $V_{OUT} = V_{EE} + 2.5V$ | | | 2.5 | A |
| | | $V_{OUT} = V_{EE} + 15V$ | | | 5 | A |
| Low Level Output Current During Fault Condition | $I_{OLF}$ | $V_{OUT} - V_{EE} = 14V$ | 90 | | 230 | mA |
| High Level Output Voltage | $V_{OH}$ | $I_{OUT}$ = -100mA | $V_S-2$ | $V_S-1.5$ | | V |
| | | $I_{OUT}$ = -650µA | $V_S-1.5$ | $V_S-1$ | | |
| | | $I_{OUT}$ = 0 | | | $V_S$ | |
| Low Level Output Voltage | $V_{OL}$ | $I_{OUT}$ = 100mA | | | 0.5 | V |
| Output Supply Current | $I_{CC2}$ | $V_{OUT}$ = Open | | | 5 | mA |
| Low Level Source Current | $I_{SL}$ | $I_{OUT}$ = 0mA | | | 1 | mA |
| High Level Source Current | $I_{SH}$ | $I_{OUT}$ = 0mA | | | 1.3 | mA |
| | | $I_{OUT}$ = -650µA | | | 3.0 | |
| $V_E$ High Level Supply Current | $I_{EL}$ | $I_{OUT}$ = 0mA | -0.8 | -0.5 | 0 | mA |
| $V_E$ Low Level Supply Current | $I_{EH}$ | | -0.5 | -0.25 | 0 | mA |

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## OUTPUT IC

| Parameter | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Blanking Capacitor Charging Current | $I_{CHG}$ | $V_{DESAT}$ = 0 – 6V | -0.13 | | -0.33 | mA |
| | | $V_{DESAT}$ = 0 – 6V, $T_A$ = 25 – 100°C | -0.18 | | -0.33 | |
| Blanking Capacitor Discharge Current | $I_{DSCHG}$ | $V_{DESAT}$ = 7V | 10 | | | mA |
| DESAT Threshold | $V_{DESAT}$ | $V_{CC2} – V_E$ > UVLO- | 6.5 | 7.1 | 7.5 | V |
| UVLO Threshold | $V_{UVLO+}$ | $V_O$ > 5V | 11.6 | | 13.5 | V |
| | $V_{UVLO-}$ | $V_O$ < 5V | | | 12.4 | |
| UVLO Hysteresis | $UVLO_{HYS}$ | $V_{UVLO+} – V_{UVLO-}$ | 0.4 | | | V |

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## SWITCHING

| Parameter | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Propagation Delay Time to High Output Level | $t_{PLH}$ | $R_g$ = 10Ω, $C_g$ = 10nF, f = 10kHz, Duty Cycle = 50% | 100 | 220 | 500 | ns |
| Propagation Delay Time to Low Output Level | $t_{PHL}$ | | 100 | 220 | 500 | |
| Pulse Width Distortion $\|t_{PHL} - t_{PLH}\|$ for any given Device | PWD | | -100 | 50 | 100 | |
| Propagation Delay Difference ($t_{PHL} - t_{PLH}$) between any Two Devices | PDD | | -350 | | 350 | |
| Output Rise Time (10% to 90%) | $t_r$ | | | 100 | | |
| Output Fall time (90% to 10%) | $t_f$ | | | 100 | | |
| DESAT Sense to 90% $V_O$ Delay | $t_{DESAT(90\%)}$ | $R_g$ = 10Ω, $C_g$ = 10nF | | | 0.5 | µs |
| DESAT Sense to 10% $V_O$ Delay | $t_{DESAT(10\%)}$ | | | | 3 | |
| DESAT Sense to Low Level $\overline{FAULT}$ Signal Delay | $t_{DESAT(\overline{FAULT})}$ | | | | 5 | |
| DESAT Sense to DESAT Low Propagation Delay | $t_{DESAT(LOW)}$ | | | 0.25 | | |
| $\overline{RESET}$ to High Level FAULT Signal Delay | $t_{\overline{RESET}(\overline{FAULT})}$ | | 3 | | 20 | |
| $\overline{RESET}$ Signal Pulse Width | $PW_{\overline{RESET}}$ | | 0.1 | | | |
| UVLO to $V_{OUT}$ High Delay | $t_{UVLO\ ON}$ | $V_{CC2}$ = 1.0ms Ramp | | | 4.0 | |
| UVLO to $V_{OUT}$ Low Delay | $t_{UVLO\ OFF}$ | | | | 6.0 | |

## ELECTRICAL CHARACTERISTICS (Over Recommended Operating Conditions unless Otherwise Specified. All Typical Values at $V_{CC1}$ = 5V, $V_{CC2} - V_{EE}$ = 30V, $V_E - V_{EE}$ = 0V $T_A$ = 25°C unless otherwise specified.)

### SWITCHING

| Parameter | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Common Mode Transient Immunity at High Level Output | $CM_H$ | $V_{CC1}$ = 5V, $V_{CC2}$ = 25V, $V_{CM}$ = 1500$V_{P-P}$, $T_A$ = 25°C | 15 | | | kV/µs |
| Common Mode Transient Immunity at Low Level Output | $CM_L$ | $V_{CC1}$ = 5V, $V_{CC2}$ = 25V, $V_{CM}$ = 1500$V_{P-P}$, $T_A$ = 25°C | 15 | | | kV/µs |

### ISOLATION

| Parameter | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Isolation Voltage | $V_{ISO}$ | R.H. ≤ 40% – 60%, $T_A$ = 25°C, t = 1 min | 5000 | | | V |
| Input - Output Resistance | $R_{I-O}$ | $V_{I-O}$ = 500VDC | | $10^9$ | | Ω |
| Input - Output Capacitance | $C_{I-O}$ | f = 1MHz, $T_A$ = 25°C | | 1.3 | | pF |

Device is considered a two terminal device : pins 1 to 8 are shorted together and pins 9 to 16 are shorted together

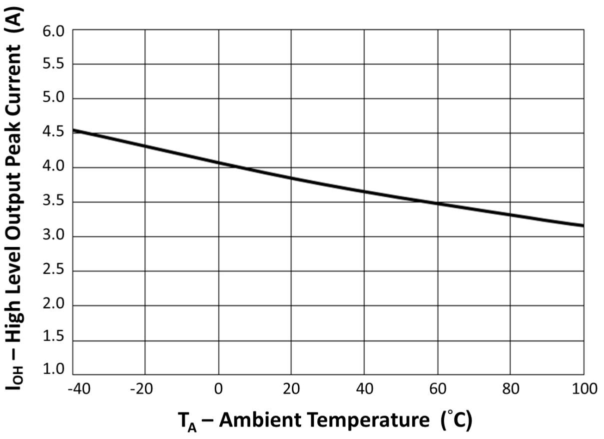



Fig 1 High Level Output Current vs Ambient Temperature

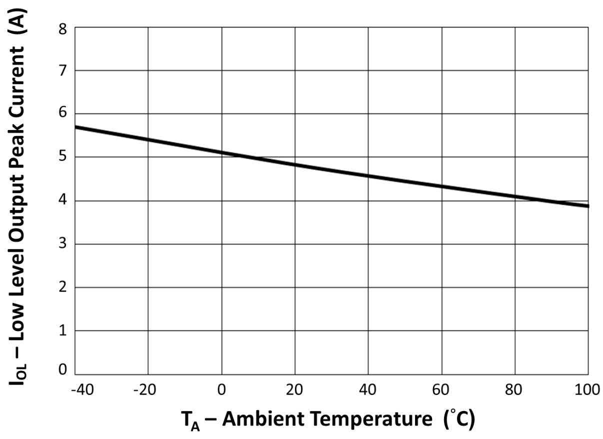



Fig 2 Low Level Output Current vs Ambient Temperature

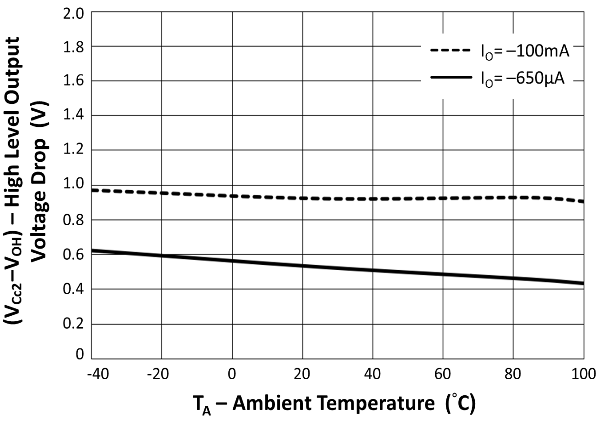



Fig 3 High Level Output Voltage Drop vs Ambient Temperature

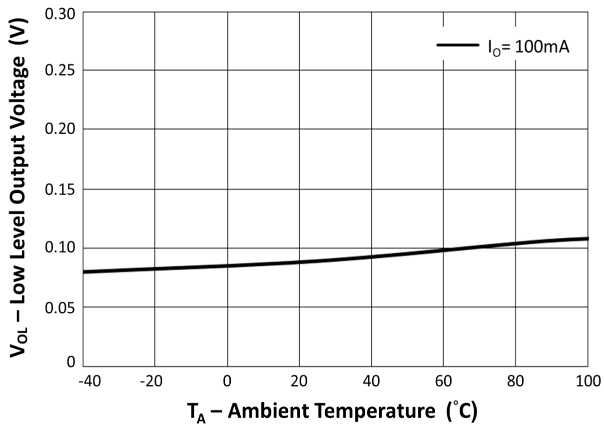



Fig 4 Low Level Output Voltage vs Ambient Temperature

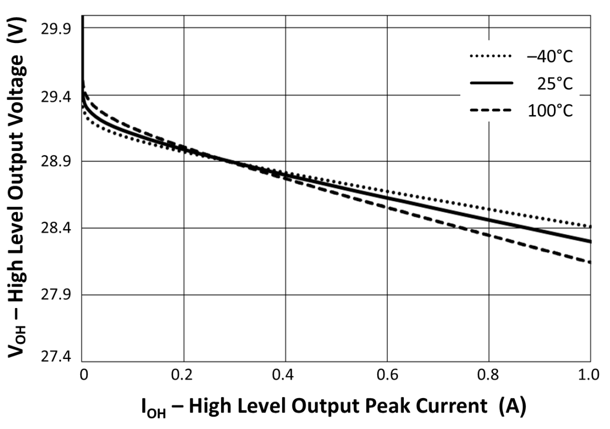



Fig 5 High Level Output Voltage vs High Level Output Current

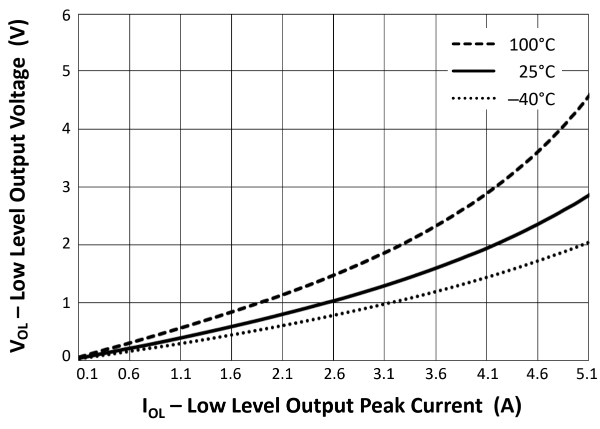



Fig 6 Low Level Output Voltage vs Low Level Output Current

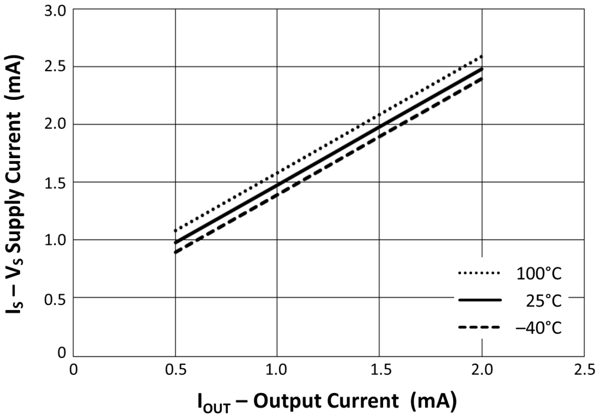



Fig 7 Source Current vs Output Current

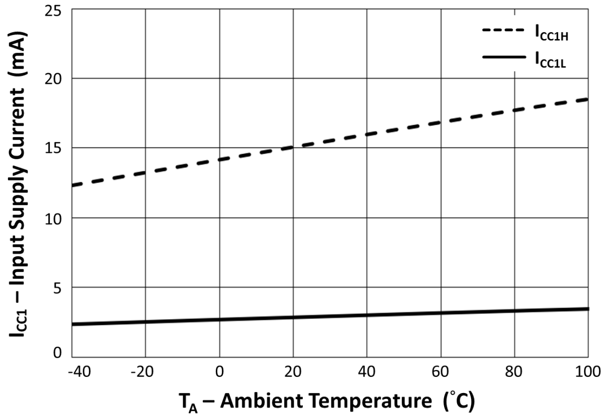



Fig 8 Input Supply Current vs Ambient Temperature

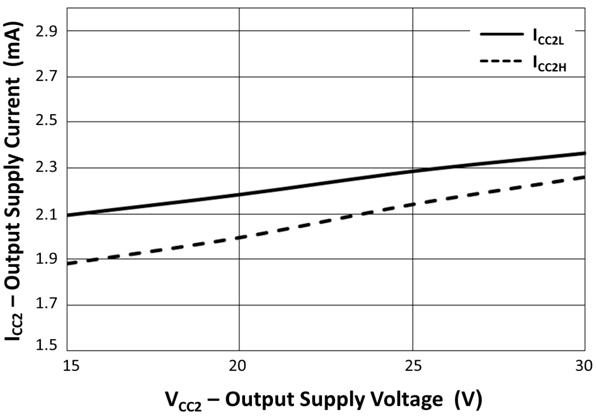



Fig 9 Output Supply Current vs Output Supply Voltage

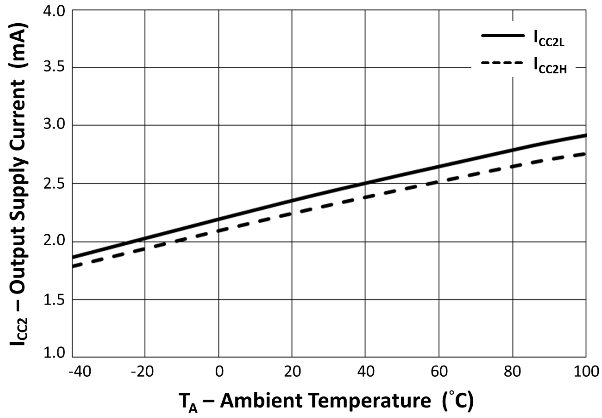



Fig 10 Output Supply Current vs Ambient Temperature

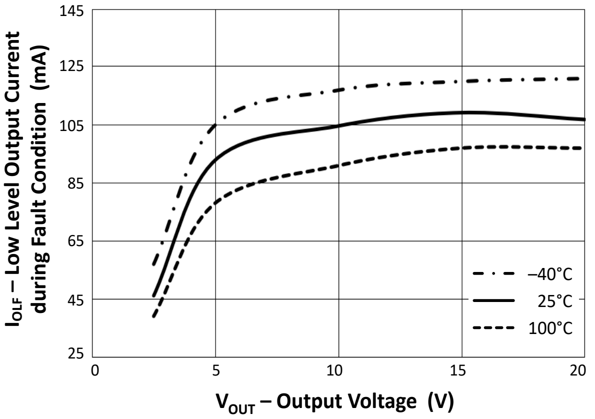



Fig 11 Low Level Output Current during Fault vs Output Voltage

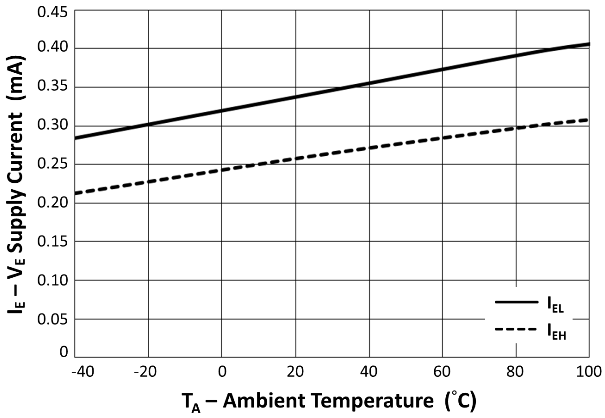



Fig 12 Supply Current ($I_E$) vs Ambient Temperature

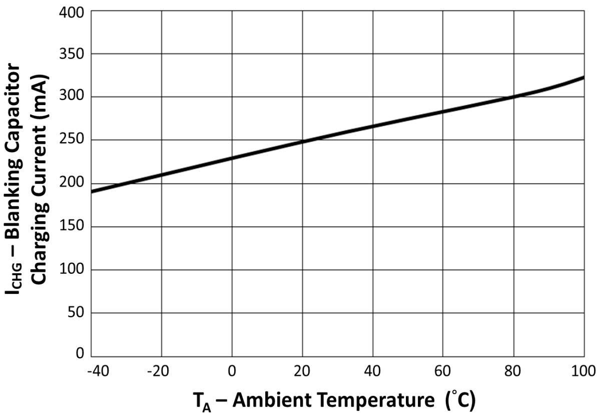



**Fig 13 Blanking Capacitor Charging Current vs Ambient Temperature**

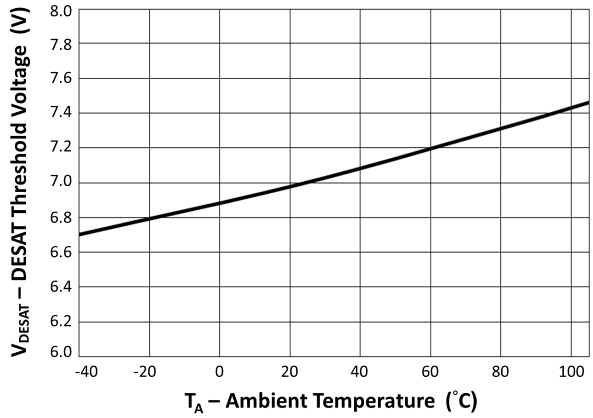



**Fig 14 DESAT Threshold Voltage vs Ambient Temperature**

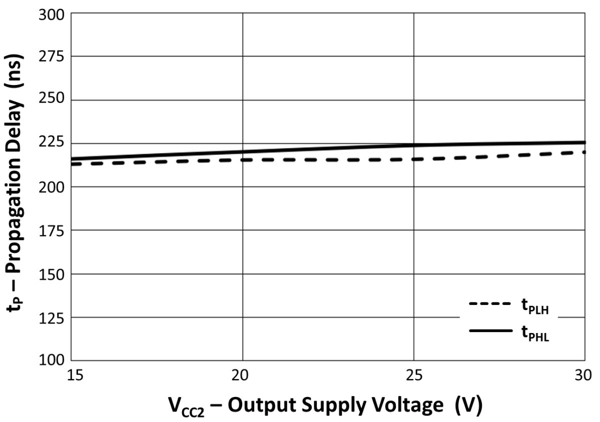



**Fig 15 Propagation Delay vs Output Supply Voltage**

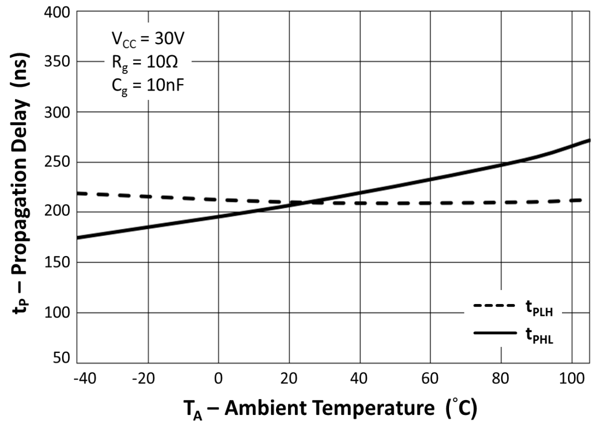



**Fig 16 Propagation Delay vs Ambient Temperature**

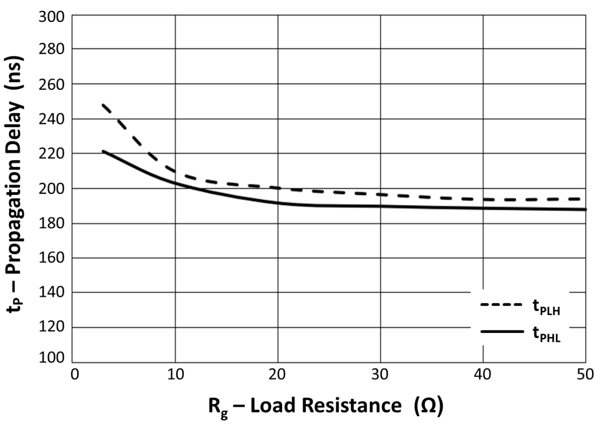



**Fig 17 Propagation Delay vs Load Resistance**

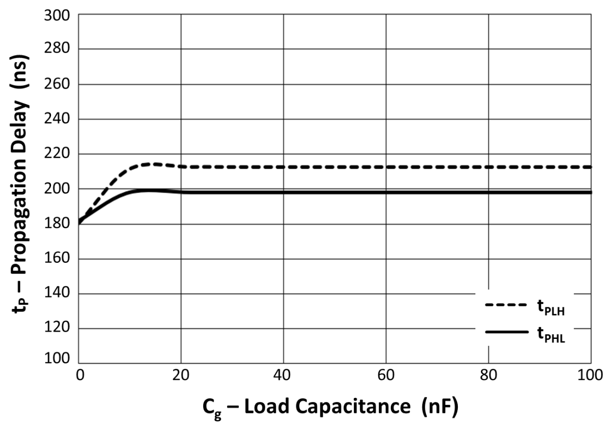



**Fig 18 Propagation Delay vs Load Capacitance**

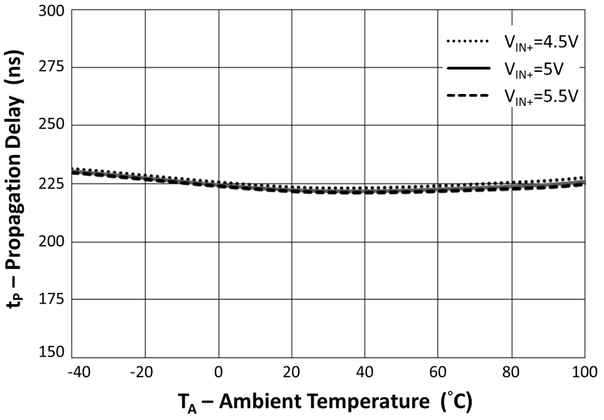



**Fig 19 $V_{IN}$ to High Output Propagation Delay vs Ambient Temperature**

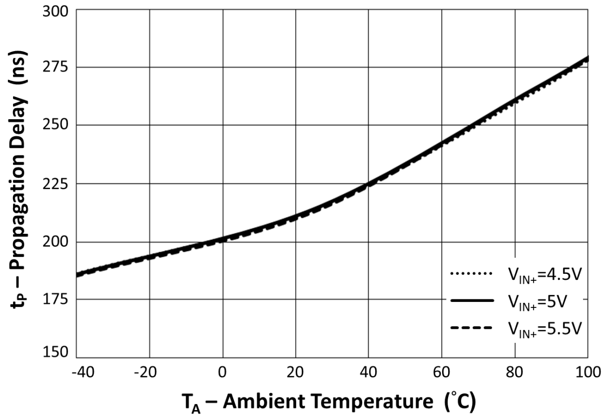



**Fig 20 $V_{IN}$ to Low Output Propagation Delay vs Ambient Temperature**

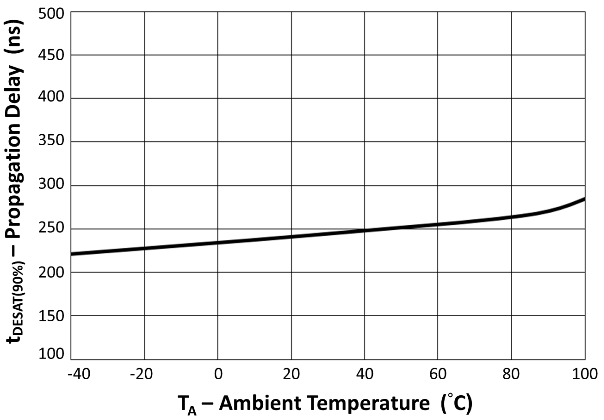



**Fig 21 DESAT Sense to 90% Output Voltage Delay vs Ambient Temperature**

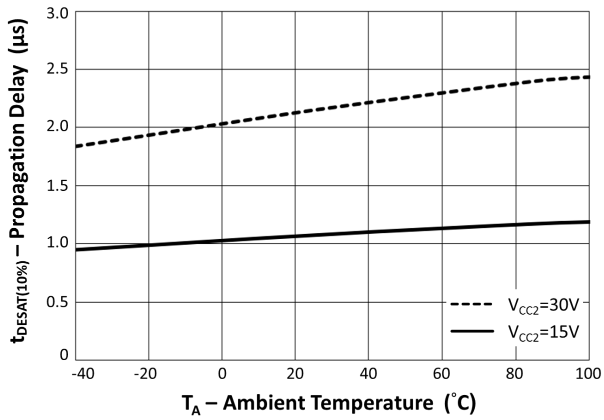



**Fig 22 DESAT Sense to 10% Output Voltage Delay vs Ambient Temperature**

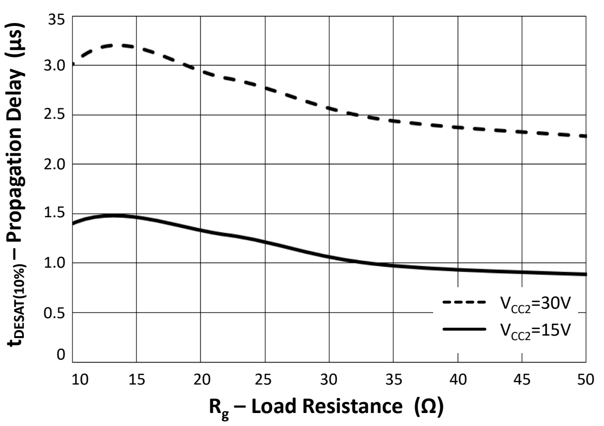



**Fig 23 DESAT Sense to 10% Output Voltage Delay vs Load Resistance**

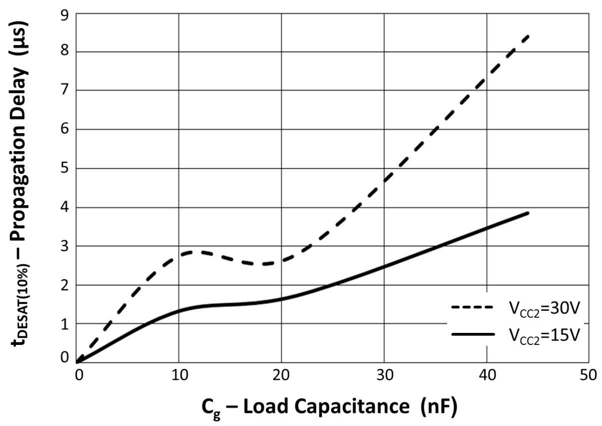



**Fig 24 DESAT Sense to 10% Output Voltage Delay vs Load Capacitance**

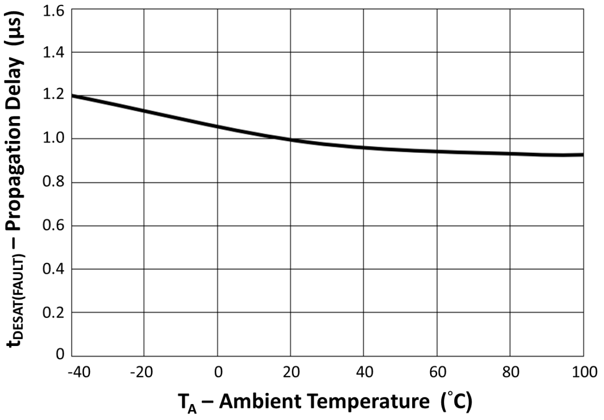



**Fig 25 DESAT Sense to Low Level $\overline{\text{FAULT}}$ Signal Delay vs Ambient Temperature**

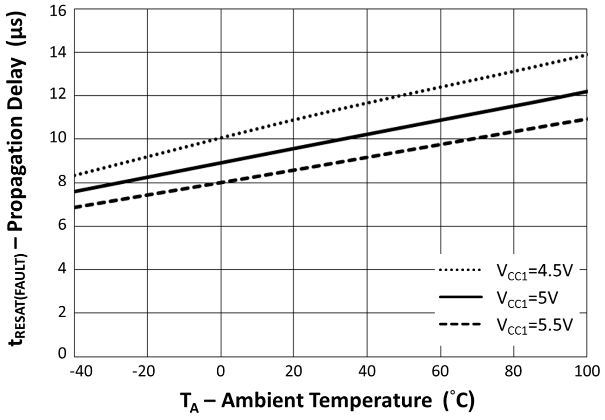



**Fig 26 RESET to High Level $\overline{\text{FAULT}}$ Signal Delay vs Ambient Temperature**

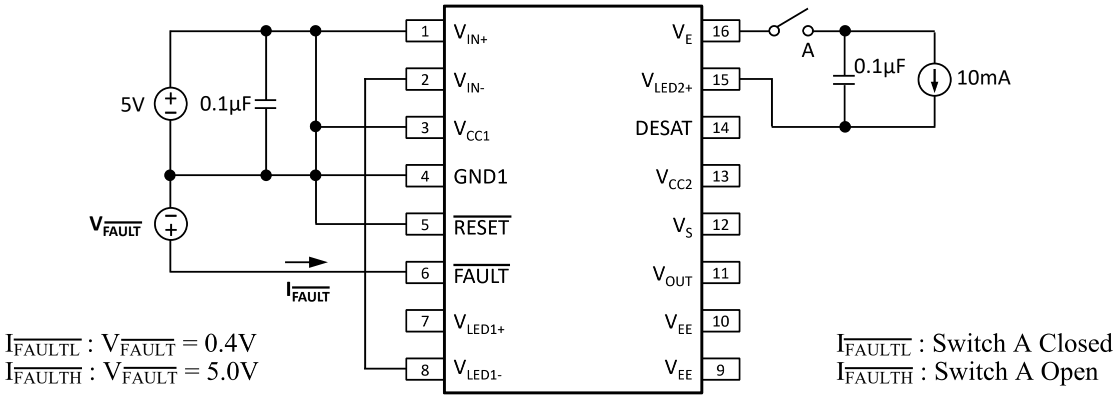



**Fig 27 Fault Output Current ($I_{\overline{FAULTL}}$ and $I_{\overline{FAULTH}}$) Test Circuit**

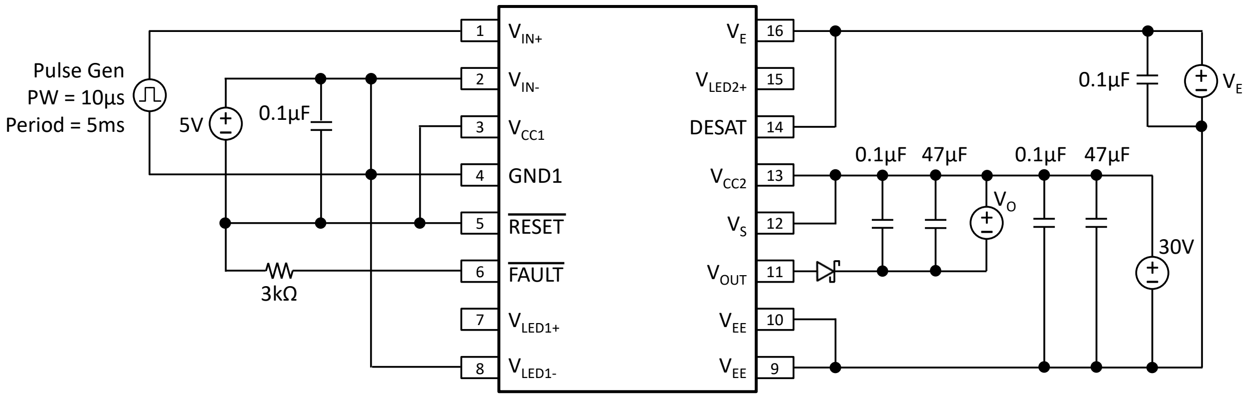



**Fig 28 High Level Output Current ($I_{OH}$) Test Circuit**

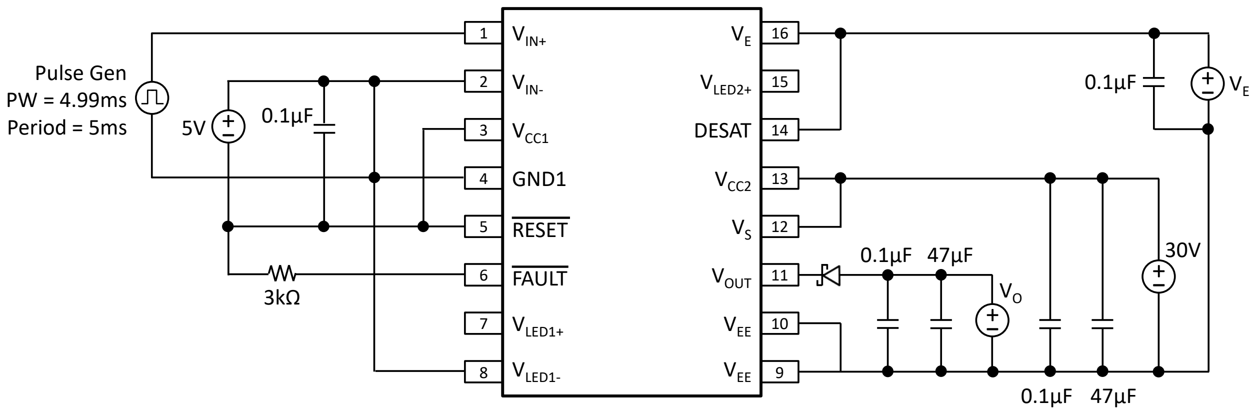



**Fig 29 Low Level Output Current ($I_{OL}$) Test Circuit**

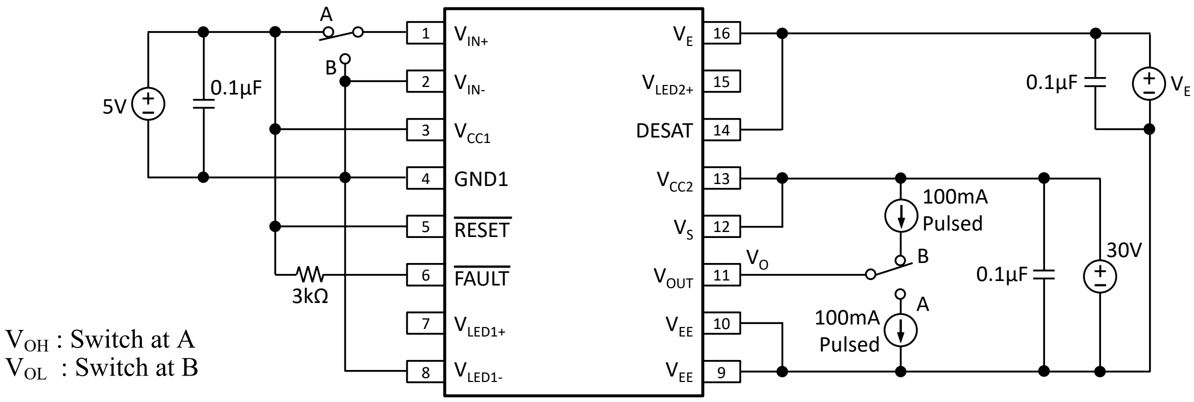



**Fig 30 Output Voltage ($V_{OH}$ and $V_{OL}$) Test Circuit**

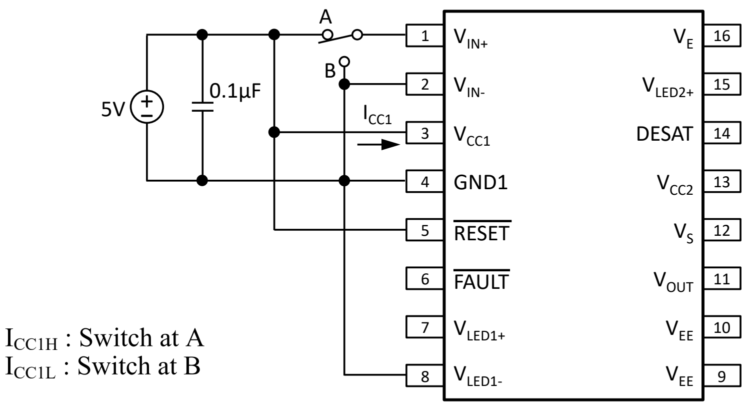



**Fig 31 Input Supply Current ($I_{CC1H}$ and $I_{CC1L}$) Test Circuit**

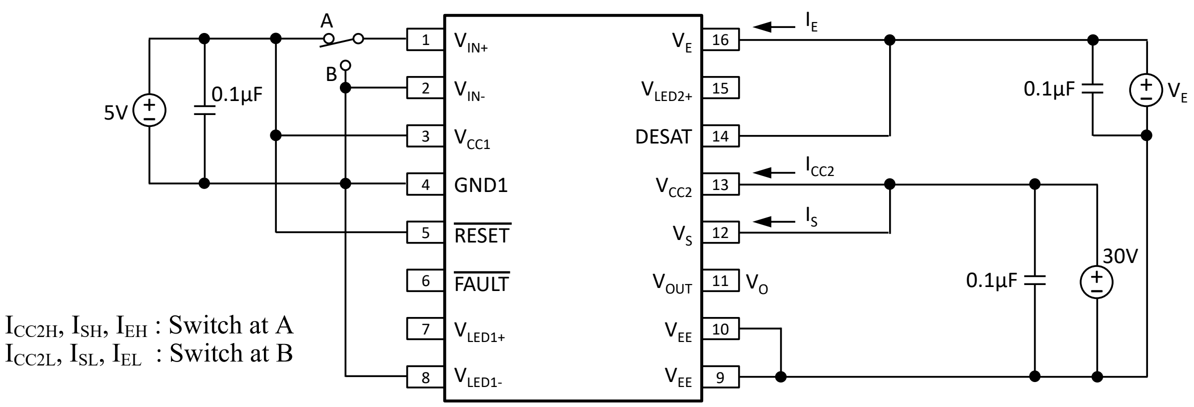



**Fig 32 Output Supply Current ($I_{CC2H}$ and $I_{CC2L}$), Source Current ($I_{SH}$ and $I_{SL}$), $V_E$ Supply Current ($I_{EH}$ and $I_{EL}$) Test Circuit**

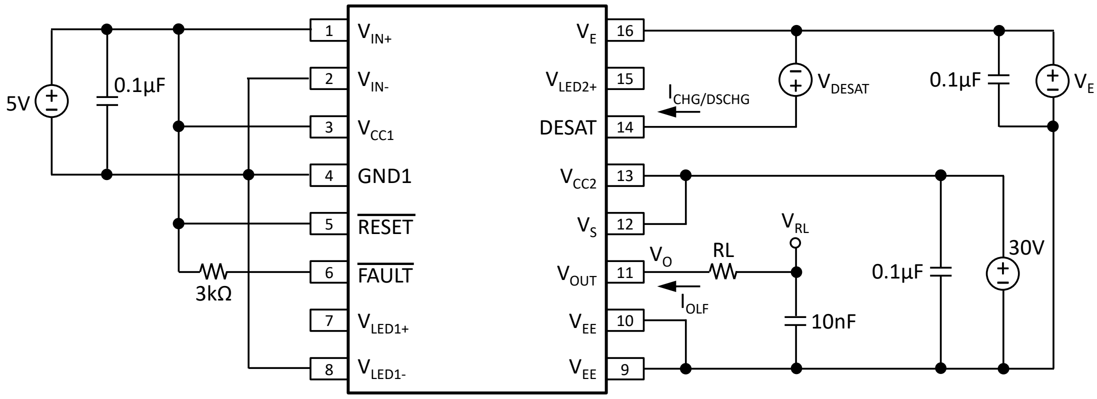



**Fig 33 Test Circuit for Low Level Output Current during Fault ($I_{OLF}$), DESAT Threshold ($V_{DESAT}$), Blanking Capacitor Charging and Discharging Current ($I_{CHG}$ and $I_{DSCHG}$)**

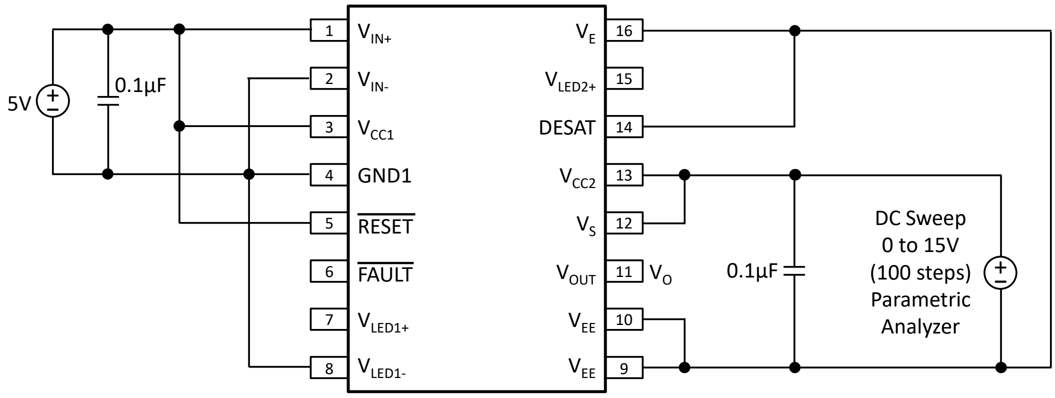



**Fig 34 Under Voltage Lockout Threshold ($V_{UVLO+}$ and $V_{UVLO-}$) Test Circuit**

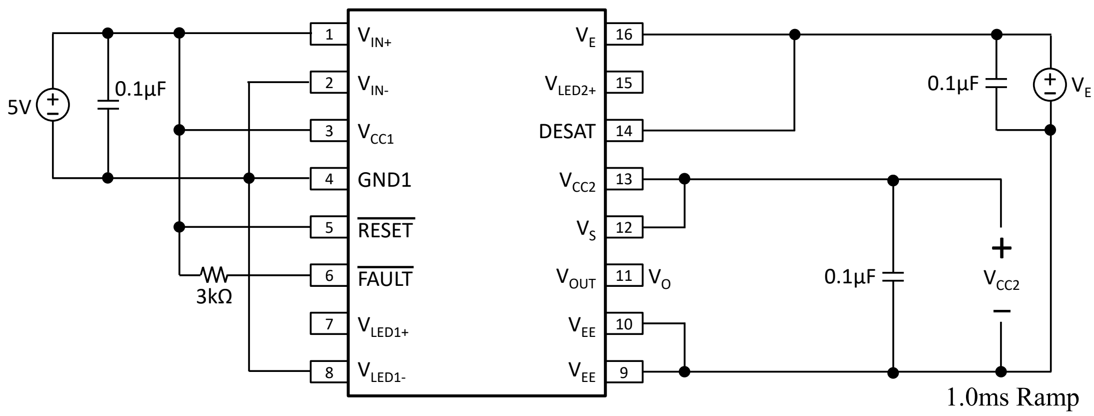



**Fig 35 Under Voltage Lockout Delay ($t_{UVLO+}$ and $t_{UVLO-}$) Test Circuit**

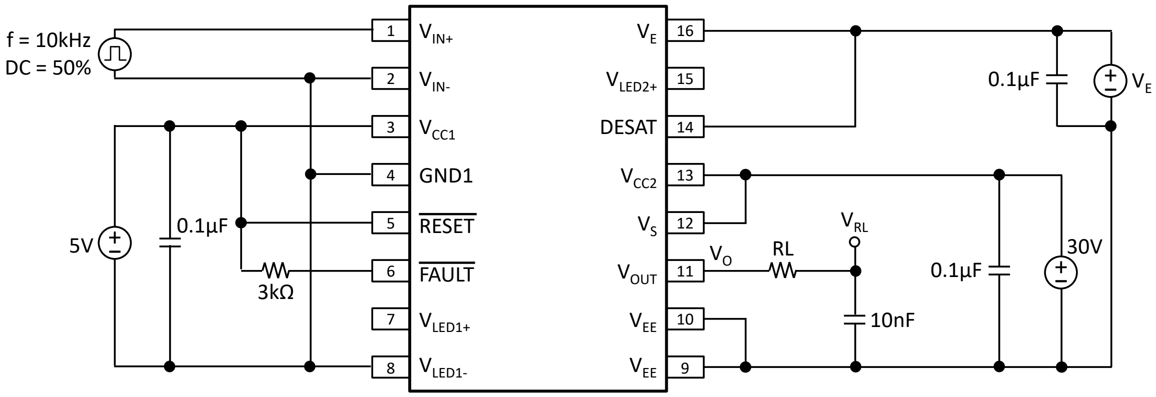



**Fig 36 Propagation Delay ($t_{PLH}$ and $t_{PHL}$), Pulse Width Distortion (PWD), Rise Time ($t_r$) and Fall Time ($t_f$) Test Circuit**

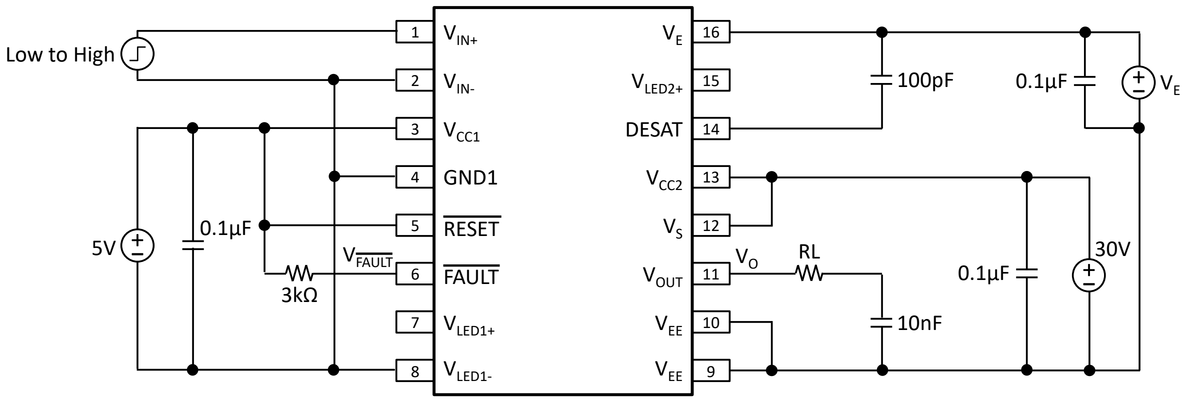



**Fig 37 Test Circuit for DESAT Sense to $V_O$ Delay ($t_{DESAT(90\%)}$ and $t_{DESAT(10\%)}$), DESAT Sense to Low Level $\overline{FAULT}$ Signal Delay ($t_{DESAT(\overline{FAULT})}$), DESAT Sense to DESAT Low Propagation Delay ($t_{DESAT(LOW)}$)**

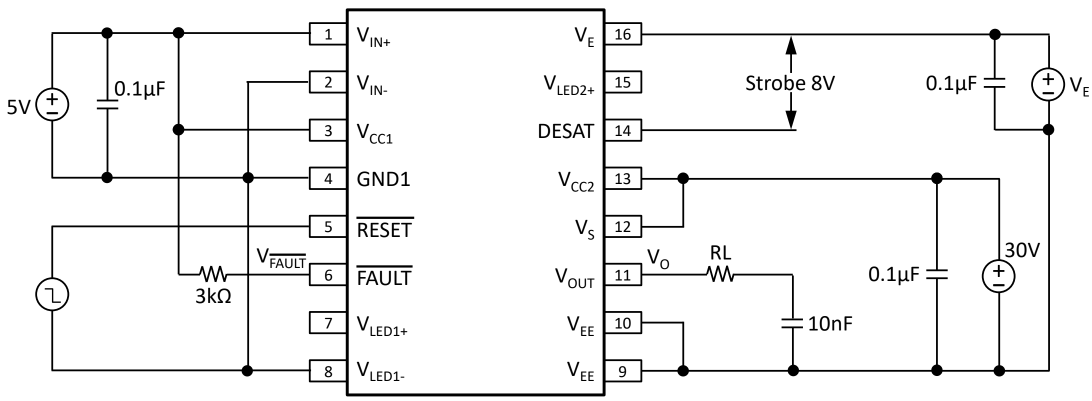



**Fig 38 Reset Delay ($t_{\overline{RESET}(\overline{FAULT})}$) Test Circuit**

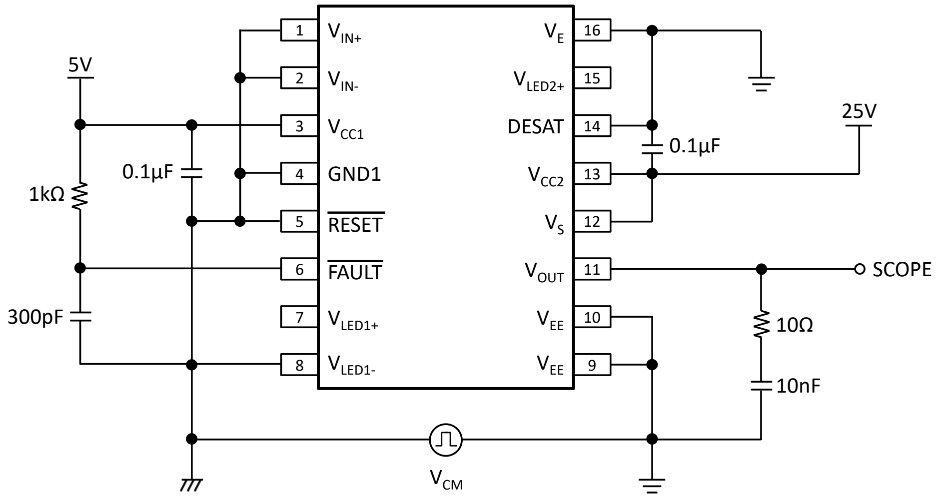



**Fig 39 Common Mode Transient Immunity at Low Level Output with LED1 OFF ($CM_L$)**

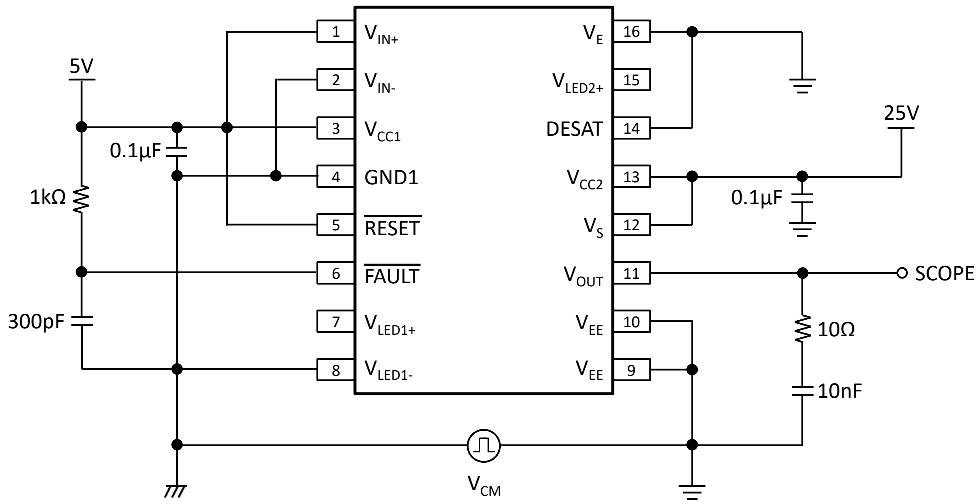



**Fig 40 Common Mode Transient Immunity at High Level Output with LED1 ON ($CM_H$)**

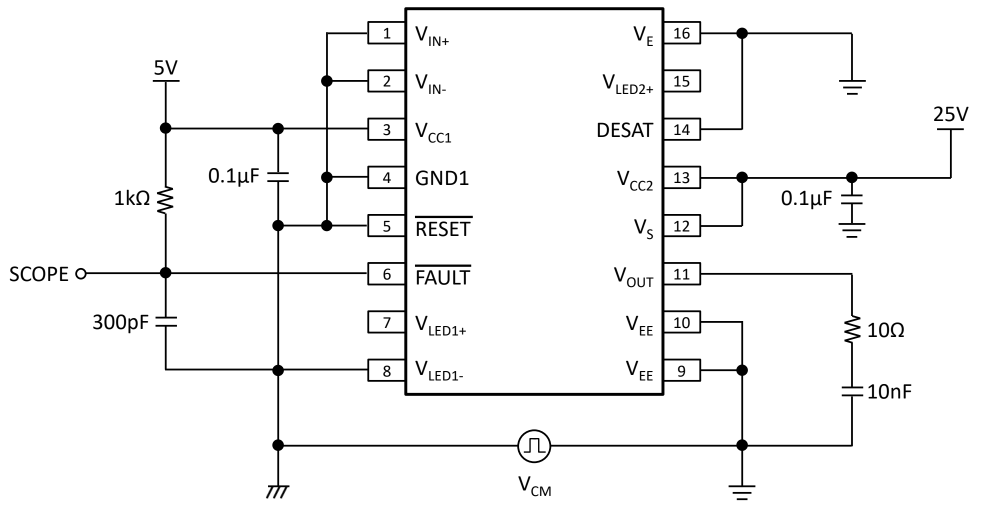



**Fig 41  Common Mode Transient Immunity at High Level Output with LED2 OFF ($CM_H$)**

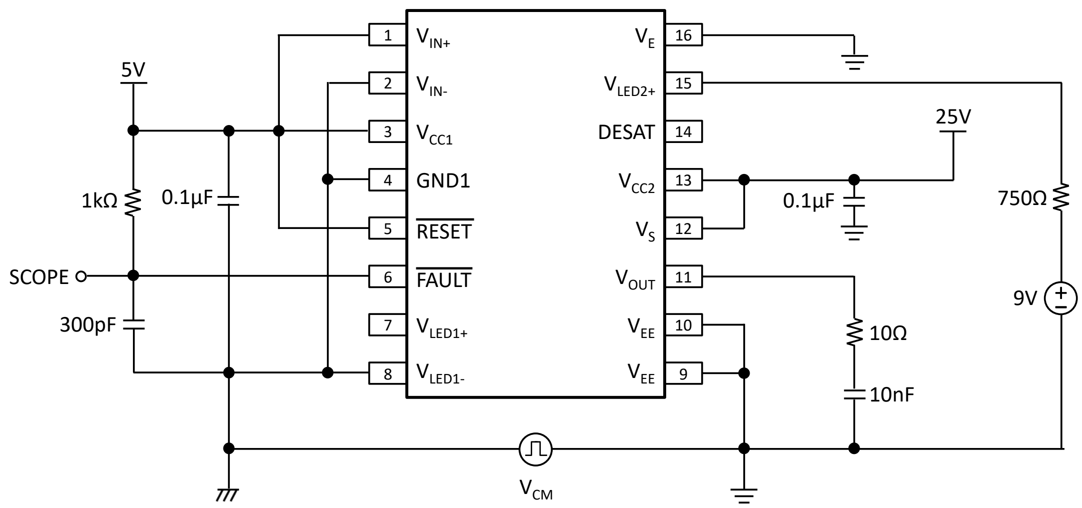
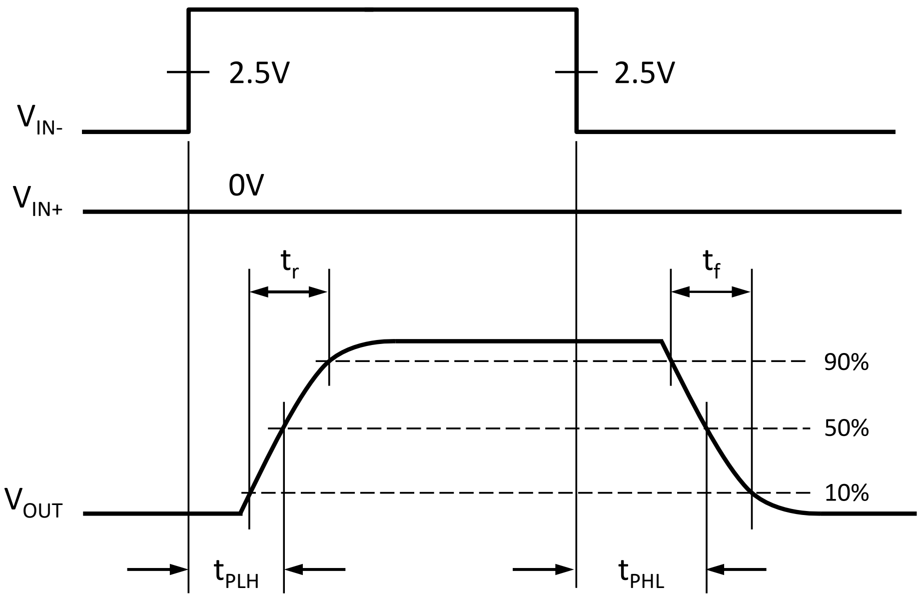
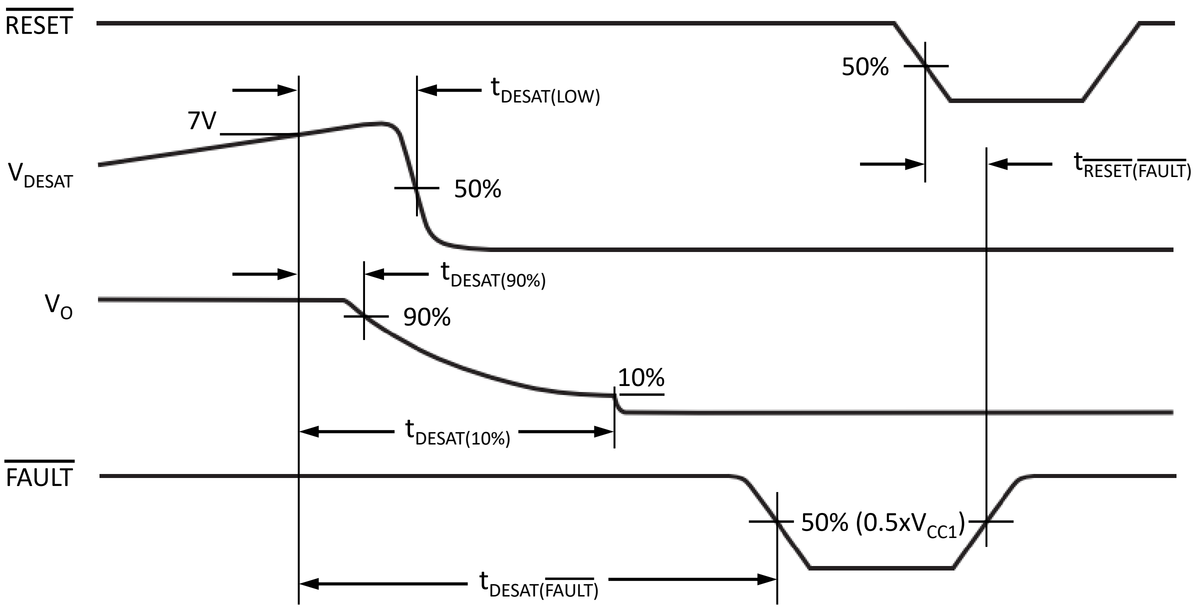



**Fig 42  Common Mode Transient Immunity at Low Level Output with LED2 ON ($CM_L$)**




**Propagation Delay ($t_{PLH}$ and $t_{PHL}$), Rise Time ($t_r$) and Fall Time ($t_f$) Timing Waveforms**




**Fault Reset Input (RESET), Desaturation Voltage Input ($V_{DESAT}$), Output Voltage ($V_O$) and Fault Output (FAULT) Timing Waveforms**

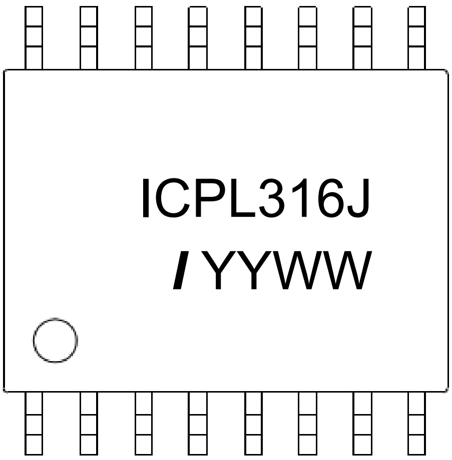
ISOCOM COMPONENTS

# ICPL316J

## ORDER INFORMATION

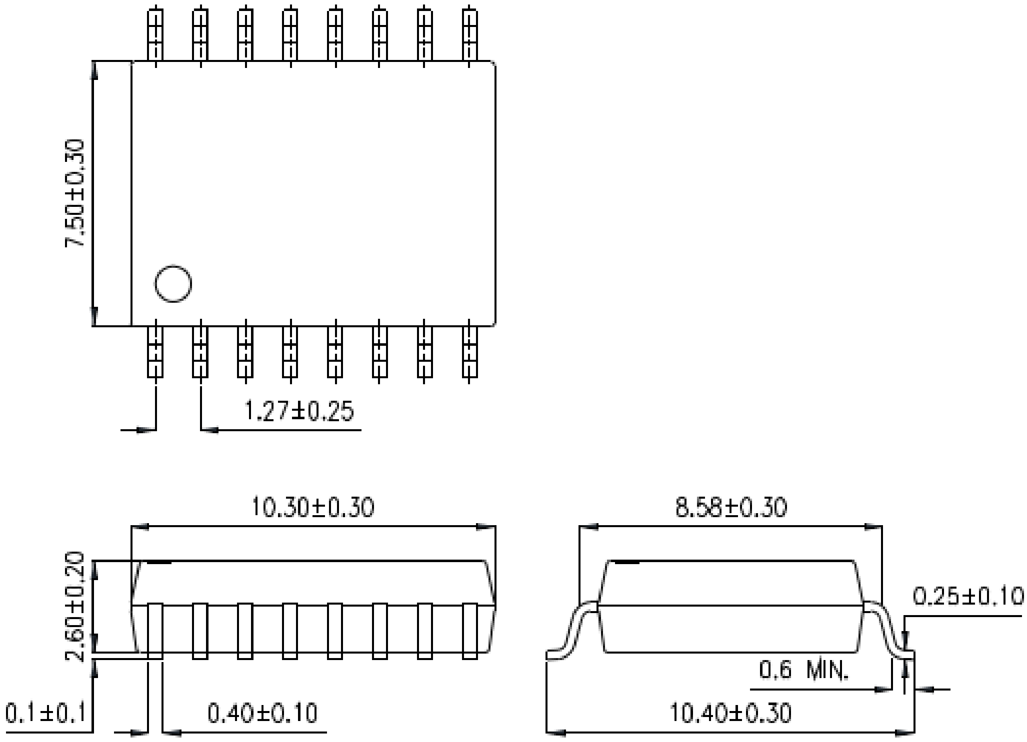
| ICPL316J | | | |
|---|---|---|---|
| **After PN** | **PN** | **Description** | **Packing quantity** |
| None | ICPL316J | Surface Mount Tape & Reel | 850 pcs per reel |

## DEVICE MARKING

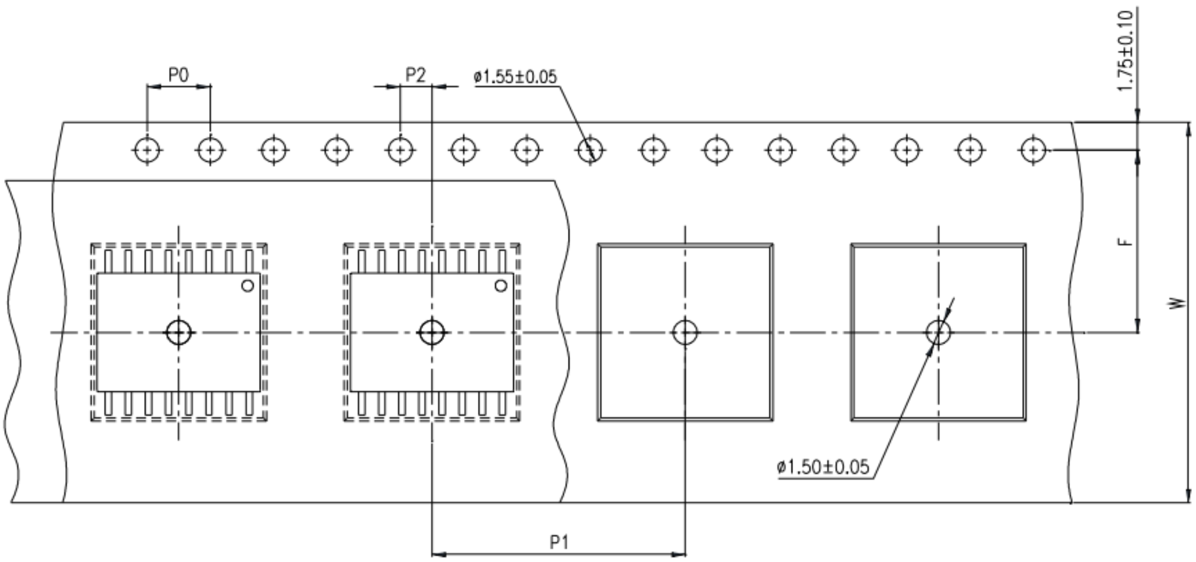


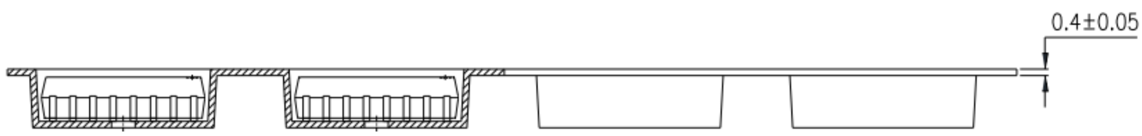

| | |
|---|---|
| ICPL316J | denotes Device Part Number |
| *I* | denotes Isocom |
| YY | denotes 2 digit Year code |
| WW | denotes 2 digit Week code |

**PACKAGE DIMENSIONS in mm (inch)**



## TAPE AND REEL PACKAGING

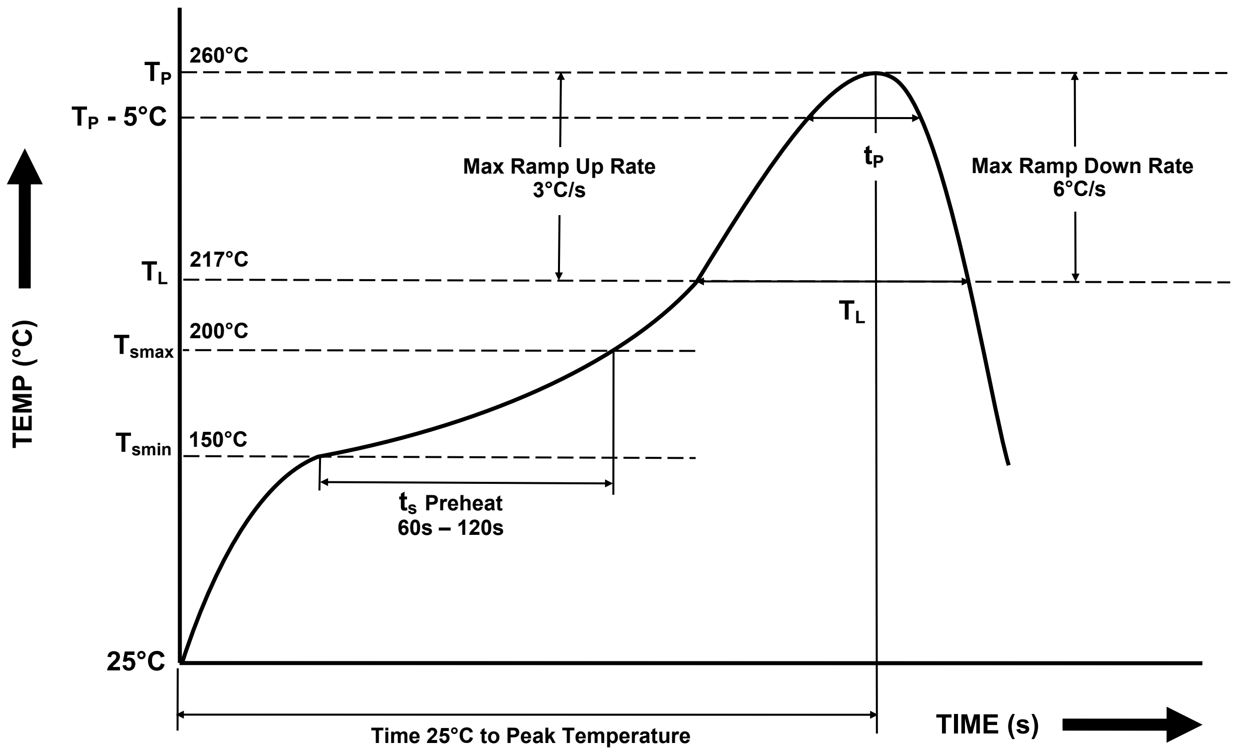



| Description | Symbol | Dimension mm (inch) |
|---|---|---|
| Tape Width | W | 24 ± 0.3 (0.94) |
| Pitch of Sprocket Holes | $P_0$ | 4 ± 0.1 (0.15) |
| Distance of Compartment to Sprocket Holes | F | 11.5 ± 0.1 (0.452) |
| | $P_2$ | 2 ± 0.1 (0.079) |
| Distance of Compartment to Compartment | $P_1$ | 16 ± 0.1 (0.63) |

## IR REFLOW SOLDERING TEMPERATURE PROFILE

**Note : One Time Reflow Soldering is Recommended.**
**Do Not Immerse Device Body in Solder Paste.**




| Profile Details | Conditions |
|---|---|
| **Preheat**<br>- Min Temperature ($T_{SMIN}$)<br>- Max Temperature ($T_{SMAX}$)<br>- Time $T_{SMIN}$ to $T_{SMAX}$ ($t_s$) | <br>150°C<br>200°C<br>60s - 120s |
| **Soldering Zone**<br>- Peak Temperature ($T_P$)<br>- Time at Peak Temperature<br>- Liquidous Temperature ($T_L$)<br>- Time within 5°C of Actual Peak Temperature ($T_P$ – 5°C)<br>- Time maintained above $T_L$ ($t_L$)<br>- Ramp Up Rate ($T_L$ to $T_P$)<br>- Ramp Down Rate ($T_P$ to $T_L$) | <br>260°C<br>10s max<br>217°C<br>30s max<br>60s - 100s<br>3°C/s max<br>6°C/s max |
| Average Ramp Up Rate ($T_{smax}$ to $T_P$) | 3°C/s max |
| Time 25°C to Peak Temperature | 8 minutes max |

ISOCOM COMPONENTS

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