ADuM1254

Bidirectional I2C Isolator with Idle-Bus Hot-Swap and Low VOL

General Description

The ADuM1254 offers two bidirectional, open-drain channels for applications, such as I²C, that require data to be transmitted in both directions on the same line. To prevent latch-up action, side 1 outputs comprise special buffers that regulate the logic-low voltage at 0.64V and the input logic-low threshold is at least 50mV lower than the output logic-low voltage. Side 2 features conventional buffers that do not regulate logic-low output voltage.

The ADuM1254 features independent 2.25V to 5.5V supplies on both side 1 and side 2 of the isolator. The device operates up to 2MHz.

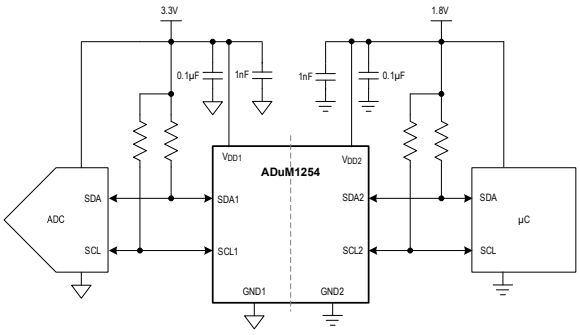
The ADuM1254 provides a disturbance-free bus connection for hot-plug connections on side 2 by first precharging the bus pins and then monitoring the bus state for either an idle bus or detection of a I²C stop condition before connecting side 1 and side 2.

The ADuM1254 is available in 8-pin narrow-body and 8-pin wide-body SOIC packages. The device is rated for operation at ambient temperatures of -40°C to +125°C.

Key Applications

- Isolated I²C/SMBus Interface
- Battery Management Systems
- Power Over Ethernet (PoE)
- Motor Control Systems

Simplified Application Diagram



Benefits and Features

- Low $V_{OL(MAX)}$ for Greater I²C Device Compatibility
  - Side 1: 0.69V
  - Side 2: 0.4V
- Independent V_{DD1}/V_{DD2} Supplies Supports 3.3V and 5V Logic Voltage Levels and Allows Level Shifting
  - 2.25V to 5.5V for Both Sides
- Enhanced Hot Swappable Side 2 I/Os
  - Initial Side 2 Connection Occurs at Bus Idle or Stop States to Prevent Data Corruption
- Bidirectional I²C Data Transfer up to 2MHz SCL
- Bidirectional SCL for Advanced Bus Topologies
  - Supports Clock Stretching and Multiple Controllers Across Isolation Barrier
- Strong Current Sinking Enables Lower $R_{PULL-UP}$ Values for Faster Bus Speeds
  - Side 1: 5mA
  - Side 2: 50mA
- Robust Galvanic Isolation of Digital Signals
  - Continuously Withstands (V_{IOWM})
    - 8 Narrow SOIC: $445V_{RMS}$
    - 8-Wide SOIC: 848 V_{RMS}
  - Withstands ±10kV Surge per IEC 61000-4-5
  - Creepage and Clearance
    - 8 Narrow SOIC: 4mm
    - 8-Wide SOIC: 8mm
- Safety and Regulatory Approvals (Pending)
  - IEC 60747-17 (Pending)
    - Reinforced V_{IORM} Narrow SOIC: $630V_{PEAK}$
    - Reinforced V_{IORM} Wide SOIC: $1200V_{PEAK}$
  - UL 1577 (Pending)
    - 8-Narrow SOIC: $3000V_{RMS}$ for 1min
    - 8-Wide SOIC: 5000 V_{RMS} for 1min
  - IEC/EN/CSA 62368-1 (Pending)
  - IEC/EN/CSA 61010-1 (Pending
  - CAN/CSA-C22.2 No. 14-18 (Pending)

Ordering Information ***appears at end of data sheet.***

19-101762; Rev 1; 5/24

Absolute Maximum Ratings

V_{DD1} to GND1 ..... -0.3V to +6.0V

V_{DD2} to GND2 ..... -0.3V to +6.0V

SDA1, SCL1 to GND1 ..... -0.3V to +6.0V

SDA2, SCL2 to GND2 ..... -0.3V to +6.0V

Short-Circuit Continuous Current

- SDA1, SCL1 to V_{DD1} 20mA
- SDA2, SCL2 to V_{DD2} 100mA

Continuous Power Dissipation

- 8 NSOIC (Derate 5.49mW/°C above +70°C) ..... +440mW
- 8 WSOIC (Derate 5.88mW/°C above +70°C)..... +471mW

Temperature

- Operating Temperature Range..... -40°C to +125°C
- Junction Temperature.....+150°C
- Storage Temperature ..... -65°C to +150°C
- Lead Temperature (Soldering, 10s) .....+300°C
- Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

8 Narrow SOIC

Outline Number	*21-0041*
Land Pattern Number	*90-0096*
Junction-to-Ambient Thermal Resistance (θ_{JA})	182°C/W
Junction-to-Case Top Thermal Resistance ($\theta_{JC(TOP)}$)	50°C/W
Junction-to-Board Thermal Resistance (θ_{JB})	63.6°C/W
Junction-to-Case Top Thermal Characterization Parameter (ψ_{JT})	8°C/W
Junction-to-Board Thermal Characterization Parameter (ψ_{JB})	60°C/W
Moisture Sensitivity Level	3

8 Wide SOIC

Outline Number	21-100415
Land Pattern Number	90-100146
Junction-to-Ambient Thermal Resistance (θ_{JA})	170°C/W
Junction-to-Case Top Thermal Resistance ($\theta_{JC(TOP)}$)	64°C/W
Junction-to-Board Thermal Resistance (θ_{JB})	60.9°C/W
Junction-to-Case Top Thermal Characterization Parameter (ψ_{JT})	12°C/W
Junction-to-Board Thermal Characterization Parameter (ψ_{JB})	62°C/W
Moisture Sensitivity Level	3

For the latest package outline information and land patterns (footprints), go to www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.
Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.

Electrical Characteristics

(V_{DD1} - V_{GND1} = +2.25V to +5.5V, V_{DD2} - V_{GND2} = +2.25V to +5.5V, C_L = 20pF, T_A = -40°C to +125°C, unless otherwise noted (Note 1, Note 2). Typical values are at V_{DD1} - V_{GND1} = 3.3V, V_{DD2} - V_{GND2} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage	V_{DD1}	Relative to GND1		2.25		5.5	V
	V_{DD2}	Relative to GND2		2.25		5.5	
Undervoltage-Lockout Threshold Side_	$V_{UVLO\_}$	$V_{DD\_}$ rising		1.48	1.6	1.65	V
Undervoltage-Lockout Threshold Hysteresis	V_{UVLO_HYST}	(Note 5)			30		mV
SUPPLY CURRENT (Note 2, Note 3)							
Supply Current Side 1	I_{DD1}	V_{DD1} = V_{DD2} = 2.25V - 5V				1	mA
Supply Current Side 2	I_{DD2}	V_{DD1} = V_{DD2} = 2.25V - 5V				1	mA
LOGIC INPUTS AND OUTPUTS							
Input High Voltage, SDA1/SCL1	V_{IH1}	Relative to GND1		0.52	0.56	0.62	V
Input Low Voltage, SDA1/SCL1	V_{IL1}	Relative to GND1		0.47	0.51	0.56	V
Input Hysteresis, Side 1	V_{HYS1}	V_{IH1} - V_{IL1}	(Note 5)		50		mV
Output Low Voltage, SDA1/SCL1	V_{OL1}	Relative to GND1	I = 0.1mA - 5mA sink	0.59	0.64	0.69	V
Low-level Output Voltage to High-Level Input Voltage Threshold Difference, Side 1	$\Delta V_{O/IT}$	SDA1/SCL1, V_{OL} - V_{IH}	(Note 4)	45			mV
Input High Voltage, Side 2	V_{IH2}	SDA2/SCL2 to GND2		0.52 x V_{DD2}	0.45 x V_{DD2}		V
Input Low Voltage, Side 2	V_{IL2}	SDA2/SCL2 to GND2			0.38 x V_{DD2}	0.3 x V_{DD2}	V

(V_{DD1} - V_{GND1} = +2.25V to +5.5V, V_{DD2} - V_{GND2} = +2.25V to +5.5V, C_L = 20pF, T_A = -40°C to +125°C, unless otherwise noted (Note 1, Note 2). Typical values are at V_{DD1} - V_{GND1} = 3.3V, V_{DD2} - V_{GND2} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Hysteresis, Side 2	V_{HYS2}	V_{IH2} - V_{IL2}			0.07 x V_{DD2}		V
Output Low Voltage, Side 2	V_{OL2}	SDA2/SCL2 to GND2	I = 50mA sink			0.4	V
Static Output Loading	$I_{SDA1/SCL1}$	Side 1		0.1		5	mA
	$I_{SDA2/SCL2}$	Side 2		0.1		50	
Leakage Current	I_L	Device unpowered	SDA1/SCL1 = 5.5V, VDD1 = 0V	-10		+10	µA
			SDA2/SCL2 = 5.5V, VDD2 = 0V	-10		+10	
		Device powered	SDA1 = SCL1 = VDD1 = 5.5V	-10		+10	
		Device powered and not in precharge	SDA2 = SCL2 = VDD2 = 5.5V	-10		+10	
Input Capacitance	C_{IN}	f = 1MHz	(Note 5)		5		pF
ESD Protection (Note 5)							
ESD		Human Body Model	V_{DD1} to same side pins, V_{DD2} to same side pins	±8			kV
			SDA1/SCL1 to GND1	±17			
			SDA2/SCL2 to GND2	±17			
		IEC 61000-4-2 contact discharge	SDA1/SCL1 to GND1 unpowered	±8			
			SDA2/SCL2 to GND2 unpowered	±8			
		IEC 61000-4-2 contact discharge (GND2 to GND1)	8 Wide SOIC	±5			
			8 Narrow SOIC	±5			

Dynamic Characteristics

(V_{DD1} - V_{GND1} = 2.25V to 5.5V, V_{DD2} - V_{GND2} = 2.25V to 5.5V, C_L = 20pF, T_A = -40°C to +125°C, unless otherwise noted. (Note 5) Typical values are at V_{DD1} - V_{GND1} = 3.3V, V_{DD2} - V_{GND2} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	CMTI	(Note 6)		100			kV/µs
Maximum Data Rate	DR_{MAX}			2			MHz
Fall Time	t_{F1}	SDA1/SCL1 = 0.7 x V_{DD1} to 0.3 x V_{DD1}	4.5V ≤ V_{DD1} ≤ 5.5V, C_{L1} = 40pF, R_1 = 1.6kΩ	8.8	20.3	36.1	ns
			3.0V ≤ V_{DD1} ≤ 3.6V, C_{L1} = 40pF, R_1 = 1kΩ	6.1	13.7	24.1	
			2.25V ≤ V_{DD1} ≤ 2.75V, C_{L1} = 40pF, R_1 = 810Ω	4.6	10.4	18.5	

(V_{DD1} - V_{GND1} = 2.25V to 5.5V, V_{DD2} - V_{GND2} = 2.25V to 5.5V, C_L = 20pF, T_A = -40°C to +125°C, unless otherwise noted. (*Note 5*)
Typical values are at V_{DD1} - V_{GND1} = 3.3V, V_{DD2} - V_{GND2} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		SDA1/SCL1 = 0.9 x V_{DD1} to 0.9V	4.5V ≤ V_{DD1} ≤ 5.5V, C_{L1} = 40pF, R_1 = 1.6kΩ	15.4	34.7	64.7	
			3.0V ≤ V_{DD1} ≤ 3.6V, C_{L1} = 40pF, R_1 = 1kΩ	9.1	19.7	35.9	
			2.25V ≤ V_{DD1} ≤ 2.75V, C_{L1} = 40pF, R_1 = 810Ω	6.0	12.2	23.3	
	t_{F2}	SDA2/SCL2 = 0.7 x V_{DD2} to 0.3 x V_{DD2}	4.5V ≤ V_{DD2} ≤ 5.5V, C_{L2} = 400pF, R_2 = 180Ω	11.8	18.6	30.0	
			3.0V ≤ V_{DD2} ≤ 3.6V, C_{L2} = 400pF, R_2 = 120Ω	9.0	13.8	21.0	
			2.25V ≤ V_{DD2} ≤ 2.75V, C_{L2} = 400pF, R_2 = 91Ω	7.6	11.6	17.0	
		SDA2/SCL2 = 0.9 x V_{DD2} to 0.4V	4.5V ≤ V_{DD2} ≤ 5.5V, C_{L2} = 400pF, R_2 = 180Ω	25.7	41.0	63.0	
			3.0V ≤ V_{DD2} ≤ 3.6V, C_{L2} = 400pF, R_2 = 120Ω	19.0	29.0	44.4	
			2.25V ≤ V_{DD2} ≤ 2.75V, C_{L2} = 400pF, R_2 = 91Ω	15.5	24.0	36.3	
Propagation Delay	t_{PLH12}	SDA1/SCL1 = 0.66V to SDA2/SCL2 = 0.7 x V_{DD2}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V, C_{L1} = 20pF, R_1 = 1.6kΩ, C_{L2} = 20pF, R_2 = 180Ω		37.6	50.0	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V, C_{L1} = 20pF, R_1 = 1kΩ, C_{L2} = 20pF, R_2 = 120Ω		35.9	48.0	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V, C_{L1} = 20pF, R_1 = 810Ω, C_{L2} = 20pF, R_2 = 91Ω		35.2	47.0	
	t_{PHL12}	SDA1/SCL1 = 0.425V to SDA2/SCL2 = 0.3 x V_{DD2}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V, C_{L1} = 20pF, R_1 = 1.6kΩ, C_{L2} = 20pF, R_2 = 180Ω		93.7	133.3	
			3.0V ≤ $V_{DD1\_}$ ≤ 3.6V, C_{L1} = 20pF, R_1 = 1kΩ, C_{L2} = 20pF, R_2 = 120Ω		84.2	116.4	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V, C_{L1} =10pF,		78.8	107.3	

(V_{DD1} - V_{GND1} = 2.25V to 5.5V, V_{DD2} - V_{GND2} = 2.25V to 5.5V, C_L = 20pF, T_A = -40°C to +125°C, unless otherwise noted. (*Note 5*)
Typical values are at V_{DD1} - V_{GND1} = 3.3V, V_{DD2} - V_{GND2} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			R_1 = 810Ω, C_{L2} = 20pF, R_2 = 91Ω				
	t_{PLH21}	SDA2/SCL2 = 0.5 x V_{DD2} to SDA1/SCL1 = 0.7 x V_{DD1}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V, C_{L1} = 20pF, R_1 = 1.6kΩ, C_{L2} = 20pF, R_2 = 180Ω		86.7	95.8	
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V, C_{L1} = 20pF, R_1 = 1kΩ, C_{L2} = 20pF, R_2 = 120Ω		67.3	76.3	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V, C_{L1} = 20pF, R_1 = 810Ω, C_{L2} = 20pF, R_2 = 91Ω		61.0	70.1	
	t_{PHL21}	SDA2/SCL2 = 0.3 x V_{DD2} to SDA1/SCL1 = 0.3 x V_{DD1}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V, C_{L1} = 20pF, R_1 = 1.6kΩ, C_{L2} = 20pF, R_2 = 180Ω		82.6	128.4	
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V, C_{L1} = 20pF, R_1 = 1kΩ, C_{L2} = 20pF, R_2 = 120Ω		69.9	101.0	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V, C_{L1} = 20pF, R_1 = 810Ω, C_{L2} = 20pF, R_2 = 91Ω		65.1	88.9	
Pulse-Width Distortion	PWD_{12}	$\lvert t_{PLH12} - t_{PHL12} \rvert$	4.5V ≤ $V_{DD\_}$ ≤ 5.5V		56.1	94.2	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V		48.3	79.0	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V		43.6	70.6	
	PWD_{21}	$\lvert t_{PLH21} - t_{PHL21} \rvert$	4.5V ≤ $V_{DD\_}$ ≤ 5.5V		5.9	50.7	
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V		12.6	43.1	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V		14.1	37.6	
Round-Trip Propagation Delay on Side 1	t_{LOOP1}	SDA1/SCL1 = 0.425V to SDA1/SCL1 = 0.3 x V_{DD1}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V, C_{L1} = 40pF, R_1 = 1.6kΩ, C_{L2} = 400pF, R_2 = 180Ω		142.2	163.2	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V, C_{L1} = 40pF, R_1 = 1kΩ, C_{L2} = 400pF, R_2 = 120Ω		114.1	133.5	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V, C_{L1} = 40pF, R_1 = 810Ω, C_{L2} = 400pF, R_2 = 91Ω		101.3	122.8	
Side 1 Time from UVLO to Active State	t_{ACT}	V_{DD1} rising, V_{DD2} powered up for more than t_{HS_EN} and SDA_/SCL_ high			1.1	1.7	ms

(V_{DD1} - V_{GND1} = 2.25V to 5.5V, V_{DD2} - V_{GND2} = 2.25V to 5.5V, C_L = 20pF, T_A = -40°C to +125°C, unless otherwise noted. (*Note 5*)
Typical values are at V_{DD1} - V_{GND1} = 3.3V, V_{DD2} - V_{GND2} = 3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Power Loss to Output High-Z	t_{Hi-Z}	Opposite $V_{DD\_}$ falling below $V_{UVLO\_}$				0.4	ms
HOT SWAP/BUS STUCK TIMER, SIDE 2							
Precharge Voltage	V_{PRECHG}	SDA2/SCL2 open, V_{DD2} > 0.6V	At power-up		0.3 x V_{DD2}		V
Precharge Thevenin Equivalent Impedance	R_{PRECHG}	SDA2/SCL2 open, V_{DD2} > 0.6V	At power-up		140		kΩ
Precharge Glitch Filter on SDA2/SCL2	t_{PRE_GLITCH}	V_{DD2} rising above $V_{UVLO\_}$	At power-up		220		ns
Hot-Swap Detection Enable Time	t_{HS_EN}	At power-up			102		ms
SDA2/SCL2 Idle Detection Time	t_{IDLE}	After t_{HS_EN}	At power-up		75		µs
Bus Stuck Timeout	t_{STUCK}	Either SDA1 or SCL1 low			102		ms

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 2: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GND1 or GND2), unless otherwise noted.

Note 3: The supply current does not include any current entering the SDA_/SCL_ pins. Current is after successful hot-swap connection. R_1 = R_2 = 1kΩ, C_{L1} = C_{L2} = 10pF.

Note 4: This is the minimum difference between the output logic-low level and the input logic threshold. This ensures that there is no possibility of the part latching up the bus to which it is connected.

Note 5: Not production tested. Guaranteed by design.

Note 6: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining operation. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GND1 and GND2 (V_{CM} = 1000V).

Timing Diagrams

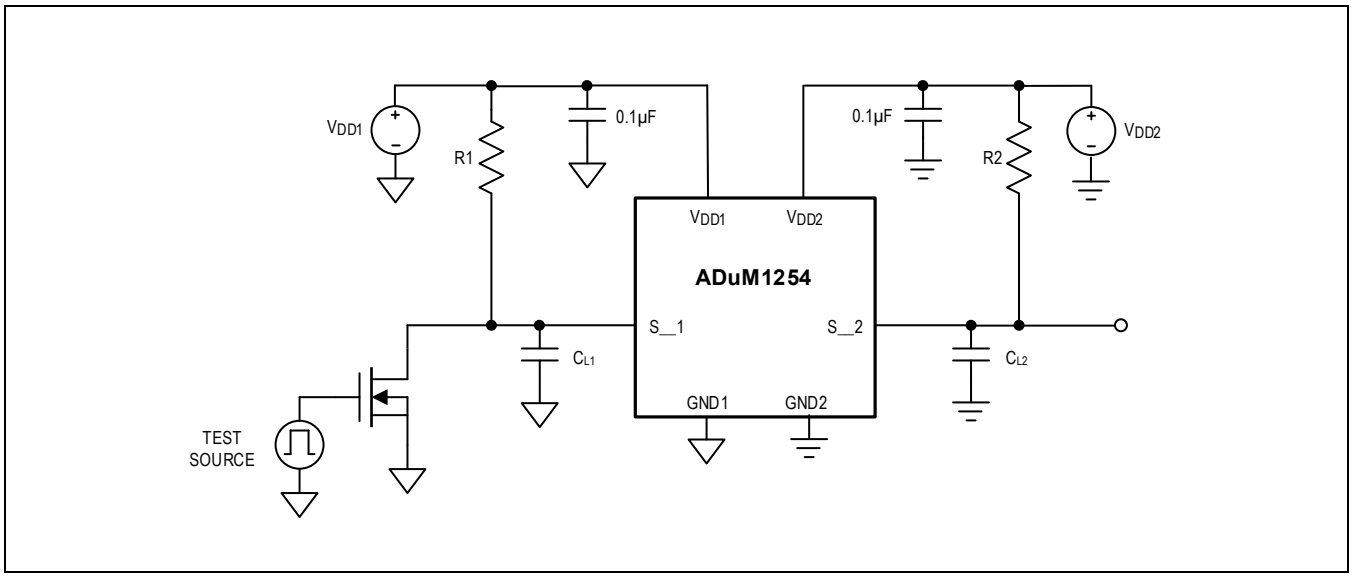


Figure 1. Timing Test Diagram

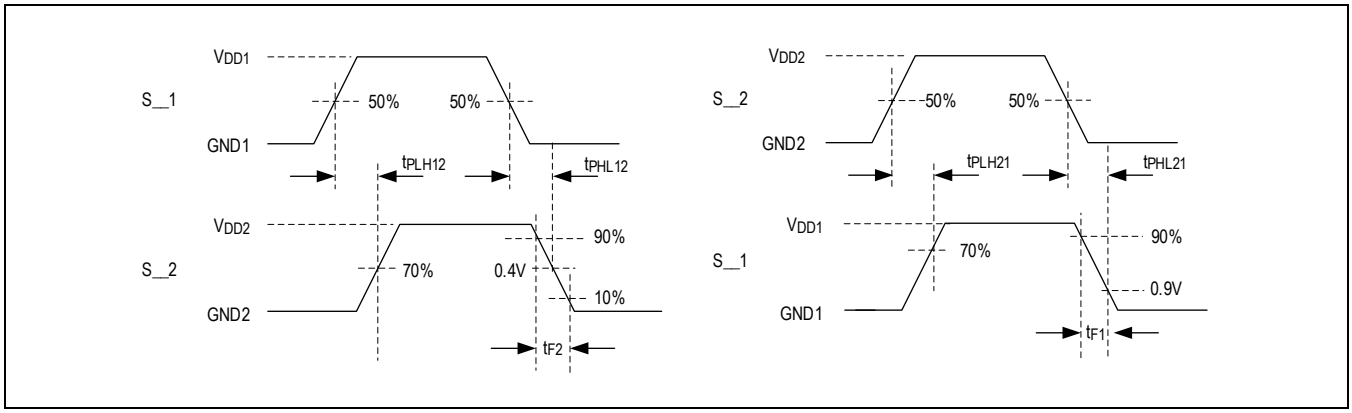


Figure 2. Timing Parameter Definition

Safety Limits

Damage to the IC can result in a low-resistance path to ground or to the supply and, without current limiting, the ADuM1254 can dissipate excessive amounts of power. Excessive power dissipation can damage the die and result in damage to the isolation barrier, potentially causing downstream issues. The safety limits for the ADuM1254 are listed in the package specific *Isolation Characteristics* table.

The maximum safety temperature (T_S) for the device is the +150°C maximum junction temperature specified in the *Absolute Maximum Ratings*. See the *Thermal Considerations* section for details on determining the junction temperature.

Figure 3 and *Figure 4* show the thermal derating curves for safety limiting the power and the current for the device in the 8-lead Narrow SOIC (21-0041) package when mounted on the JEDEC 2S2P test card. Ensure that the junction temperature does not exceed +150°C.

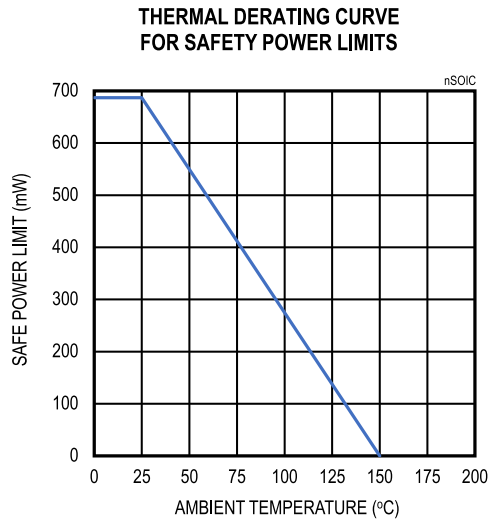


Figure 3. Thermal Derating Curve for 8-Lead Narrow SOIC Package

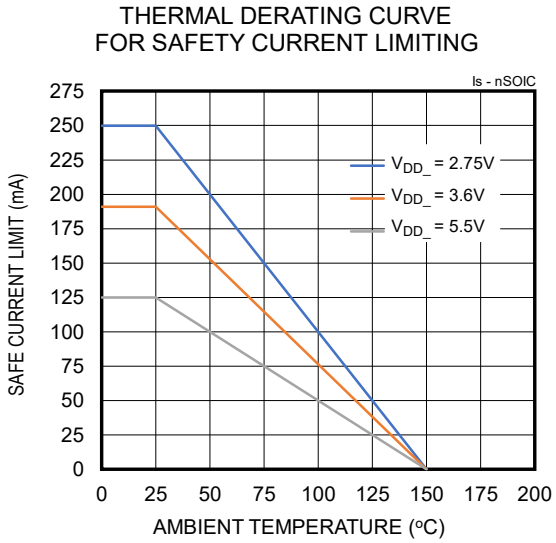


Figure 4. Thermal Derating Curve for Safety Current Limiting for 8-Lead Narrow SOIC Package

Figure 5 and *Figure 6* show the thermal derating curves for safety limiting the power and the current of the device in the 8-lead Wide SOIC (21-100415) package when mounted on the JEDEC 2S2P test card. Ensure that the junction temperature does not exceed 150°C.

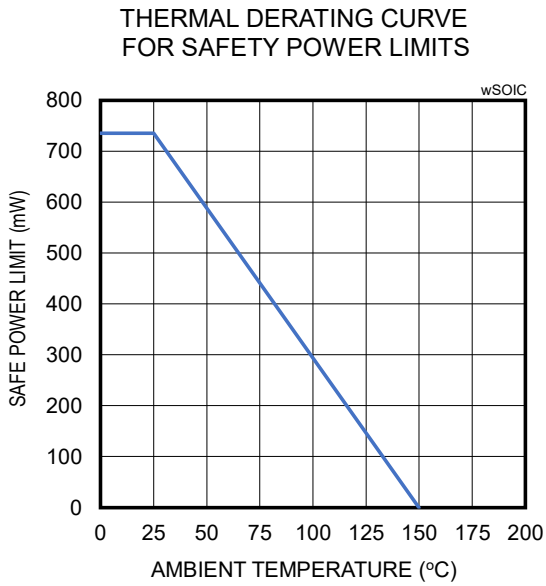


Figure 5. Thermal Derating Curve for 8-Lead Wide SOIC Package

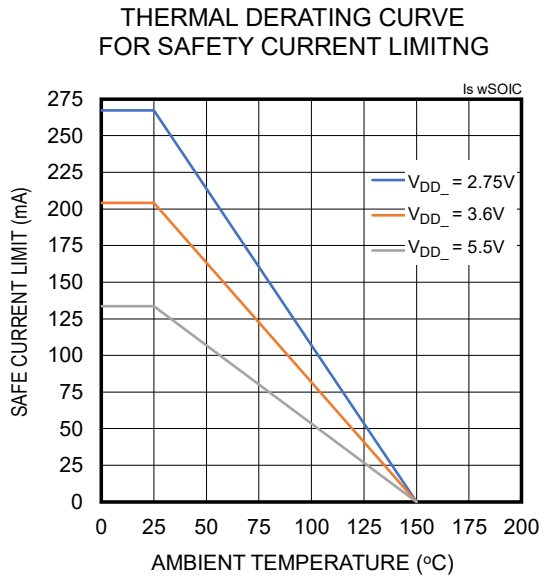


Figure 6. Thermal Derating Curve for Safety Current Limiting for 8-Lead Wide SOIC Package

Isolation Characteristics

8-Lead Narrow SOIC (21-0041) Isolation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
CLASSIFICATIONS				
Overvoltage Category per IEC60664-1		For rated mains voltage ≤ 150V_{RMS}	I to IV	—
		For rated mains voltage ≤ 300V_{RMS}	I to III	—
Climatic Classification			40/125/21	—
Pollution Degree		Per DIN VDE V 0110 (refer to *Table 1* of the DIN VDE standard)	2	—
VOLTAGE				
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (*Note 1*)	445	V_{RMS}
Maximum Repetitive Isolation Voltage	V_{IORM}	(*Note 1*)	630	V_{PEAK}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s (*Note 1*)	4242	V_{PEAK}
Maximum Withstanding Isolation Voltage	V_{ISO}	f_{TEST} = 60Hz, duration = 60s (*Note 1*, *Note 2*)	3000	V_{RMS}
Maximum Surge Isolation Voltage, Reinforced	V_{IOSM}	Test method per IEC 60065, V_{TEST} = 1.6 x V_{IOSM} = 10000V_{PEAK} (*Note 1*, *Note 4*)	6250	V_{PEAK}
Maximum Impulse Voltage	V_{IMP}	Tested in air, 1.2µs/50µs waveform per IEC 62368-1	6000	V_{PEAK}
Input to Output Test Voltage	V_{PR}		1182	V_{PEAK}
Apparent Charge	q_{pd}	Method B1, V_{PR} =1.875 x V_{IORM}, t = 1s	5	pC
PACKAGE CHARACTERISTICS				
External Clearance	CLR	Measured from input terminals to output terminals, shortest distance through air	4	mm
External Creepage	CPG	Measured from input terminals to output terminals, shortest distance along body	4	mm
Internal Clearance	DTI	Distance through insulation	21	µm
Comparative Tracking Index	CTI		> 600	V
Material Group		Material group (IEC 60112)	I	—
Resistance (Input to Output)	R_{IO}	V_{IO} = 500V, T_A = +25°C (*Note 3*)	10^{12}	Ω
		V_{IO} = 500V, +100°C ≤ T_A ≤ +125°C (*Note 3*)	10^{11}	Ω
	R_{IO_S}	V_{IO} = 500V, T_S = +150°C (*Note 3*)	10^{9}	Ω
Capacitance (Input to Output)	C_{IO}	f_{TEST} = 1MHz (*Note 3*)	1.5	pF
SAFETY LIMITING VALUES				
Maximum Ambient Safety Temperature	T_S		150	°C
Maximum Input Power Dissipation	P_{SI}	θ_{JA} = 182°C/W, T_J = +150°C, T_A = +25°C	687	mW
Maximum Output Power	P_{SO}	T_J = +150°C, T_A = +25°C		mW
Maximum Output Current	I_{SO}	θ_{JA} = 182°C/W, T_J = +150°C, T_A = +25°C, V_{DD} = 5.5V	124	mA
		θ_{JA} = 182°C/W, T_J = +150°C, T_A = +25°C, V_{DD} = 3.6V	190	mA
		θ_{JA} = 182°C/W, T_J = +150°C, T_A = +25°C, V_{DD} = 2.75V	249	mA

Note 1: V_{ISO}, V_{IOTM}, V_{IOWM}, V_{IORM} and V_{IOSM} are defined by the IEC 60747-17 standard.

Note 2: Product is qualified at V_{ISO} for 60s and 100% production tested at 120% of V_{ISO} for 1s.

Note 3: Device is measured as a 2-terminal device with Pin 1 through Pin 4 connected and Pin 5 through Pin 8 connected.

Note 4: Devices are immersed in oil during surge characterization.

8-Lead Wide SOIC (21-100415) Isolation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
CLASSIFICATIONS				
Overvoltage Category per IEC60664-1		For rated mains voltage ≤ 150 V_{RMS}	I to IV	—
		For rated mains voltage ≤ 300 V_{RMS}	I to IV	—
		For rated mains voltage ≤ 600 V_{RMS}	I to IV	—
Climatic Classification			40/125/21	—
Pollution Degree		Per DIN VDE V 0110 (refer to *Table 1* of the DIN VDE standard)	2	—
VOLTAGE				
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (*Note 1*)	848	V_{RMS}
Maximum Repetitive Isolation Voltage	V_{IORM}	(*Note 1*)	1200	V_{PEAK}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s (*Note 1*)	7070	V_{PEAK}
Maximum Withstanding Isolation Voltage	V_{ISO}	f_{TEST} = 60Hz, duration = 60s (*Note 1*, *Note 2*)	5000	V_{RMS}
Maximum Surge Isolation Voltage, Reinforced	V_{IOSM}	Test method per IEC 60065, V_{TEST} = 1.6 x V_{IOSM} = 10000V_{PEAK} (*Note 1*, *Note 4*)	6250	V_{PEAK}
Maximum Impulse Voltage	V_{IMP}	Tested in air, 1.2µs/50µs waveform per IEC 62368-1	8000	V_{PEAK}
Input to Output Test Voltage	V_{PR}		2250	V_{PEAK}
Apparent Charge	q_{pd}	Method B1, V_{PR} =1.875 x V_{IORM}, t = 1s	5	pC
PACKAGE CHARACTERISTICS				
External Clearance	CLR	Measured from input terminals to output terminals, shortest distance through air	8	mm
External Creepage	CPG	Measured from input terminals to output terminals, shortest distance along body	8	mm
Internal Clearance	DTI	Distance through insulation	21	µm
Comparative Tracking Index	CTI		> 600	V
Material Group		Material group (IEC 60112)	I	—
Resistance (Input to Output)	R_{IO}	V_{IO} = 500V, T_A = +25°C (*Note 3*)	10^{12}	Ω
		V_{IO} = 500V, +100°C ≤ T_A ≤ +125°C *Note 3*)	10^{11}	Ω
	R_{IO_S}	V_{IO} = 500V, T_S = +150°C (*Note 3*)	10^{9}	Ω
Capacitance (Input to Output)	C_{IO}	f_{TEST} = 1MHz (*Note 3*)	1.5	pF
SAFETY LIMITING VALUES				
Maximum Ambient Safety Temperature	T_S		150	°C
Maximum Input Power Dissipation	P_{SI}	θ_{JA} = 170°C/W, T_J = +150°C, T_A = +25°C	735	mW
Maximum Output Current	I_{SO}	θ_{JA} = 170°C/W, T_J = +150°C, T_A = +25°C, V_{DD} = 5.5V	133	mA
		θ_{JA} = 170°C/W, T_J = +150°C, T_A = +25°C, V_{DD} = 3.6V	204	mA
		θ_{JA} = 170°C/W, T_J = +150°C, T_A = +25°C, V_{DD} = 2.75V	267	mA

Note 1: V_{ISO}, V_{IOTM}, V_{IOWM}, V_{IORM} and V_{IOSM} are defined by the IEC 60747-17 standard.

Note 2: Product is qualified at V_{ISO} for 60s and 100% production tested at 120% of V_{ISO} for 1s.

Note 3: Device is measured as a 2-terminal device with Pin 1 through Pin 4 connected and Pin 5 through Pin 8 connected.

Note 4: Devices are immersed in oil during surge characterization.

Regulatory Information

The ADuM1254 has been approved by the organizations listed below. Certifications are available at *Safety and Regulatory Certifications for Digital Isolation*.

8-Lead Narrow SOIC (21-0041) Package Certifications

REGULATORY AGENCY	STANDARD CERTIFICATION/APPROVAL	FILE
UL	UL 1577 component recognition program (*Note 1*): Single/basic 3000V_{RMS} isolation voltage.	(Pending)
CSA	CSA No 14-18 (*Note 2* and *Note 3*): CSA 62368-1:19, IEC 62368-1:2018 Ed. 3 and EN62368-1:2020+A11:2020: Basic insulation at 400V_{RMS}. CSA 61010-1-12+A1 and IEC 61010-1 3rd Ed.: Basic insulation at 300V_{RMS} from mains, 400V_{RMS} from secondary circuit.	(Pending)
VDE	IEC 60747-17 (*Note 4*): Reinforced insulation, maximum transient isolation voltage 4242V_{PK}, maximum repetitive peak isolation voltage 630V_{PK}.	(Pending)
CQC	GB 4943.1-2022: Basic insulation at 400V_{RMS} (565V_{PEAK}) maximum working voltage, tropical climate, altitude < 5000m	(Pending)
TUV Sud	IEC 62368-1:2018 Ed. 3 and EN62368-1:2020+A11:2020: Basic insulation at 400V_{RMS}	(Pending)

Note 1: In accordance with UL 1577, each ADuM1254ASA+ is proof tested by applying an insulation test voltage ≥ 3600V_{RMS} for 1 second (current leakage detection limit = 5µA).

Note 2: Working voltages are quoted for material group III case material in pollution degree 2. ADuM1254ASA+ case material has been evaluated by CSA as material group I.

Note 3: The creepage and clearance distances have been evaluated for altitudes < 2000m, material group III, in pollution degree 2 and overvoltage category II, except where specified above.

Note 4: In accordance with IEC 60747-17, each ADuM1254 is proof tested by applying an insulation test voltage ≥ 1182V peak for 1s (partial discharge detection limit = 5 pC). This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

8-Lead Wide SOIC (21-00415) Package Certifications

REGULATORY AGENCY	STANDARD CERTIFICATION/APPROVAL	FILE
UL	UL 1577 component recognition program (*Note 1*): Single/basic 5000V_{RMS} isolation voltage.	(Pending)
CSA	CSA No 14-18 (*Note 2* and *Note 3*): CSA 62368-1:19, IEC 62368-1:2018 Ed. 3 and EN62368-1:2020+A11:2020: Basic insulation at 800V_{RMS}. CSA 61010-1-12+A1 and IEC 61010-1 3rd Ed.: Basic insulation at 600V_{RMS} from mains, 800V_{RMS} from secondary circuit	(Pending)

VDE	IEC 60747-17 (*Note 4*): Reinforced insulation, maximum transient isolation voltage 7070V_{PK}, maximum repetitive peak isolation voltage 1200V_{PK}.	(Pending)
CQC	GB 4943.1-2022: Basic insulation at 800V_{RMS} (1131V_{PEAK}) maximum working voltage, tropical climate, altitude < 5000m	(Pending)
TUV Sud	IEC 62368-1:2018 Ed. 3 and EN62368-1:2020+A11:2020: Basic insulation at 800V_{RMS}	(Pending)

Note 1: In accordance with UL 1577, each ADuM1254AWA+ is proof tested by applying an insulation test voltage ≥ 6000V_{RMS} for 1 second (current leakage detection limit = 5µA).

Note 2: Working voltages are quoted for material group III case material in pollution degree 2. ADuM1254AWA+ case material has been evaluated by CSA as material group I.

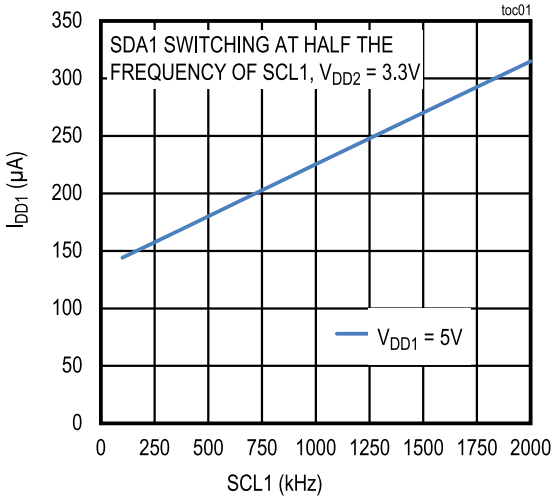
Note 3: The creepage and clearance distances have been evaluated for altitudes < 2000m, material group III, in pollution degree 2 and overvoltage category II, except where specified above.

Note 4: In accordance with IEC 60747-17, each ADuM1254 is proof tested by applying an insulation test voltage ≥ 2250V peak for 1s (partial discharge detection limit = 5 pC). This coupler is suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

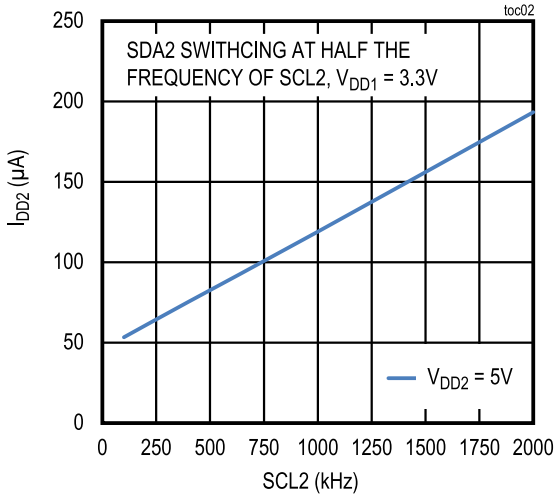
Typical Operating Characteristics

(Typical values are at V_{DD1} = V_{DD2} = 3.3V, GND1 = GND2, T_A = +25°C, unless otherwise noted. C_L = 20pF, R_{PULLUP} = 1kΩ and 1nF, 100nF, and 1µF decoupling capacitors are on V_{DD1} and V_{DD2}. All tests were performed using the ADuM1252SEVKIT#.)

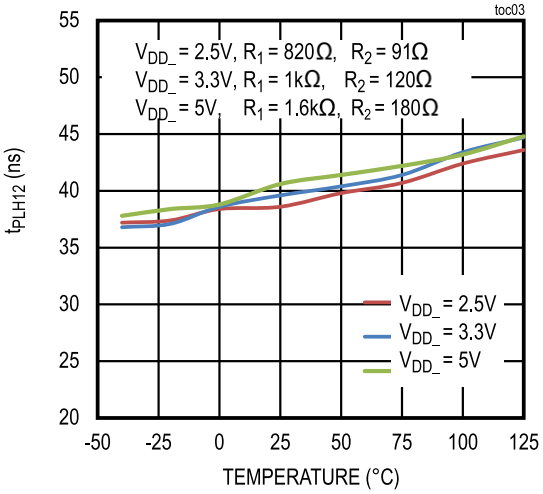
SIDE 1 SUPPLY CURRENT vs. DATA RATE



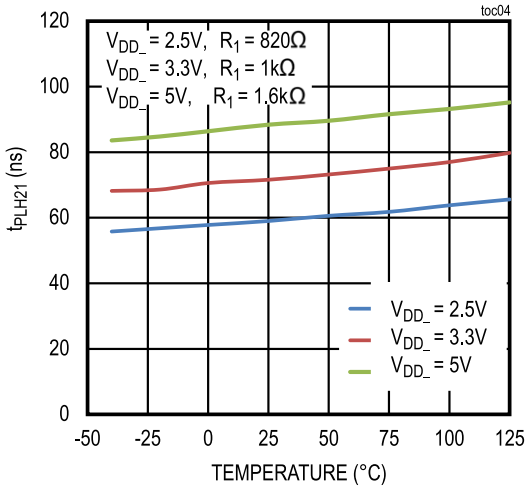
SIDE 2 SUPPLY CURRENT vs. DATA RATE



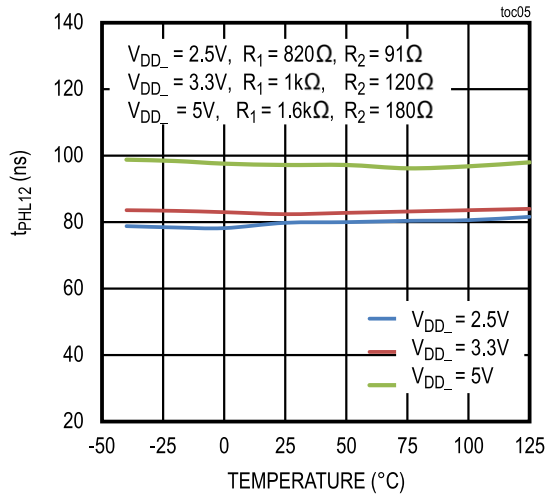
PROPAGATION DELAY t_{PLH12} vs. TEMPERATURE



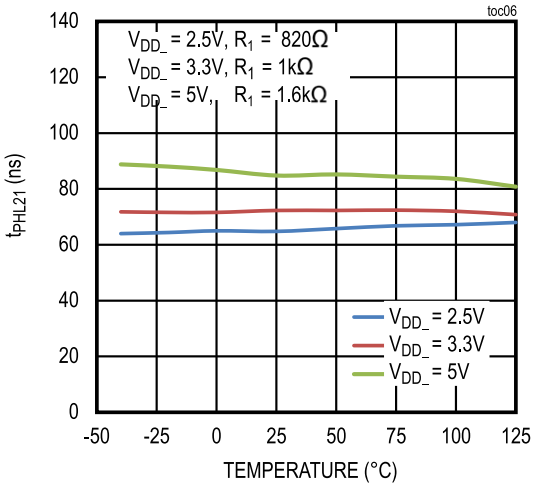
PROPAGATION DELAY t_{PLH21} vs. TEMPERATURE



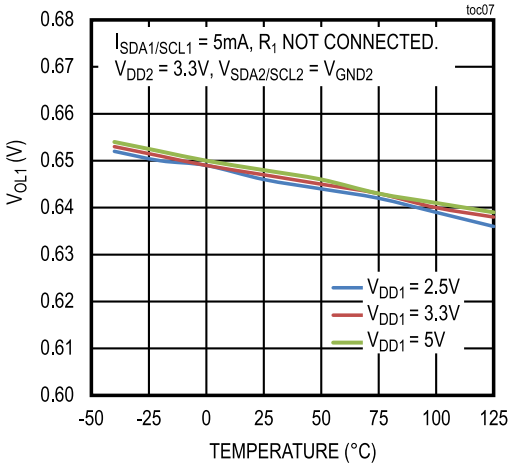
PROPAGATION DELAY t_{PHL12} vs. TEMPERATURE



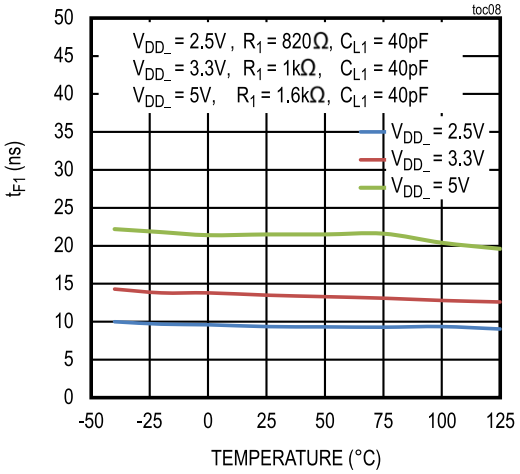
PROPAGATION DELAY t_{PHL21} vs. TEMPERATURE



SIDE 1 OUTPUT LOW VOLTAGE vs. TEMPERATURE

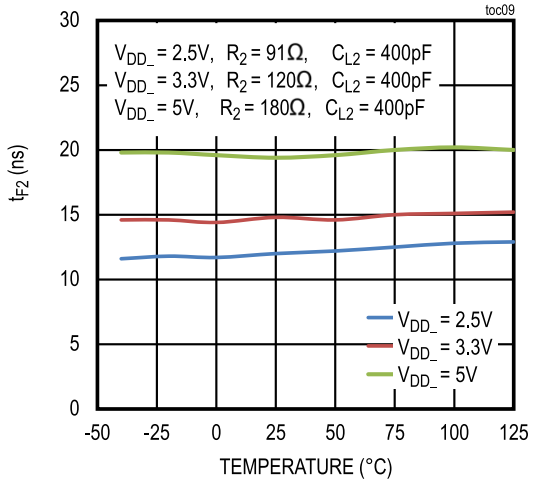


SIDE 1 OUTPUT FALL TIME vs. TEMPERATURE



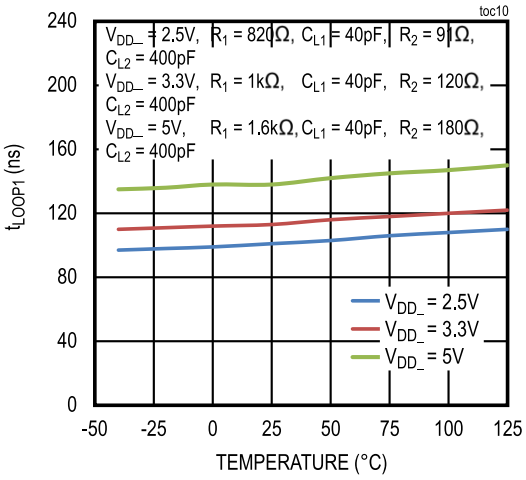
t_{F1} MEASURED FROM 0.7V_{DD1} TO 0.3V_{DD1}

SIDE 2 OUTPUT FALL TIME vs. TEMPERATURE

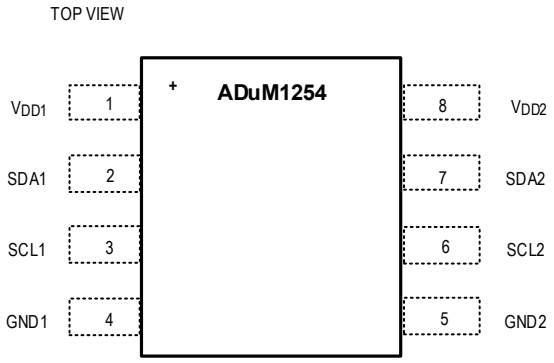


t_{F2} MEASURED FROM 0.7V_{DD2} TO 0.3V_{DD2}

t_{LOOP1} vs. TEMPERATURE



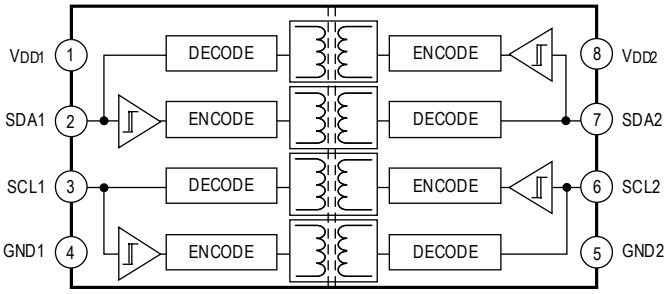
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	V_{DD1}	Supply Voltage Side 1. Bypass V_{DD1} with a 1nF and a 0.1µF ceramic capacitor as close as possible to the pin.
2	SDA1	Serial Data Input/Output on Side 1. SDA1 is translated to/from SDA2 and is an open-drain output.
3	SCL1	Serial Clock Input/Output on Side 1. SCL1 is translated to/from SCL2 and is an open-drain output.
4	GND1	Ground Reference for Side 1
5	GND2	Ground Reference for Side 2
6	SCL2	Serial Clock Input/Output on Side 2. SCL2 is translated to/from SCL1 and is an open-drain output.
7	SDA2	Serial Data Input/Output on Side 2. SDA2 is translated to/from SDA1 and is an open-drain output.
8	V_{DD2}	Supply Voltage Side 2. Bypass V_{DD2} with a 1nF and a 0.1µF ceramic capacitor as close as possible to the pin.

Functional Diagram



Detailed Description

The ADuM1254 is a two-channel I2C isolator utilizing Analog Devices, Inc. proprietary process technology. The device transfers digital signals between circuits with different power domains at ambient temperatures up to +125°C.

The device offers two bidirectional open-drain channels for applications, such as I2C, that require data to be transmitted in both directions on the same line. The bidirectional clock channel allows for applications with multiple I2C controllers located on both sides of the isolation barrier and/or clock stretching by a I2C target device regardless of its location relative to the isolation barrier and controller.

The device features independent 2.25V to 5.5V supplies on each side of the isolator. The device operates with SCL frequencies up to 2MHz. The wide temperature range and high isolation voltage make the device ideal for use in harsh industrial environments.

Digital Isolation

The ADuM1254 provides reinforced galvanic isolation for digital signals that are transmitted between two ground domains.

In the 8-pin narrow SOIC package (21-0041), the ADuM1254 withstands voltage differences of up to $3kV_{RMS}$ for up to 60 seconds and up to $630V_{PEAK}$ of continuous isolation.

In the 8-pin wide SOIC package (21-100415), the ADuM1254 withstands voltage differences of up to $5kV_{RMS}$ for up to 60 seconds and up to $1200V_{PEAK}$ of continuous isolation.

Bidirectional Channels

The ADuM1254 device features two bidirectional channels that have open-drain outputs.

The bidirectional channels do not require a direction control input. A logic-low on one side causes the corresponding pin on the other side to be pulled low while avoiding data latching within the device due to the coordination of the side 1 output logic-low voltage (V_{OL1}) and input logic-low threshold (V_{IL1}). The side 1 outputs utilize special buffers that regulate V_{OL1} to approximately 0.64V while keeping V_{IL1} at least 50mV lower than V_{OL1}. This difference prevents an output logic-low on side 1 from being accepted as an input low and subsequently transmitted to side 2, thus, preventing a latching action. SDA2 and SCL2 are conventional outputs that do not regulate the logic-low output voltage.

Due to their special nature, the side 1 SDA/SCL pins of different ADuM1254 devices cannot be connected together. This restriction also includes pins on other devices which employ similar buffers or rise-time accelerators. The side 2 pins do not have this restriction. Therefore, the side 2 pins of the ADuM1254 can be connected to each other or to any other bidirectional buffer or level translator's pin, including the side 1 pins of the ADuM1254.

The ADuM1254's outputs are all open-drain and require pull-up resistors to their respective supplies to generate the logic-high output voltage. The output low voltages are guaranteed for sink currents of up to 50mA for side 2 and 5mA for side 1 (see the *Electrical Characteristics* table).

The ADuM1254's bidirectional SCL channel supports I2C clock stretching.

Startup and Undervoltage Lockout

The V_{DD1} and V_{DD2} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage

condition is detected on either supply, all outputs go to their default states regardless of the state of the inputs as seen in *Table 1*.

Table 1. Output Behavior During Undervoltage Condition

V_{DD1}	V_{DD2}	INPUT	V_{OUT1}	V_{OUT2}
Powered	Powered	High	High-Z	High-Z
Powered	Powered	Low	Low	Low
Undervoltage	Powered	Don't care	High-Z	High-Z
Powered	Undervoltage	Don't care	High-Z	High-Z

Level Shifting

The wide supply voltage range of both V_{DD1} and V_{DD2} allows the ADuM1254 to be used for level translation in addition to isolation. V_{DD1} and V_{DD2} can be independently set to any voltage from 2.25V to 5.5V. The supply voltage sets the logic level on the corresponding side of the isolator.

Hot Swap

The ADuM1254 includes special precharge circuitry on SDA2/SCL2 to prevent loading on the I²C bus lines while the supply is either unpowered or in the process of being powered on. When the supply is below the UVLO threshold, the ADuM1254 bus lines do not load the bus to avoid disrupting or corrupting an active I²C bus. If the isolator is plugged into a live backplane using a staggered connector, where the supply and ground make connection first followed by the bus lines, the SDA2 and SCL2 lines are precharged to $V_{DD2}/3$ to minimize the current required to charge the parasitic capacitance of the device. Once the device is fully powered on, the device I/O pins become active. However, the connection between side 1 and side 2 does not occur until after the side 2 bus either detects an I²C stop condition or the bus has been idle for 125µs. See *Figure 7*.

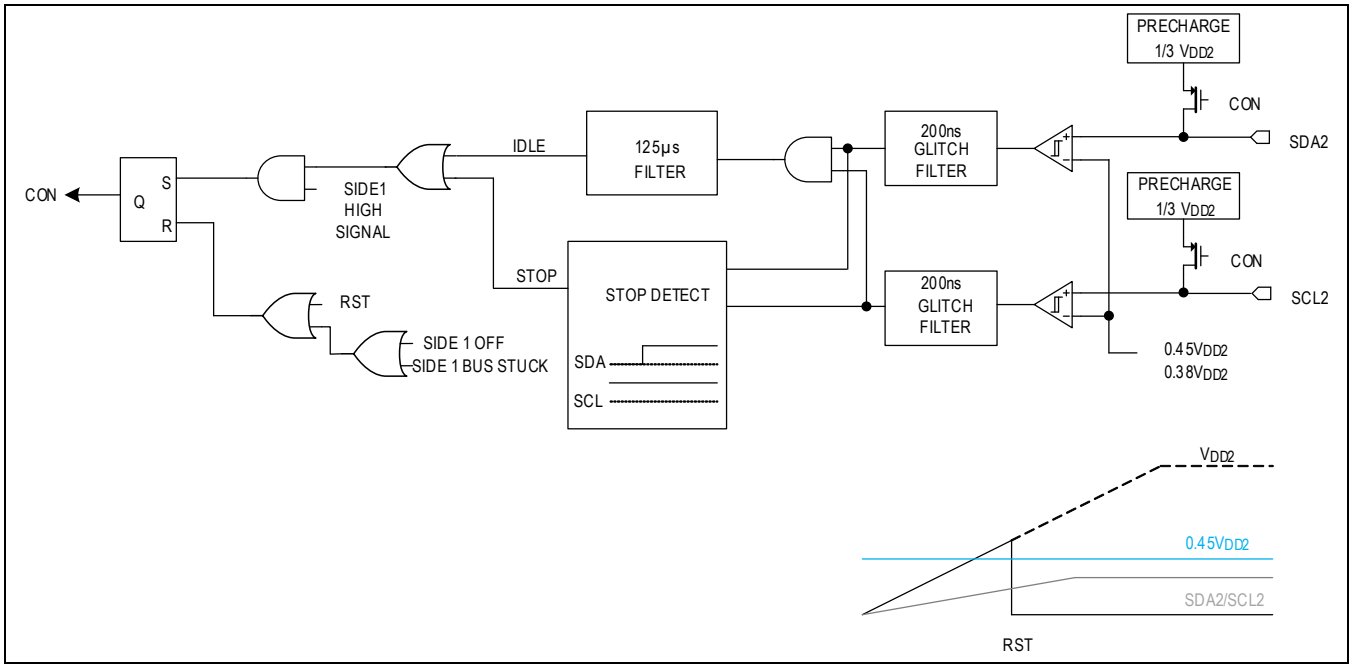


Figure 7. Bus Connection Logic

Bus Connection

The ADuM1254 connects the side 1 bus to the side 2 bus when both busses are idle or when side 1 is high and an I^2C stop condition has been detected on side 2. If a stuck bus condition is detected on side 1, then the ADuM1254 disconnects the two busses to allow the external system to attempt a recovery.

Applications Information

Power-Supply Sequencing

The ADuM1254 does not require special power-supply sequencing. The logic levels are set independently on either side by V_{DD1} and V_{DD2}. Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors especially if large common-mode transients are expected in the application, bypass V_{DD1} and V_{DD2} with 100nF and 1nF low-ESR ceramic capacitors to GND1 and GND2, respectively. Place the bypass capacitors as close to the power-supply input pins as possible.

Thermal Considerations

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Pay careful attention to the PCB thermal design.

Thermal parameter values are specified in the *Package Information* section. θ_{JA} and θ_{JB} are mainly used to compare the thermal performance of the package of the device with other semiconductor packages when all test conditions listed are similar. Ψ_{JB} or Ψ_{JT} can be used to estimate the junction temperature when an accurate thermal measurement of the board temperature is available. The temperature measurement must be near the device under test (DUT) or directly on the package top surface, operating in the system environment.

θ_{JA} can be used for a first-order approximation to calculate the junction temperature in the system environment. The power dissipation (P_D), junction-to-ambient thermal impedance (θ_{JA}), and ambient temperature (T_A) determine the junction temperature (T_J) according to the expression:

$$T_J = T_A + (P_D \times \theta_{JA})$$

A more accurate estimate of the junction temperature can be found using Ψ_{JT}. Measure the device package temperature ($T_{PACKAGE}$) in the center of the package using an IR camera or thermocouple and then use the following expression:

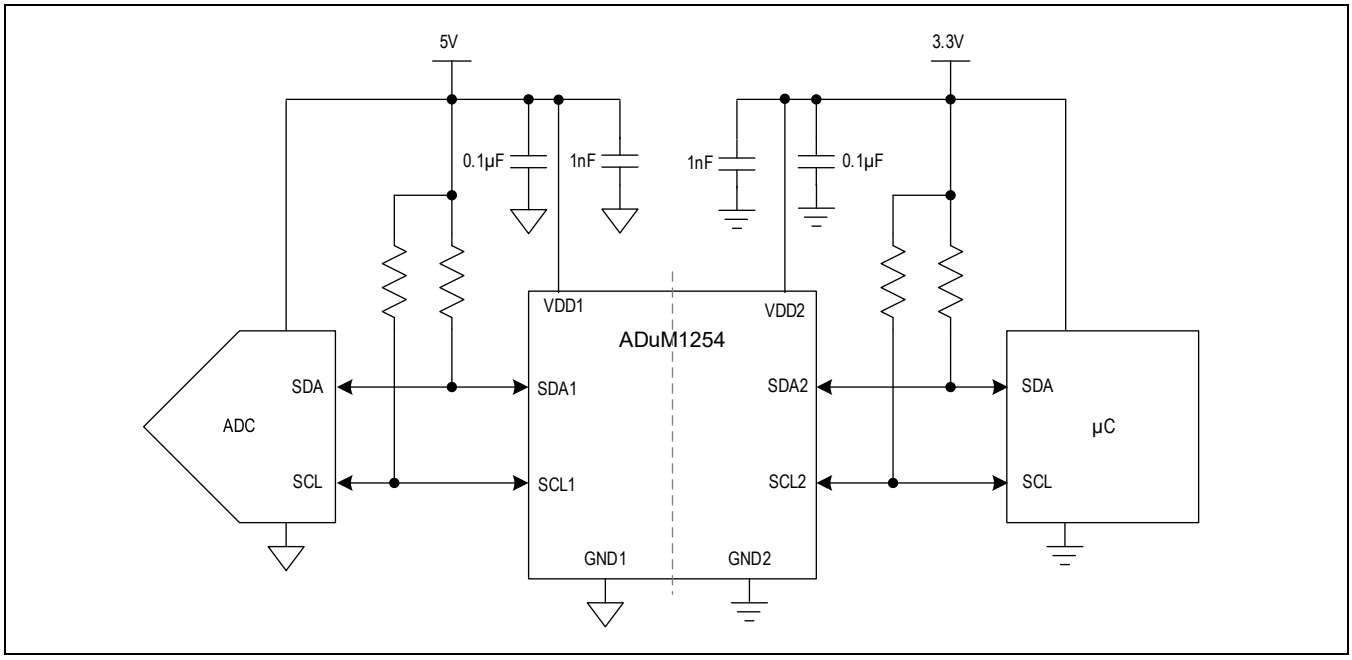
$$T_J = T_{PACKAGE} + \Psi_{JT} \times P_D$$

Layout Considerations

The PCB designer should follow some critical recommendations to get the best performance from the design.

- Keep the input/output traces as short as possible. To keep signal paths low inductance, avoid using vias.
- Have a solid ground plane underneath the high-speed signal layer.
- Keep the area underneath the ADuM1254 free from ground and signal planes. Any galvanic or metallic connection between side 1 and side 2 defeats the isolation.

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
ADuM1254ASA+	-40°C to +125°C	8 Narrow SOIC
ADuM1254ASA+T	-40°C to +125°C	8 Narrow SOIC
ADuM1254AWA+	-40°C to +125°C	8 Wide SOIC
ADuM1254AWA+T	-40°C to +125°C	8 Wide SOIC

+ Denotes a lead (Pb)-free/RoHS-compliant package.
T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/23	Initial release	—
1	5/24	Added of Wide SOIC package, changed Narrow SOIC safety limit current VDD from 5.6V to 5.5V, moved ESD characteristics to Electrical Characteristics table, clarified which parameters are guaranteed by design, removed statement that asterisk (*) marking branded on the component designates DIN IEC60747-17 approval, and added statement on safe electrical isolation to Package Certifications table Note 4	1–13, 17, 20