DATA SHEET
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3.75 kV_{RMS}, 4.5-A/9-A Isolated Single Channel Gate Driver with Integrated Negative Bias Control

NCV51752

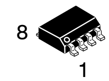
The NCV51752 is a family of isolated single−channel gate driver with 4.5−A/9−A source and sink peak current respectively. They are designed for fast switching to drive power MOSFETs and SiC MOSFET power switches. The NCV51752 offers short and matched propagation delays. For improved reliability, dV/dt immunity and even faster turn−off, the NCV51752 can utilize to generate a negative bias rail. The NCV51752 is available in a 4 mm SOIC−8 package and can support isolation voltage up to 3.75 kV_{RMS}. The NCV51752 offers other important protection function such as independent under−voltage lockout for both−side driver.

Features

- Feature Options
  - V_{CC} UVLO Referenced to GND2
  - Built−in Negative Bias between GND2 and V_{EE} Pins Selectable Negative Bias Levels via Trim
- 3−V to 20−V Input Supply Voltage
- Output Supply Voltage from 6.5 V to 30 V with 6−V and 8−V for MOSFET, 12−V and 17−V for SiC, Threshold
- 4.5−A Peak Source, 9−A Peak Sink Output Current Capability
- Minimum CMTI of 200 V/ns dV/dt
- Negative 5−V Handling Capability on Input Pins
- Propagation Delay Typical 36 ns with
  - 5 ns Max Delay Matching
- AEC−Q100 Qualified for Automotive Application Requirements
- Isolation & Safety
  - 3.75 kV_{RMS} Isolation for 1 Minute (per UL1577 Requirements) (Planned)
  - CQC Certification per GB4943.1−2011 (Planned)
  - SGS FIMO Certification per IEC 62386−1 (Planned)

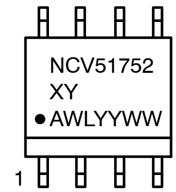
Typical Applications

- On−board Chargers
- xEV DC−DC Converters
- Traction Inverters
- Charging Stations



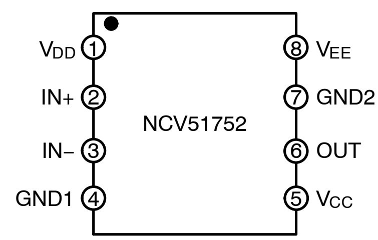
SOIC−8 NB
CASE 751−07

MARKING DIAGRAM



NCV51752	=	Specific Device Code
X	=	A or B or C or D for UVLO Option
Y	=	A or B or C or D for Neg. Bias Level Option
A	=	Assembly Location
WL	=	Wafer Lot
YY	=	Year
WW	=	Work Week

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 23 of this data sheet.

TYPICAL APPLICATION CIRCUIT

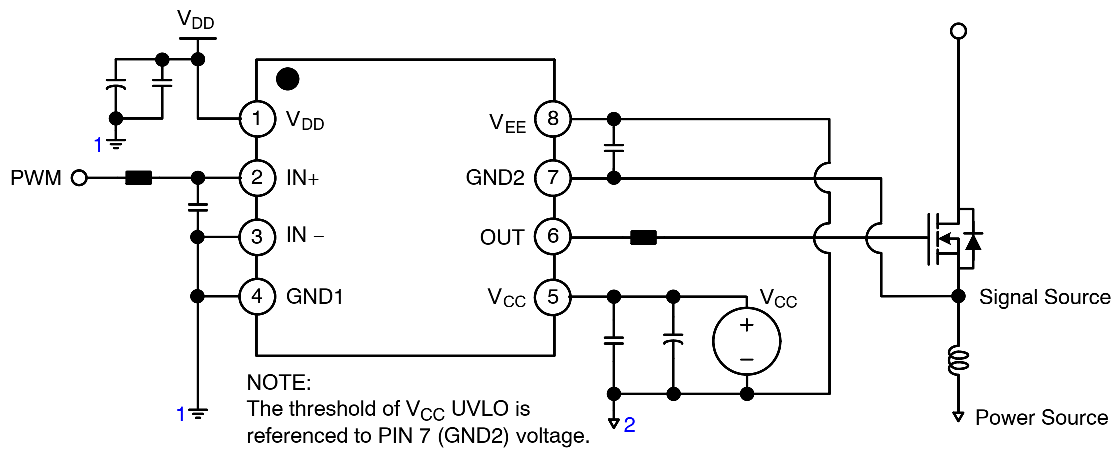


Figure 1. Typical Application Schematic

FUNCTIONAL BLOCK DIAGRAM

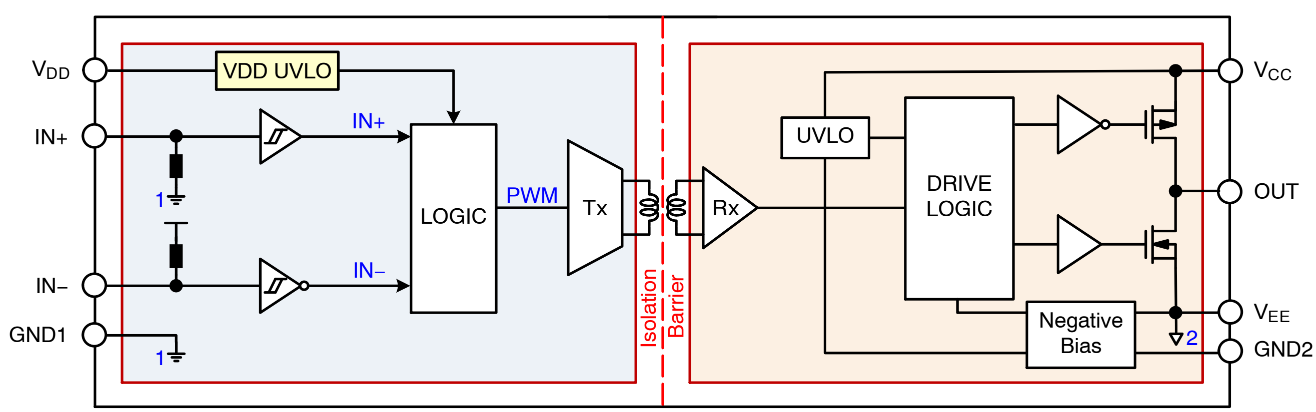


Figure 2. Simplified Block Diagram

PIN CONNECTIONS

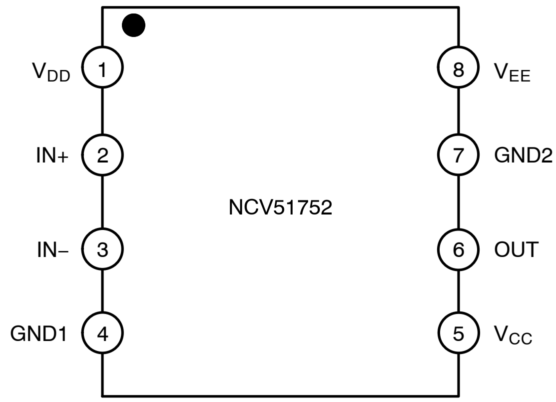


Figure 3. Pin Connections – SOIC−8 NB (Top View)

PIN DESCRIPTION

Pin Name	Pin No.	I/O	Description
V_{DD}	1	Power	Input−side Supply Voltage. It is recommended to place a bypass capacitor from V_{DD} to GND1.
IN+	2	Input	Non−inverting Logic Input with internal pull−down resistor to GND1.
IN−	3	Input	Inverting Logic Input with internal pull−up resistor to V_{DD}.
GND1	4	Power	Ground Input−side. (All signals on input−side are referenced to this ground)
V_{CC}	5	Power	Positive Output Supply Rail.
OUT	6	Output	Gate Drive Output.
GND2	7	Power	Gate−drive common pin. Connect this pin to the MOSFET source. V_{CC} UVLO threshold referenced to GND2.
V_{EE}	8	Power	Negative output supply rail.

INSULATION RATINGS

Symbol	Parameter		Value	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage	<150 V_{RMS}	I–IV	
		<300 V_{RMS}	I–IV	
		<450 V_{RMS}	I–IV	
		<600 V_{RMS}	I–IV	
		<1000 V_{RMS}	I–III	
CTI	Comparative Tracking Index (DIN IEC 112/VDE 0303 Part 1)		600	
	Climatic Classification		40/125/21	
	Pollution Degree (DIN VDE 0110/1.89)		2	
V_{PR}	Input−to−Output Test Voltage, Method b, V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 s, Partial Discharge < 5 pC		2250	V_{PK}
V_{IORM}	Maximum Repetitive Peak Isolation Voltage		1200	V_{PK}
V_{IOWM}	Maximum Working Voltage		870	V_{RMS}
V_{IOTM}	Maximum Transient Isolation Voltage		6300	V_{PK}
E_{CR}	External Creepage		4.0	mm
E_{CL}	External Clearance		4.0	mm
DTI	Insulation Thickness		17.3	μm
R_{IO}	Insulation Resistance at T_S, V_{IO} = 500 V		10^9	Ω

SAFETY LIMITING VALUE

Symbol	Parameter	Test Condition	Side	Value	Unit
P_S	Safety Supply Power	$R_{\theta JA}$ = 100°C/W, T_A = 25°C, T_J = 150°C	INPUT	0.21	W
			OUTPUT	1.04	W
			TOTAL	1.25	W
T_S	Safety Temperature			150	°C

MAXIMUM RATINGS

Symbol		Parameter	Min	Max	Unit
V_{DD} to GND1		Power Supply Voltage – Input Side (Note 2)	−0.3	25	V
V_{CC} – VEE		Power Supply Voltage – Driver cside (Note 3)	−0.3	33	V
VEE – GND2		VEE Bipolar Supply Voltage (Note 3)	−18	0.3	V
OUT to VEE		Driver Output Voltage (Note 3)	V_{EE} − 0.3	V_{CC} + 0.3	V
OUT to VEE, Transient for 200 ns (Note 4)			V_{EE} − 2	V_{CC} + 0.3	V
IN+, and IN−		Input Signal Voltages (Note 2)	−5	V_{DD} + 0.3	V
T_J		Junction Temperature	−40	+150	°C
T_S		Storage Temperature	−65	+150	°C
Electrostatic Discharge Capability	HBM (Note 5)	Human Body Model	–	2	kV
	CDM (Note 5)	Charged Device Model	–	1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. All voltage values are given with respect to GND1 pin.
3. All voltage values are given with respect to VEE pin.
4. This parameter verified by design and bench test, not tested in production.
5. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Charged Device Model tested per AEC−Q100−011 (EIA/JESD22−C101)
   Latch up Current Maximum Rating: ≤100 mA per JEDEC standard: JESD78F.

THERMAL CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit
θ_{JA}	Thermal Resistance of Junction−Air (Note 6)	Type−A (Note 7)	100	°C/W
		Type−B (Note 8)	120	
Ψ_{JT}	Thermal Characterization Parameter Junction−Case Top	Type−A (Note 7)	8	
		Type−B (Note 8)	8	
P_D	Power Dissipation (Note 6)	Type−A (Note 7)	1.25	W
		Type−B (Note 8)	1.04	

6. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
7. As specified for a reference layout shown in Figure 4. The DUT is mounted on a 60 x 40 x 1.6 mm FR4 substrate with an additional heat spreading copper of 240 mm^2/300 mm^2 (Primary/Secondary). The copper thickness is 1 oz and test conditions is under natural convection or zero air flow.

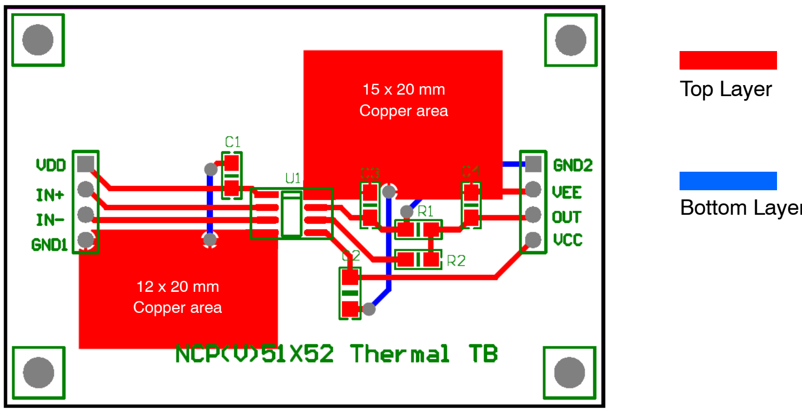


Figure 4. Reference Layout for the Type−A

8. As specified for a reference layout shown in Figure 5. The DUT is mounted on a 60 x 40 x 1.6 mm FR4 substrate with an additional heat spreading copper of 240 mm^2/300 mm^2 (Primary/Secondary). The copper thickness is 1oz and test conditions is under natural convection or zero air flow.

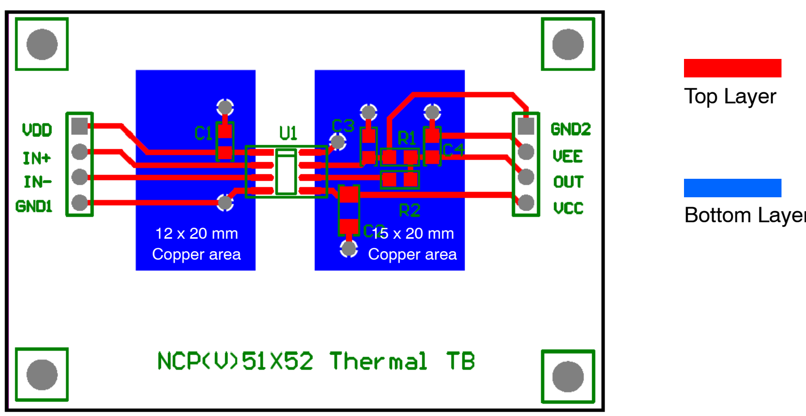


Figure 5. Reference Layout for the Type−B

RECOMMENDED OPERATING CONDITIONS

Symbol	Rating		Min	Max	Unit
V_{DD}	Power Supply Voltage – Input Side		3.0	20	V
V_{CC}	Power Supply Voltage – Driver Side (Note 9)	6−V UVLO Version	6.5	30	V
		8−V UVLO Version	9.5	30	V
		12−V UVLO Version	13.5	30	V
		17−V UVLO Version	18.5	30	V
V_{IN}	Logic Input Voltage at Pins IN+, and IN−		0	V_{DD}	V
T_A	Ambient Temperature		−40	+125	°C
T_J	Junction Temperature		−40	+125	°C
CMTI	Common Mode Transient Immunity		200	–	kV/μs

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

9. All V_{CC} UVLO threshold voltages are given with respect to GND2 pin.

ISOLATION CHARACTERISTICS

Symbol	Parameter	Condition	Value	Unit
$V_{ISO,INPUT\ TO\ OUTPUT}$	Input to Output Isolation Voltage	T_A = 25°C, Relative Humidity < 50%, t = 1.0 minute, $I_{I-O} <$ 30 μA, 50 Hz (Note 10,11,12)	3750	V_{RMS}
R_{ISO}	Isolation Resistance	V_{I_O} = 500 V (Note 10)	10^{11}	Ω

10. Device is considered a two−terminal device: pins 1 to 4 are shorted together and pins 5 to 8 are shorted together.
11. 3,750 V_{RMS} for 1−minute duration is equivalent to 4,500 V_{RMS} for 1−second duration for input to output isolation test, and Impulse Test > 10 ms; sample tested for between channel isolation test.
12. The input−output isolation voltage is a dielectric voltage rating per UL1577. It should not be regarded as an input−output continuous voltage rating. For the continuous working voltage rating, refer to equipment−level safety specification or DIN VDE V 0884−11 Safety and Insulation Ratings Table.

ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V, V_{CC} = 15 V, or 20 V or 25 V (Note 15) for typical values T_J = T_A = 25°C, for min/max values T_J = −40°C to +125°C, unless otherwise specified. (Note 15))

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PRIMARY POWER SUPPLY SECTION (VDD)						
I_{QVDD}	V_{DD} Quiescent Current	V_{IN+}= V_{IN-} = 0 V, V_{DD} = 5 V	500	715	1000	μA
		V_{IN+}= V_{IN-} = 0 V, V_{DD} = 15 V	600	870	1100	μA
		V_{IN+} = V_{IN-} = V_{DD}, V_{DD} = 5 V	500	720	1000	μA
		V_{IN+} = V_{IN-} = V_{DD}, V_{DD} = 15 V	600	870	1100	μA
I_{VDD}	V_{DD} Operating Current	V_{IN+} = V_{DD}, V_{IN-} = 0 V, V_{DD} = 5 V	4.5	6.4	8.0	mA
		V_{IN+} = V_{DD}, V_{IN-} = 0 V, V_{DD} = 15 V	5.0	6.6	8.4	mA
		f_{IN+} = 500 kHz, C_{OUT} = 200 pF, V_{DD} = 5 V	2.9	3.9	5.0	mA
		f_{IN+} = 500 kHz, C_{OUT} = 200 pF, V_{DD} = 15 V	3.0	4.1	5.2	mA
V_{DDUV+}	V_{DD} Supply Under−Voltage Positive−Going Threshold	V_{DD} = Sweep	2.7	2.8	2.9	V
V_{DDUV-}	V_{DD} Supply Under−Voltage Negative−Going Threshold	V_{DD} = Sweep	2.6	2.7	2.8	V
V_{DDHYS}	V_{DD} Supply Under−Voltage Lockout Hysteresis	V_{DD} = Sweep	–	0.1	–	V
t_{VDDUV}	Debounce Time (Note 16)		–	–	10	μs

ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V, V_{CC} = 15 V, or 20 V or 25 V (Note 15) for typical values $T_J = T_A$ = 25°C, for min/max values T_J = −40°C to +125°C, unless otherwise specified. (Note 15)) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SECONDARY POWER SUPPLY SECTION						
I_{QVCC}	V_{CC} Quiescent Current	$V_{IN+} = V_{IN-}$ = 0 V or 5 V, No Load	100	556	1200	μA
		V_{IN+} = 5 V, V_{IN-} = 0 V, No Load	100	670	1400	μA
I_{VCC}	V_{CC} Operating Current	f_{IN+} = 500 kHz, C_{OUT} = 200 pF, V_{CC} = 15 V	3.0	4.2	5.0	mA
		f_{IN+} = 500 kHz, C_{OUT} = 200 pF, V_{CC} = 20 V	3.7	5.2	6.2	mA
		f_{IN+} = 500 kHz, C_{OUT} = 200 pF, V_{CC} = 25 V	4.5	6.2	7.5	mA
VCC UVLO THRESHOLD (6−V UVLO VERSION)						
V_{CCUV+}	V_{CC} Supply Under−Voltage Positive−Going Threshold (Note 13)		5.7	6.0	6.4	V
V_{CCUV-}	V_{CC} Supply Under−Voltage Negative−Going Threshold		5.3	5.7	6.0	V
V_{CCHYS}	Under−Voltage Lockout Hysteresis		−	0.3	−	V
t_{VCCUV}	UVLO Filter Debounce Time (Note 16)		−	−	10	μs
VCC UVLO THRESHOLD (8−V UVLO VERSION)						
V_{CCUV+}	V_{CC} Supply Under−Voltage Positive−Going Threshold (Note 13)		8.2	8.7	9.2	V
V_{CCUV-}	V_{CC} Supply Under−Voltage Negative−Going Threshold		7.7	8.2	8.7	V
V_{CCHYS}	Under−Voltage Lockout Hysteresis		−	0.5	−	V
t_{VCCUV}	UVLO Filter Debounce Time (Note 16)		−	−	10	μs
VCC UVLO THRESHOLD (12−V UVLO VERSION)						
V_{CCUV+}	V_{CC} Supply Under−Voltage Positive−Going Threshold (Note 13)		11	12	13	V
V_{CCUV-}	V_{CC} Supply Under−Voltage Negative−Going Threshold		10	11	12	V
V_{CCHYS}	Under−Voltage Lockout Hysteresis		−	1.0	−	V
t_{VCCUV}	UVLO Filter Debounce Time (Note 16)		−	−	10	μs
VCC UVLO THRESHOLD (17−V UVLO VERSION)						
V_{CCUV+}	V_{CC} Supply Under−Voltage Positive−Going Threshold (Note 13)		16	17	18	V
V_{CCUV-}	V_{CC} Supply Under−Voltage Negative−Going Threshold		15	16	17	V
V_{CCHYS}	Under−Voltage Lockout Hysteresis		−	1.0	−	V
t_{VCCUV}	UVLO Filter Debounce Time (Note 16)		−	−	10	μs
LOGIC INPUT SECTION (IN+, AND IN−)						
V_{INH}	High Level Input Voltage		1.4	1.63	2.0	V
V_{INL}	Low Level Input Voltage		0.8	1.08	1.4	V
V_{INHYS}	Input Logic Hysteresis		−	0.55	−	V
I_{IN+H}	High Level Logic Input Bias Current at IN+	V_{IN+} = 5 V	33	40	52	μA
I_{IN+L}	Low Level Logic Input Bias Current at IN−	V_{IN+} = GND1	−	−	1.0	μA
I_{IN-H}	High Level Logic Input Bias Current at IN+	V_{IN-} = 5 V	−1.0	−	−	μA
I_{IN-L}	Low Level Logic Input Bias Current at IN−	V_{IN-} = GND1	−52	−40	−33	μA
R_{IN}	Logic Input Pull−Up/Down Resistance		95	125	155	kΩ

ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V, V_{CC} = 15 V, or 20 V or 25 V (Note 15) for typical values $T_J = T_A$ = 25°C, for min/max values T_J = −40°C to +125°C, unless otherwise specified. (Note 15)) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
NEGATIVE BIAS SECTION						
V_{EEUV+}	VEE Bias Under Voltage Threshold		0.75 x V_{REGREF}	0.8 x V_{REGREF}	0.85 x V_{REGREF}	V
$V_{EEUVHYS}$	VEE Under−Voltage Lockout Hysteresis		–	0.02 x V_{REGREF}	–	V
V_{EEOV+}	VEE Bias Over Voltage Threshold		1.15 x V_{REGREF}	1.2 x V_{REGREF}	1.25 x V_{REGREF}	V
$V_{EEOVHYS}$	VEE Over−Voltage Hysteresis		–	0.02 x V_{REGREF}	–	V
G_{REG}	Regulation OTA Gain		10	20	30	mmho
I_{REGCHG}	Charge Current (Note 16)	80% of Target > V_{GND2}, V_{CC} = 15 V	–	100	–	mA
I_{REGDIS}	Discharge Current (Note 16)	120% of Target < V_{GND2}, V_{CC} = 15 V	–	−100	–	mA
V_{REGPRE}	Precharge Disable Threshold (Note 16)		0.74 x V_{REGREF}	0.8 x V_{REGREF}	0.86 x V_{REGREF}	V
$V_{REGPREHYS}$	Precharge Disable Threshold Hysteresis (Note 16)		–	0.02 x V_{REGREF}	–	V
V_{REGREF}	Regulation Reference Voltage	For only V_{EE} = −2 V variant	1.9	2.0	2.1	V
		For only V_{EE} = −3 V variant	2.85	3.0	3.15	V
		For only V_{EE} = −4 V variant	3.8	4.0	4.2	V
		For only V_{EE} = −5 V variant	4.75	5.0	5.25	V
SHORT CIRCUIT SECTION						
$V_{CLP-OUT}$	Clamping Voltage, Sourcing ($V_{OUT} - V_{CC}$)	IN+ = High, IN− = Low, t_{CLAMP} = 10 μs I_{OUTH} or I_{OUT} = 500 mA	–	0.7	1.75	V
	Clamping Voltage, Sinking ($V_{EE} - V_{OUT}$)	IN+ = Low, IN− = High, t_{CLAMP} = 10 μs I_{OUTH} or I_{OUT} = −500 mA	–	0.24	0.5	V
GATE DRIVE SECTION						
I_{OUT+}	Source Peak Current (Note 16)	V_{IN+} = 5 V, PW ≤ 5 μs	2.6	4.5	–	A
I_{OUT-}	Sink Peak Current (Note 16)	V_{IN+} = 0 V, PW ≤ 5 μs	7.0	9.0	–	A
R_{OH}	Output Resistance at High State	I_{OUTH} = 100 mA	–	1.4	2.8	Ω
R_{OL}	Output Resistance at Low State	I_{OUTL} = 100 mA	–	0.5	1.0	Ω
V_{OH}	High Level Output Voltage ($V_{CC} - V_{OUT}$)	I_{OUTH} = 100 mA	–	140	280	mV
V_{OL}	Low Level Output Voltage ($V_{OUT} - V_{EE}$)	I_{OUTL} = 100 mA	–	50	100	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

13. All V_{CC} UVLO threshold voltages are given with respect to GND2 pin.
14. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A$ = 25°C.
15. V_{CC} = 15 V is used for the test condition of 5−V UVLO, V_{CC} = 20 V is used for 8−V UVLO, and V_{CC} = 25 V is used for 12−V and 17−V UVLO. All voltage values are given with respect to VEE pin.
16. These parameters verified by bench test only and not tested in production

DYNAMIC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{PDON}	Turn−On Propagation Delay from IN to OUT	C_{LOAD} = 0 nF	20	36	55	ns
t_{PDOFF}	Turn−Off Propagation Delay from IN to OUT		20	36	55	ns
t_{PWD}	Pulse Width Distortion ($t_{PDON} - t_{PDOFF}$)		−5	–	5	ns
$t_{SK(PP)}$	Propagation Part−to−part Skew (Note 17)		−20	–	20	ns
$t_{VPOR\ to\ OUT}$	Power−up Delay from the V_{POR} to Output (Note 17)	See the Figure 53	–	18	–	μs
t_R	Turn−On Rise Time	C_{LOAD} = 1.8 nF	–	12	22	ns
t_F	Turn−Off Fall Time	C_{LOAD} = 1.8 nF	–	8.3	22	ns
t_{PW}	Minimum Input Pulse Width that Change Output State	C_{LOAD} = 0 nF	–	15	35	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
17. These parameters verified by bench test only and not tested in production

INSULATION CHARACTERISTICS CURVES

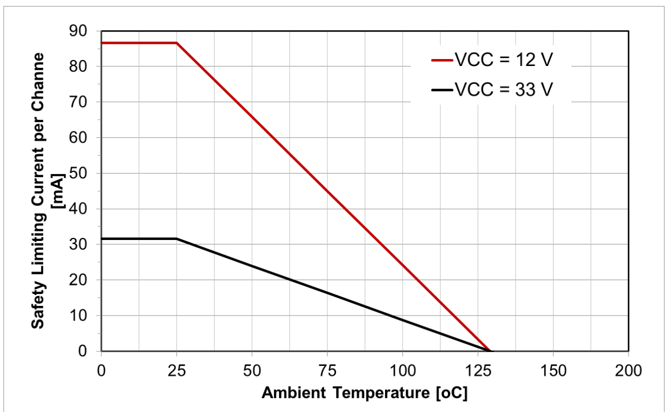


Figure 6. Thermal Derating Curve for Safety−related Limiting Current (θ_{JA} = 100°C/W) (Note 7)

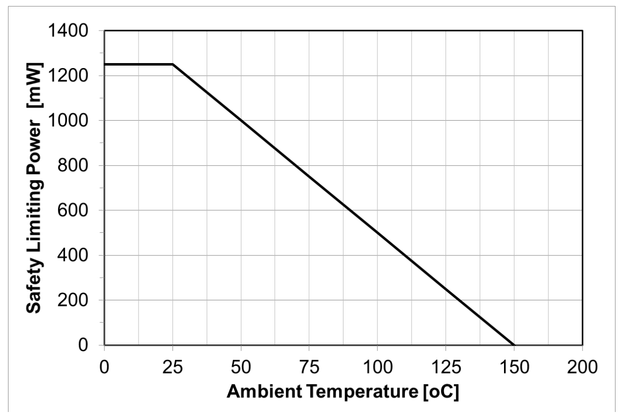


Figure 7. Thermal Derating Curve for Safety−related Limiting Power (θ_{JA} = 100°C/W) (Note 7)

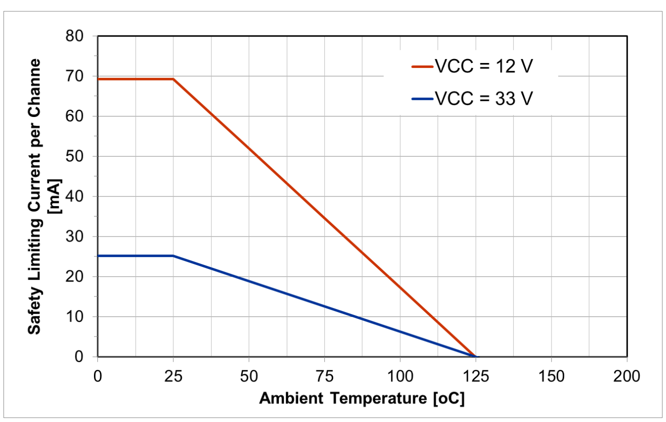


Figure 8. Thermal Derating Curve for Safety−related Limiting Current (θ_{JA} = 120°C/W) (Note 8)

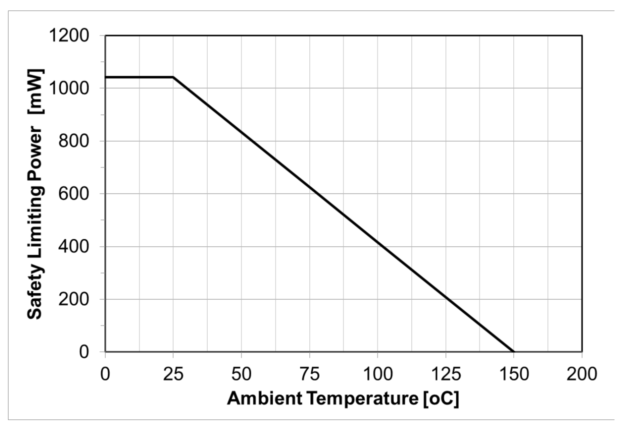


Figure 9. Thermal Derating Curve for Safety−related Limiting Power (θ_{JA} = 120°C/W) (Note 8)

TYPICAL CHARACTERISTICS

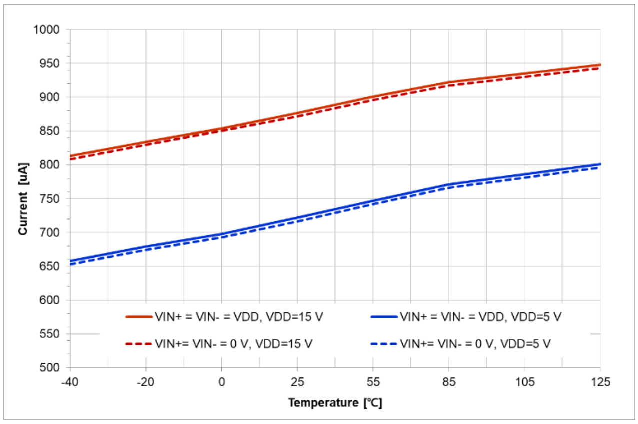


Figure 10. V_{DD} Quiescent Current vs. Temperature

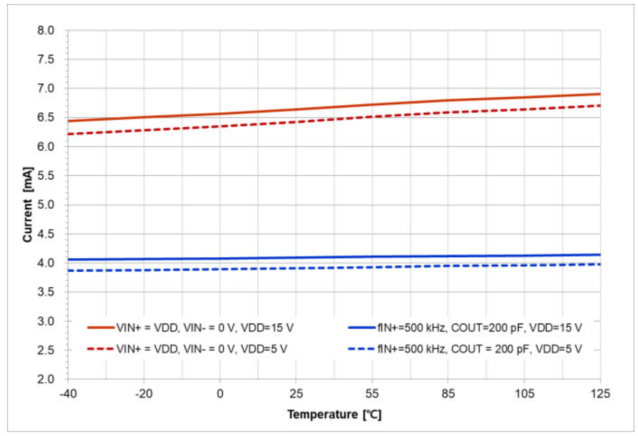


Figure 11. V_{DD} Quiescent Current vs. Temperature

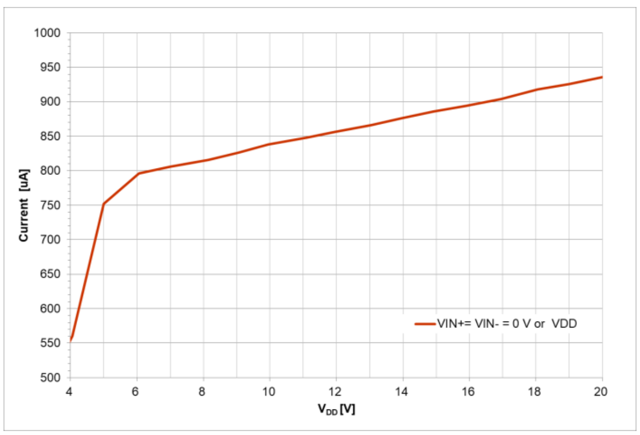


Figure 12. V_{DD} Quiescent Current vs. V_{DD}

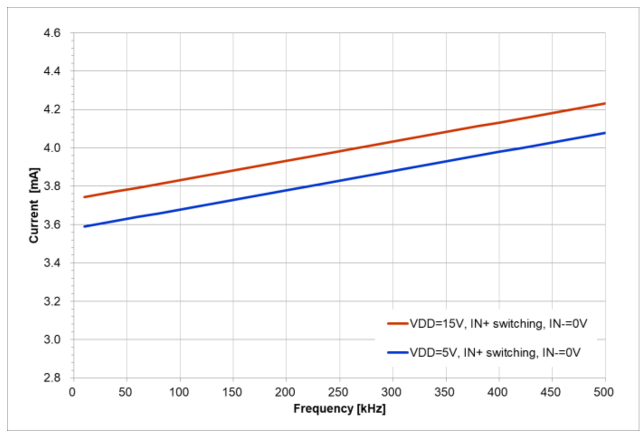


Figure 13. V_{DD} Operating Current vs. Switching Frequency

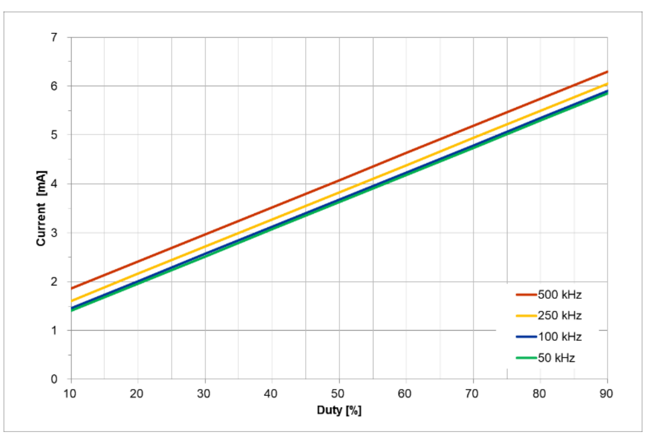


Figure 14. V_{DD} Operating Current vs. Duty (V_{DD} = 5 V, IN+ Switching with Different Frequency, IN− = 0 V)

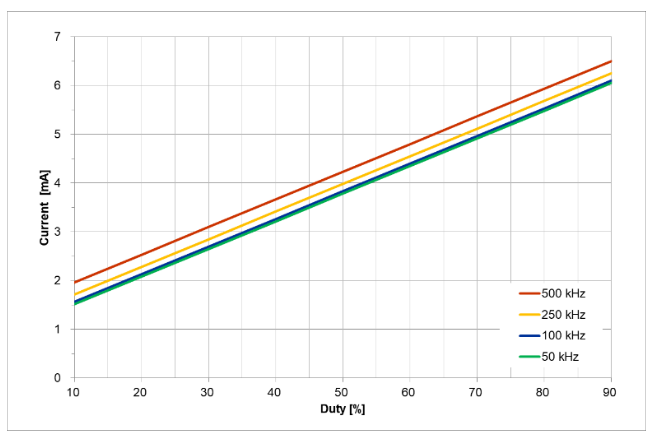


Figure 15. V_{DD} Operating Current vs. Duty (V_{DD} = 15 V, IN+ Switching with Different Frequency, IN− = 0 V)

TYPICAL CHARACTERISTICS (CONTINUED)

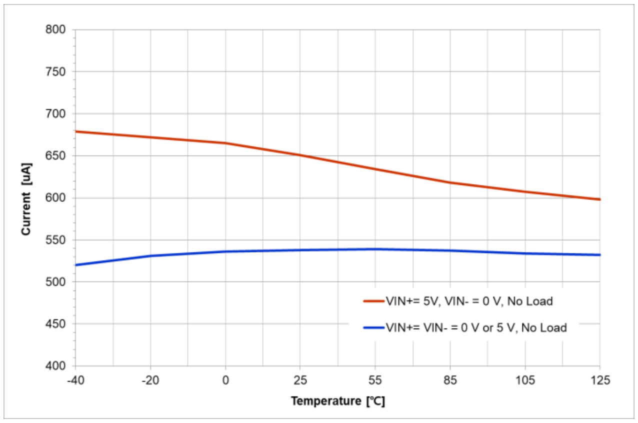


Figure 16. Quiescent V_{CC} Supply Current vs. Temperature

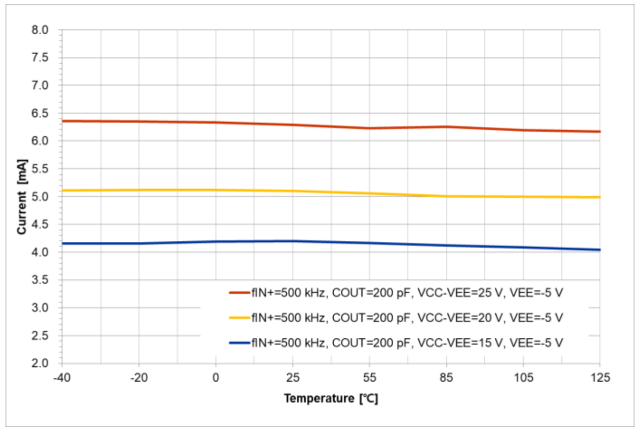


Figure 17. V_{CC} Operating Current vs. Temperature

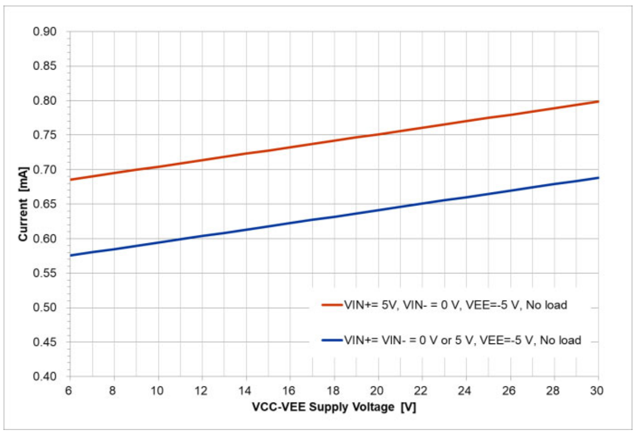


Figure 18. Quiescent V_{CC} Supply Current vs. V_{CC} Supply Voltage

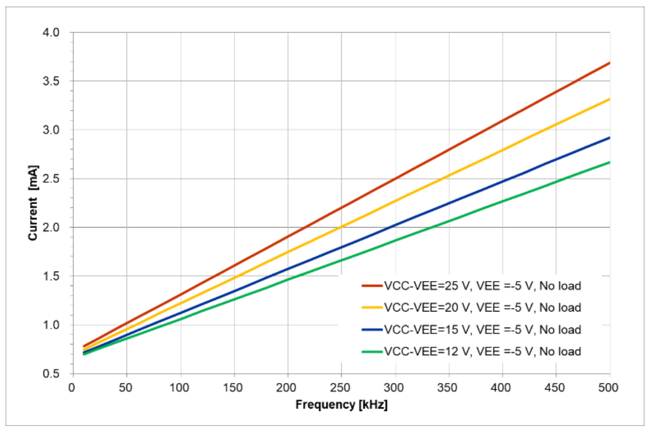


Figure 19. V_{CC} Operating Current vs. Switching Frequency (V_{CC} – V_{EE} = 12/15/20/25 V, V_{EE} = –5 V and No Load)

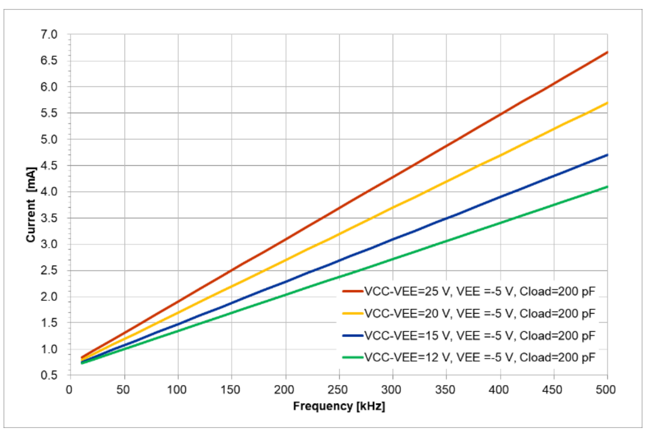


Figure 20. V_{CC} Operating Current vs. Switching Frequency (V_{CC} – V_{EE} = 12/15/20/25 V, V_{EE} = –5 V and C_{LOAD} = 200 pF)

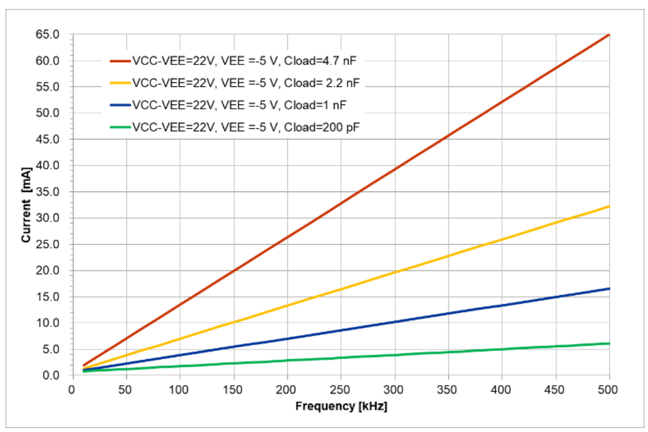


Figure 21. V_{CC} Operating Current vs. Switching Frequency (V_{CC} – V_{EE} = 22 V, V_{EE} = –5 V and Different C_{LOAD})

TYPICAL CHARACTERISTICS (CONTINUED)

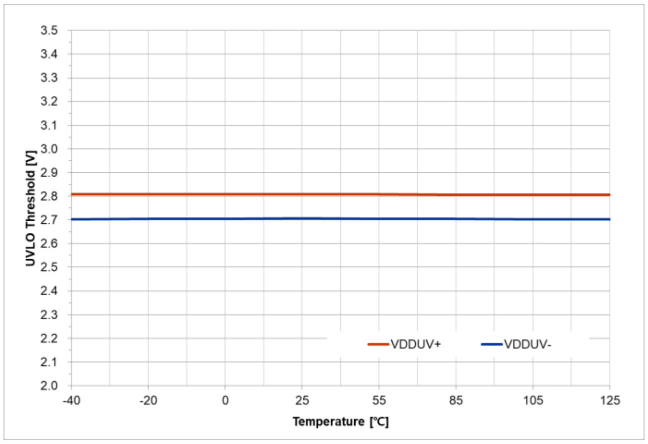


Figure 22. V_{DD} UVLO vs. Temperature

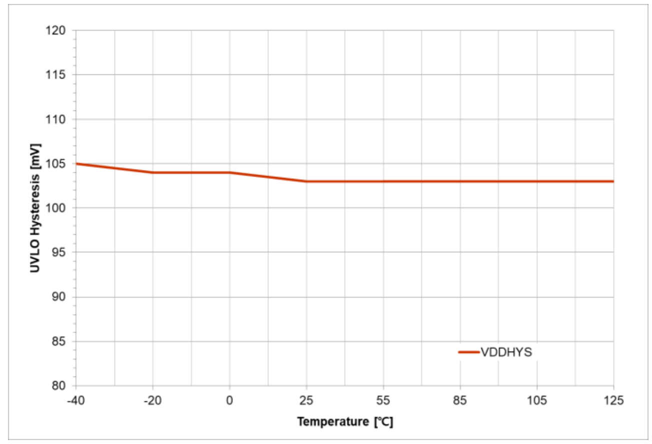


Figure 23. V_{DD} UVLO Hysteresis vs. Temperature

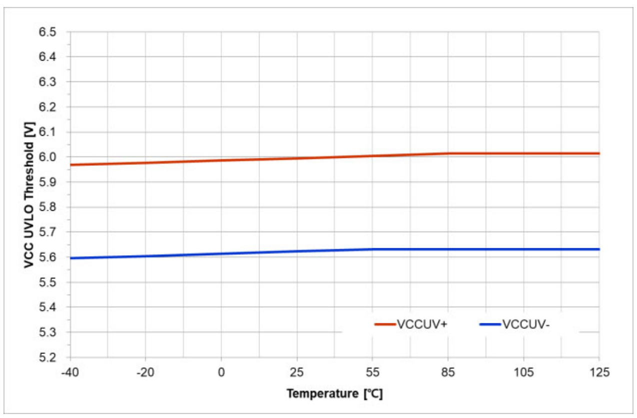


Figure 24. V_{CC} 6−V UVLO Threshold vs. Temperature

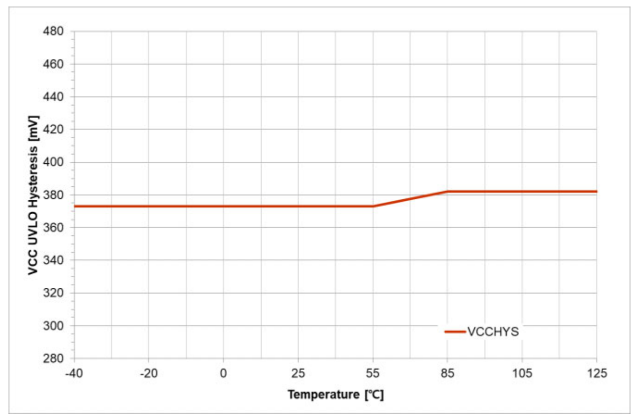


Figure 25. V_{DD} 6−V UVLO Hysteresis vs. Temperature

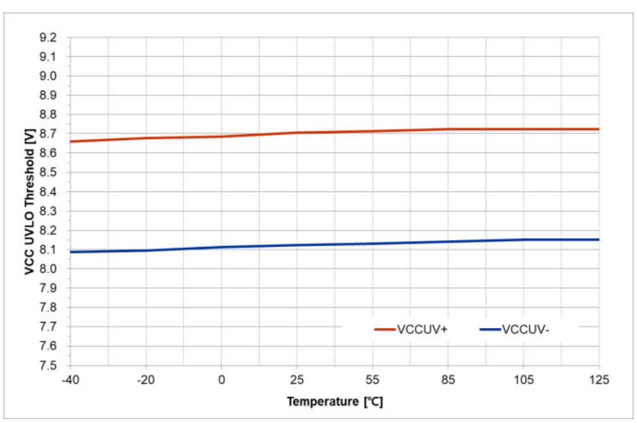


Figure 26. V_{CC} 8−V UVLO Threshold vs. Temperature

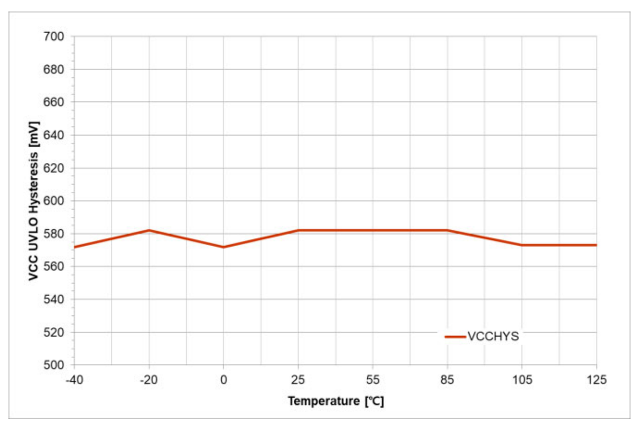


Figure 27. V_{DD} 8−V UVLO Hysteresis vs. Temperature

TYPICAL CHARACTERISTICS (CONTINUED)

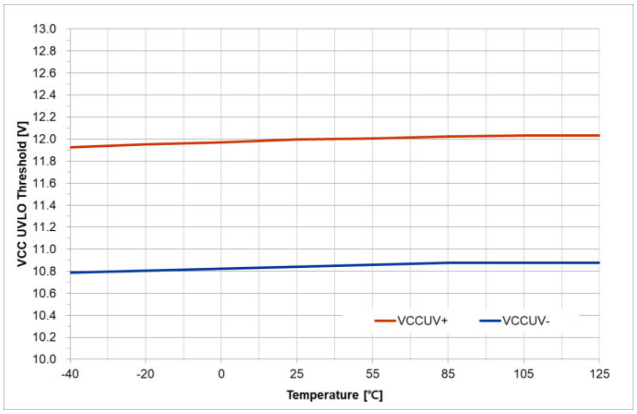


Figure 28. V_{CC} 12−V UVLO Threshold vs. Temperature

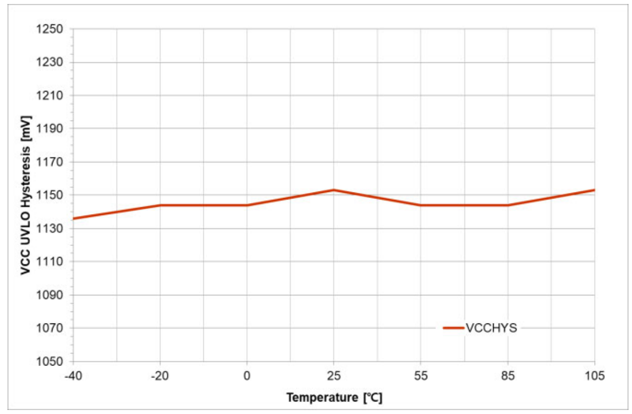


Figure 29. V_{CC} 12−V UVLO Hysteresis vs. Temperature

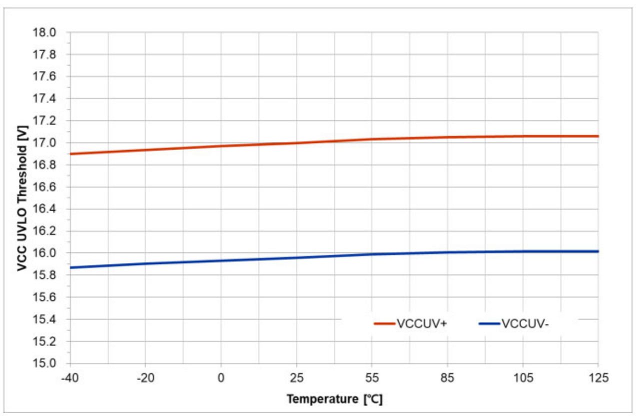


Figure 30. V_{CC} 17−V UVLO Threshold vs. Temperature

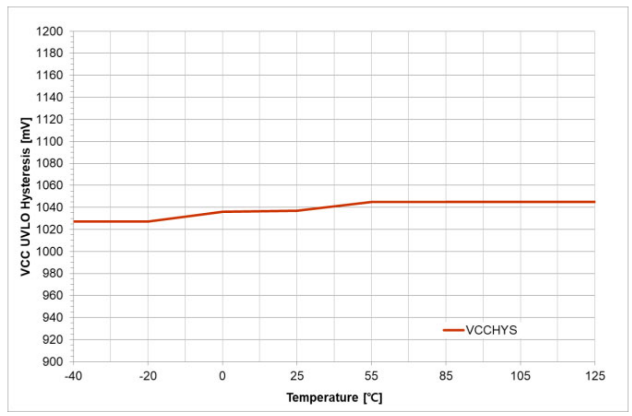


Figure 31. V_{CC} 17−V UVLO Hysteresis vs. Temperature

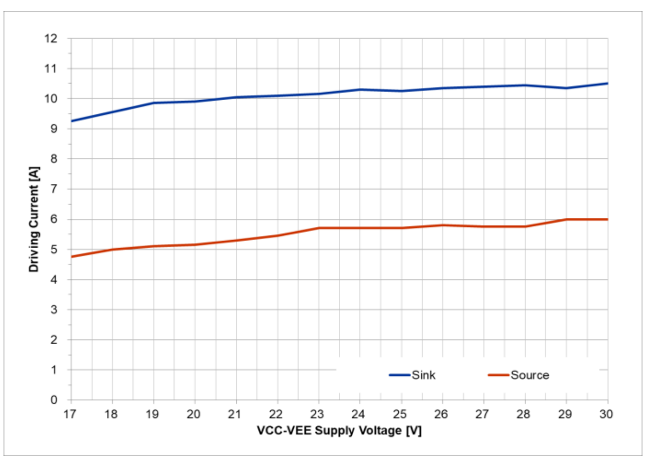


Figure 32. Figure 32. Output Current vs. V_{CC} Supply Voltage

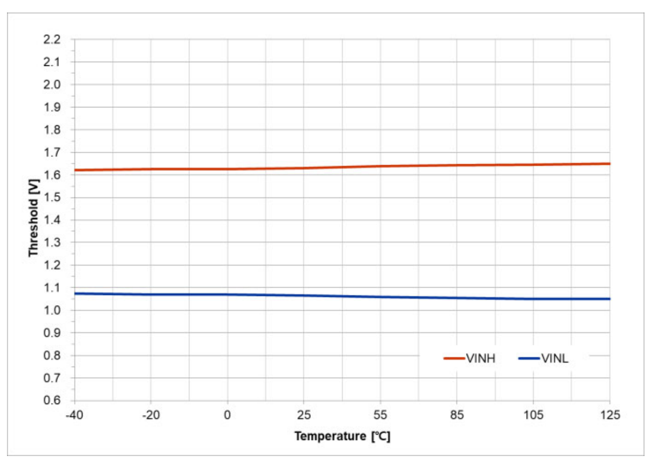


Figure 33. Input Logic Threshold vs. Temperature

TYPICAL CHARACTERISTICS (CONTINUED)

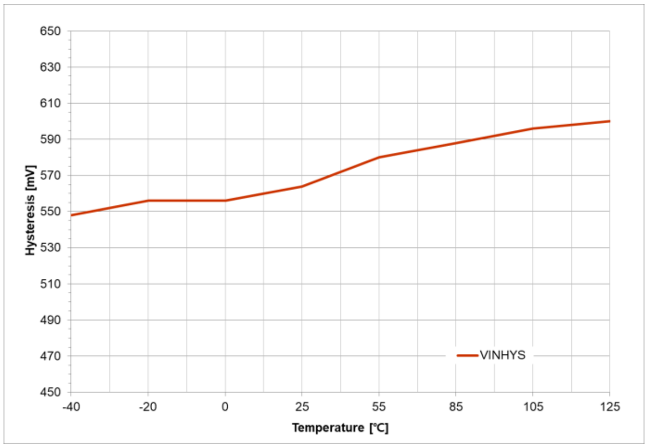


Figure 34. Input Logic Hysteresis vs. Temperature

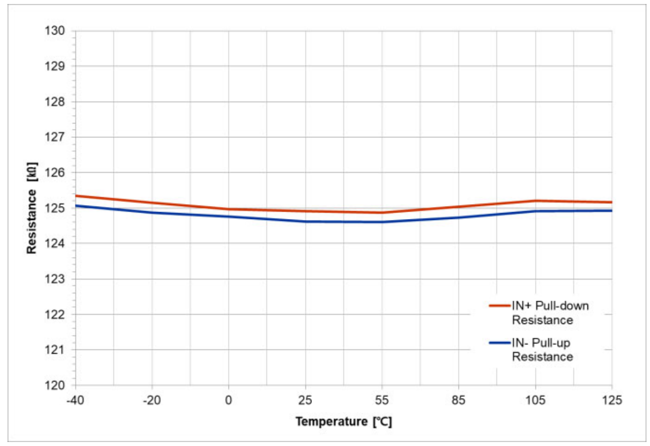


Figure 35. Logic Input Pull−Up/Down Resistance vs. Temperature

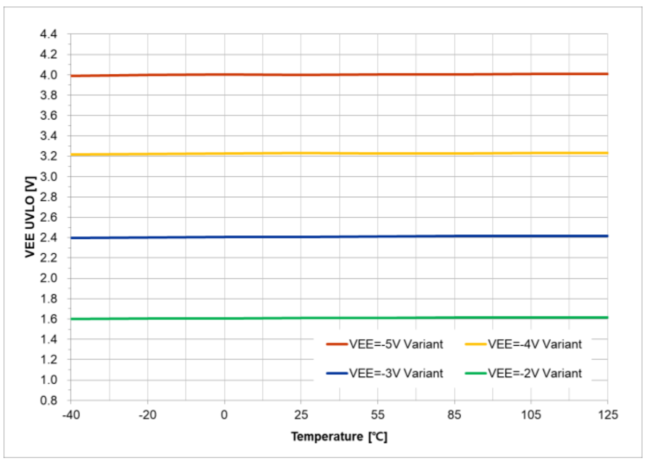


Figure 36. V_{EE} Bias Under Voltage Threshold vs. Temperature

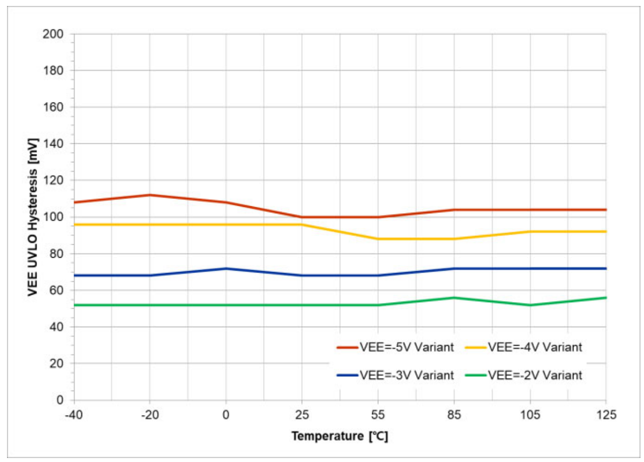


Figure 37. V_{EE} Bias Under−Voltage Lockout Hysteresis vs. Temperature

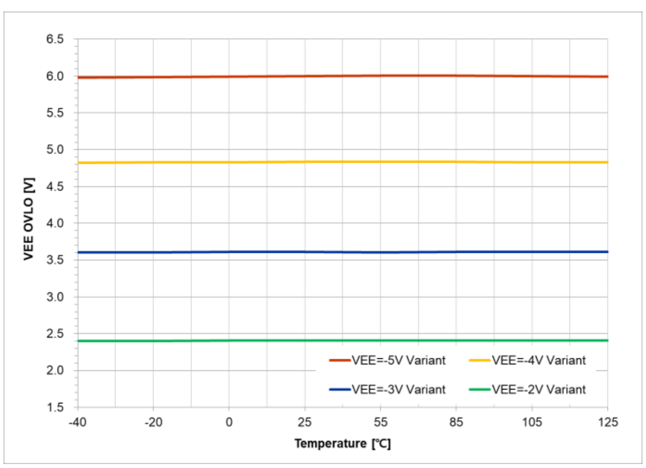


Figure 38. V_{EE} Bias Over Voltage Threshold vs. Temperature

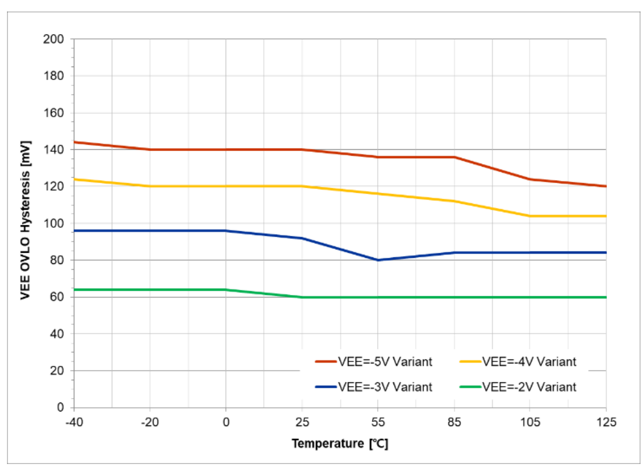


Figure 39. V_{EE} Bias Over−Voltage Lockout Hysteresis vs. Temperature

TYPICAL CHARACTERISTICS (CONTINUED)

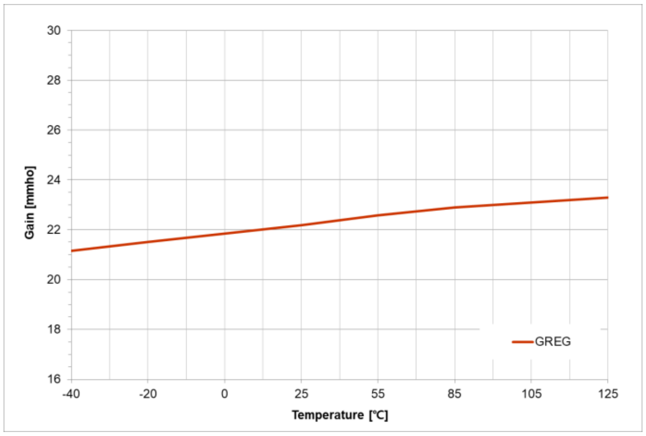


Figure 40. Regulation OTA Gain vs. Temperature

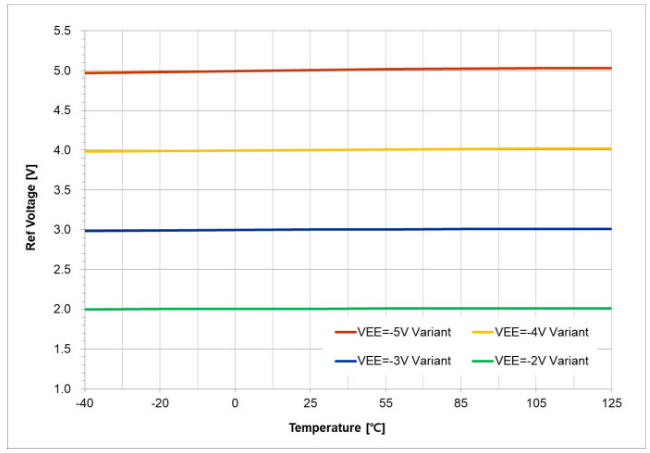


Figure 41. V_{EE} Regulation Reference Voltage vs. Temperature

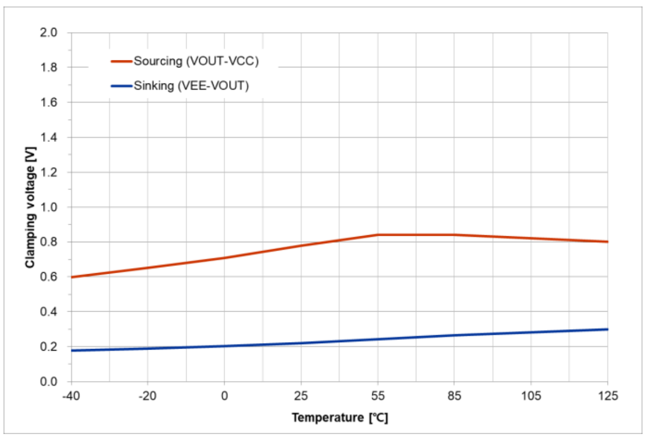


Figure 42. Clamping Voltage vs. Temperature

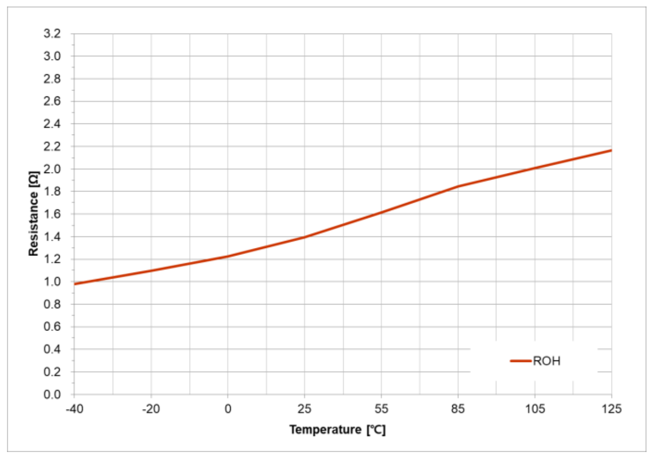


Figure 43. Output Resistance at High State vs. Temperature

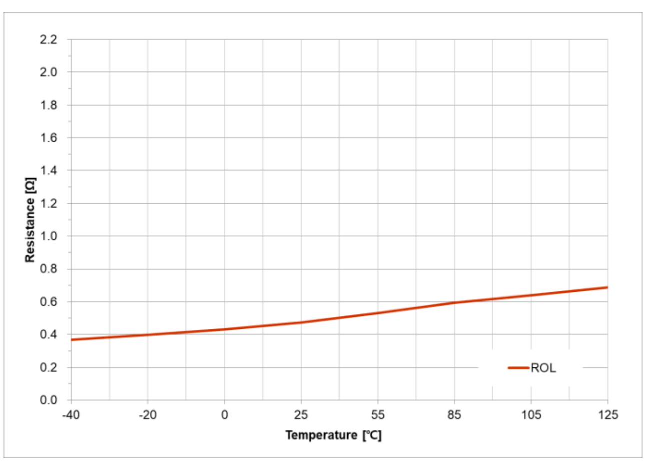


Figure 44. Output Resistance at Low State vs. Temperature

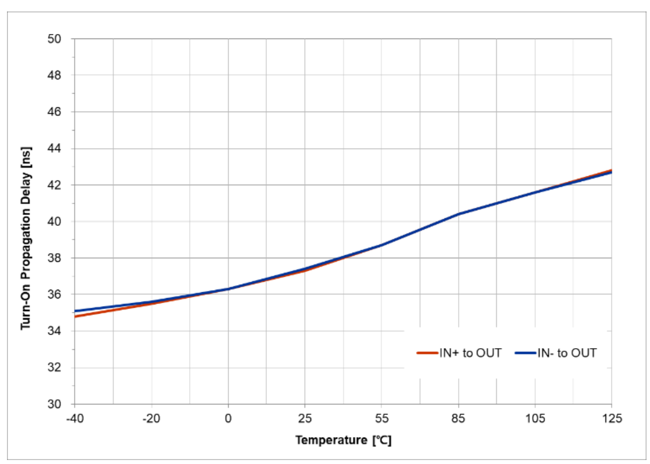


Figure 45. Turn−on Propagation Delay vs. Temperature (C_{LOAD} = 0 nF)

TYPICAL CHARACTERISTICS (CONTINUED)

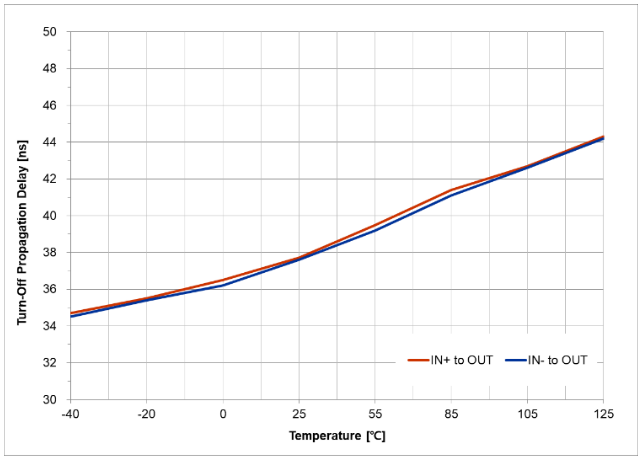


Figure 46. Turn−off Propagation Delay vs. Temperature (C_{LOAD} = 0 nF)

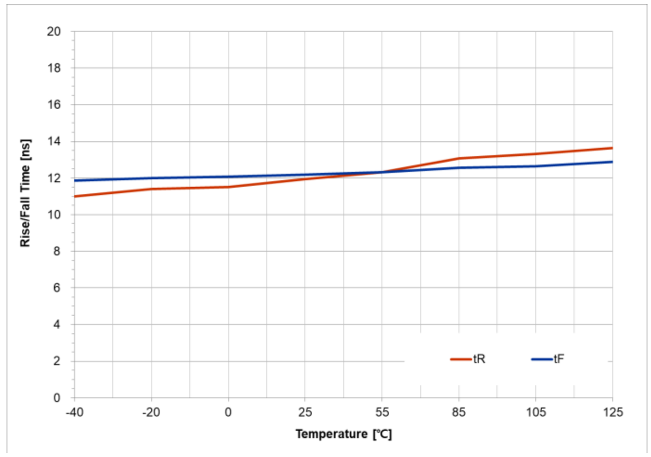


Figure 47. Rise/Fall Time vs. Temperature (C_{LOAD} = 1.8 nF)

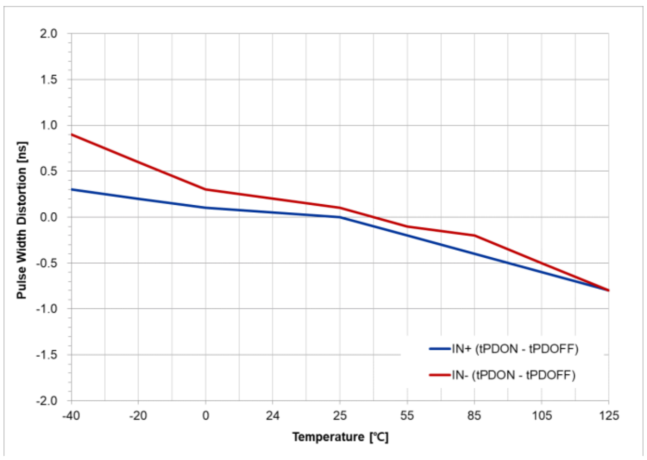


Figure 48. Pulse Width Distortion vs. Temperature (CLOAD = 0 nF)

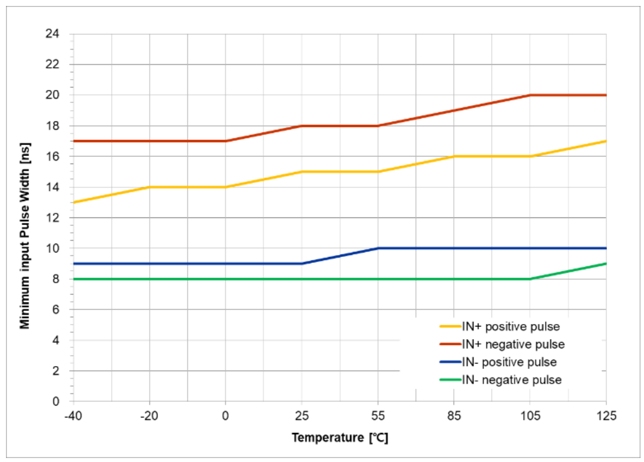


Figure 49. Minimum Input Pulse Width vs. Temperature

Switching Time Definitions

Figure 50 shows the switching time waveforms definitions of the turn−on (t_{PDON}) and turn−off (t_{PDOFF}) propagation delay times among the driver's input signal IN+ and output signal OUT. The typical values of the propagation delay (t_{PDON}, t_{PDOFF}), pulse width distortion (t_{PWD}) and delay matching between channels times are specified in the electrical characteristics table.

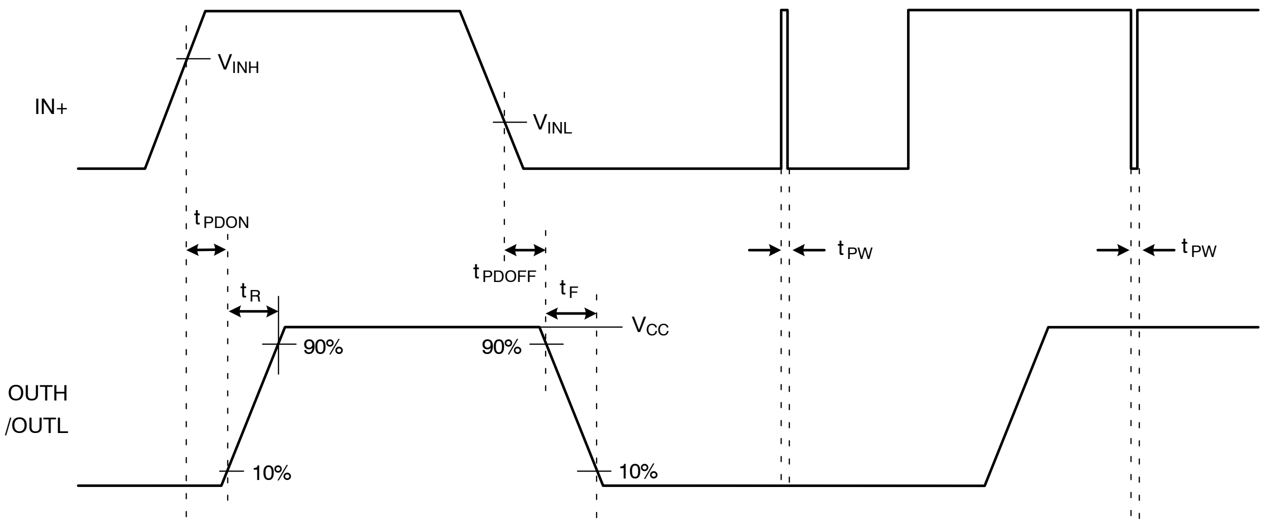


Figure 50. Switching Time Definition

General Description and Features

Input to Output Operation Definitions

The NCV51752 provides important protection functions such as independent under−voltage lockout for gate driver. Figure 51 shows an overall input to output timing diagram. Under−Voltage Lockout protection on the primary− and secondary−sides power supplies events in the *CASE−A, B and C* and the gate driver output (OUT) is immediately turn−off when two input signals (IN+ and IN−) are HIGH at same time in the *CASE−D*. The negative bias control circuit is enabled after the V_{CC} power delay time, $t_{VPOR\ to\ OUT}$, during initial V_{CC} start−up or after POR event.

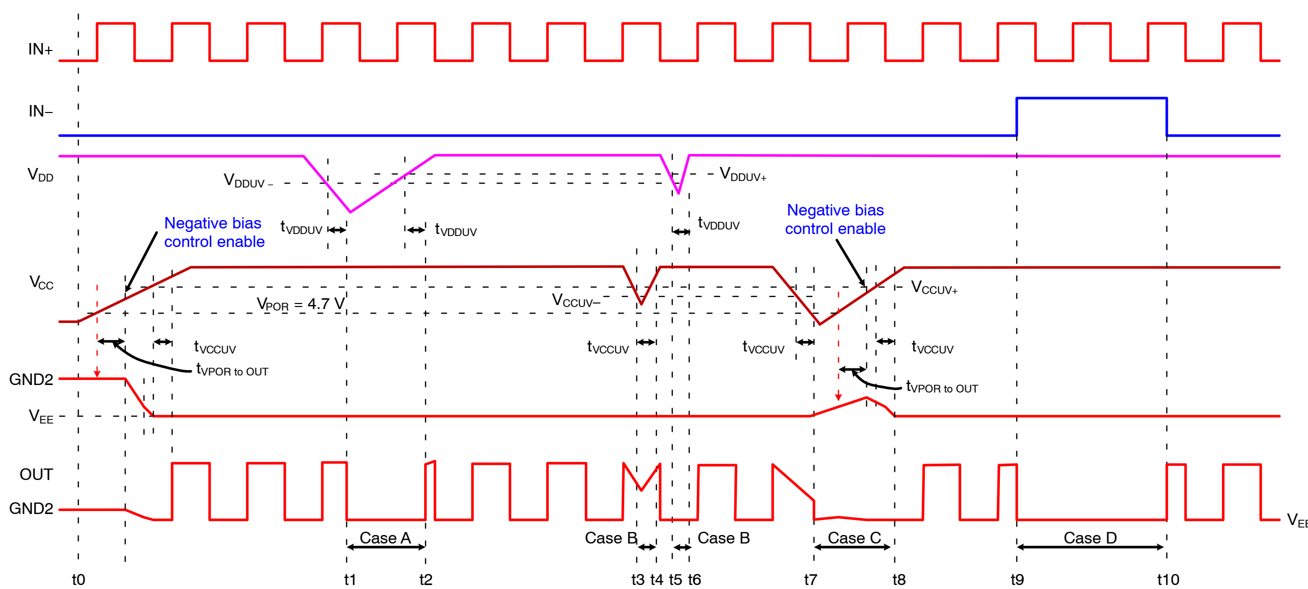


Figure 51. Overall Operating Waveforms Definitions

Under−Voltage Lockout Protection V_{DD}, V_{CC} and V_{EE}

The NCV51752 provides the protection features include Under−Voltage Lockout (UVLO) of power supplies on primary−side (V_{DD}), and secondary−side (V_{CC} and V_{EE}).

The NCV51752 provides the Under−Voltage Lockout (UVLO) protection function for V_{DD} in primary−side and gate drive output for V_{CC} in secondary−side as shown in Figure 52. The gate driver is running when the V_{DD} supply voltage is greater than the specified under−voltage lockout threshold voltage (e.g. typically 2.8 V).

In addition, gate output driver has an under−voltage lockout protection (UVLO) function in secondary−side (e.g. V_{CC}) need to be greater than specified UVLO threshold level in secondary−side to let the output operate per input signal. The typical V_{CC} UVLO threshold voltage levels with respect to GND2 for each option are per below Table 1.

Table 1. V_{CC} UVLO OPTION TABLE

Option	V_{CC} UVLO Threshold	V_{CC} UVLO Hysteresis	V_{CC} UVLO Referenced	Unit
6−V	6.0	0.3	GND2	V
8−V	8.7	0.5	GND2	V
12−V	12	1.0	GND2	V
17−V	17	1.0	GND2	V

The UVLO protection has an hysteresis to provide immunity to short V_{CC} drops that can occur. Additionally, the V_{EE} voltage rail includes an internally fixed under−voltage lockout (UVLO) set to 80% of the target V_{EE} value. Since V_{CC} and V_{EE} are each monitored by independent UVLO circuits, the NCV51752 is smart enough to realize when both voltage rails are within limits deemed safe for switching a given SiC MOSFET.

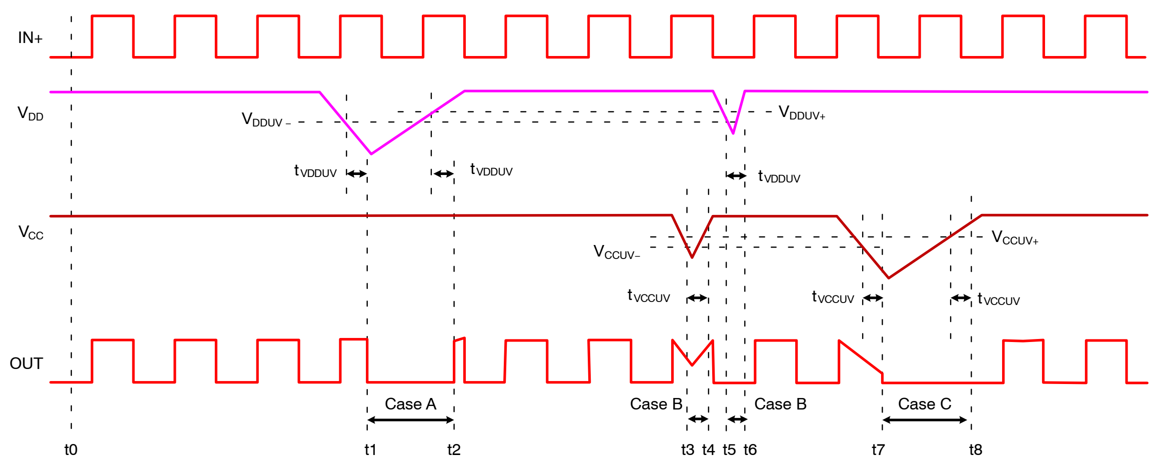


Figure 52. Timing Chart Under−Voltage Lockout Protection

Power−up VCC UVLO Delay to OUTPUT

To provide a variety of Under−Voltage Lockout (UVLO) thresholds NCV51752 has a power−up delay time during initial VCC start−up or after POR event.

Before the gate driver is ready to deliver a proper output state, there is a power−up delay time from the V_{CC} power−on reset (POR) threshold to output and it is defined as $t_{VPOR\ to\ OUT}$. (e.g. typically18 μs). Figure 53 shows the V_{CC} power−up UVLO delay time diagram.

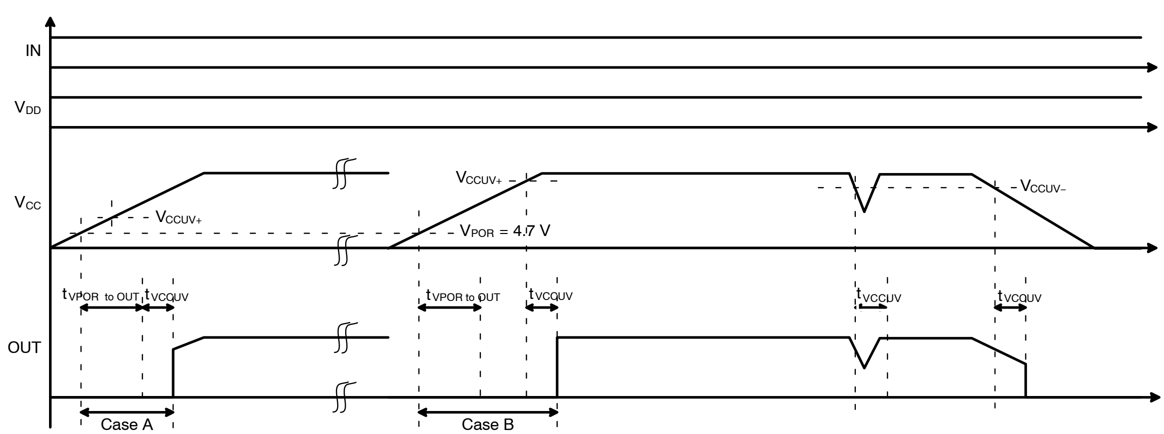


Figure 53. V_{CC} Power−up UVLO Delay Time

Functional Mode Table

Table 2 shows the functional modes for the NCV51752 assuming V_{DD} and V_{CC} are in the recommended ranges.

Table 2. FUNCTIONAL MODES

Input		Gate Drive Output
IN+	IN−	OUT
LOW	X (Note 18)	Low
X (Note 18)	HIGH	Low
HIGH	LOW	High

18. X: Don't care

Negative Bias Control Function

The NCV51752 provides a simple way to generate negative bias in the gate drive loop as shown in Figure 54. This negative bias is very useful in case of PCB layout and/or package leads generating high ringing in power transistor Vgs. This ringing of the gate voltage generally occurs under high di/dt and dv/dt switching conditions.

To keep the ringing below threshold voltage to prevent spurious Turn−ON generally applies a negative bias on the gate drive. The NCV51752 offers different options to generate −2 V, −3 V, −4 V and −5 V to accommodate all configurations and types of power transistors.

Additionally, the negative bias voltage rail includes an internally fixed under−voltage lockout (UVLO) set to 80% of the target V_{EE} value. The GND2 capacitor between GND2 and V_{EE} pins, C_{GND2}, will develop a voltage across the pins. The capacitor voltage is controlled by charging and discharging current sources. This feature allows minimizing the PCB size as well as cost and it precisely controls the negative bias voltage between GND2 and V_{EE} pins regardless of the switching frequency and duty cycle.

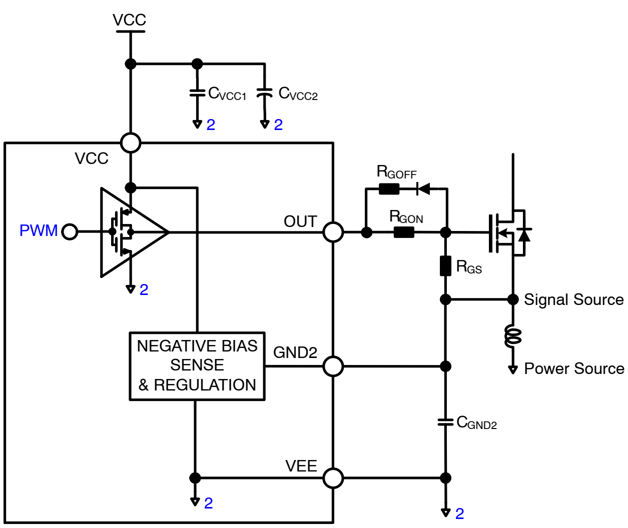


Figure 54. Supplying V_{EE} with Negative Bias Control

Figure 55 shows the timing chart of the negative bias control. If the GND2 capacitor voltage is below the specified target threshold voltage, e.g. V_{CGND2} < 80% of the target, the GND2 capacitor quickly charge up to the 80% of target threshold voltage by an internal current source, I_{REGCHG}. If the GND2 capacitor voltage is between 80% and 120 % of the target, the GND2 capacitor can be regulated by an internal operational transconductance amplifier (OTA) according to the voltage difference between GND2 and V_{EE} pins. If the GND2 capacitor voltage is exceed the specified target threshold voltage, e.g. V_{CGND2} > 120% of the target, an internal current source, I_{REGDIS}, can discharging the GND2 capacitor up to the 120% of target threshold voltage.

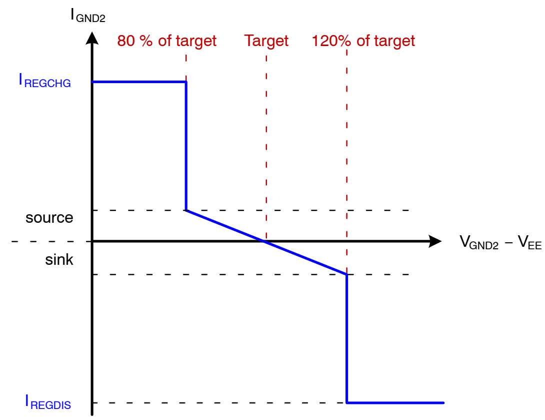


Figure 55. Timing Chart Negative Bias Control

There is also a pre−charge current mechanism to quickly reach the specified target threshold voltage, e.g. V_{CGND2} < 80% of the target, before starting as shown in Figure 56. (between after power−up delay time and 80% of the target threshold).

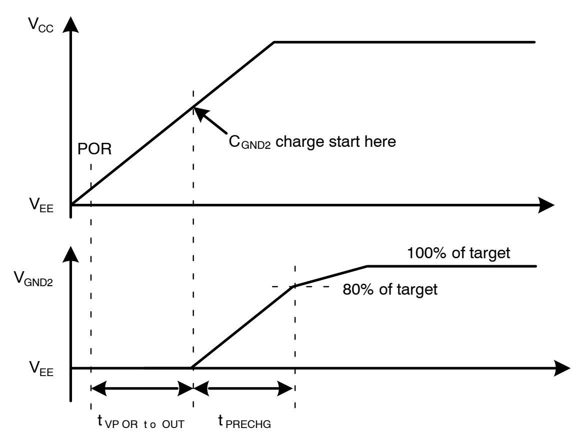


Figure 56. Timing Chart Negative Bias Control During Precharge

APPLICATION INFORMATION

This section provides application guidelines when using the NCV51752.

Power Supply Recommendations

The NCV51752 have the V_{DD} input power supply supports a wide voltage range from 3 V to 20 V with respect to GND1 pin and the V_{CC} output supply supports a voltage range from 6.5 V to 30 V with respect to V_{EE} pin. In additional, the NCV51752 provides a simple way to generate negative bias up to −5 V between GND2 and V_{EE} pins. It is important to remember that during the Turn−On of switch the output current to the Gate is drawn from the V_{CC} supply pin. The V_{CC} local bypass capacitor should be placed between the V_{CC} and V_{EE} pins with a value of at least ten times the gate capacitance, and an additional capacitor 100−nF in parallel for device biasing and both capacitors located as close to the device as possible.

In additional, for the negative bias supply capacitor, C_{GND2}, should be placed between GND2 and V_{EE} pins with a value of at least few hundred nanofarads as shown in Figure 54.

A low ESR, ceramic surface mount capacitors are recommended. Similarly, the V_{DD} bypass capacitor should also be placed between the V_{DD} and GND1 pins for input logic power supply. We recommend using 2 capacitors; at least 100 nF ceramic surface−mount capacitor with few microfarads added in parallel and both capacitors also located as close to the pins as shown in Figure 57.

Input Stage

The input signal pins (IN+, and IN−) of the NCV51752 are based on the TTL compatible input−threshold logic that is independent of the V_{DD} supply voltage.

The logic level compatible input provides a typically HIGH and LOW threshold of 1.7 V and 1.1 V respectively. The input signal pins impedance is 125 kΩ typically and the IN+ pin is pulled to GND1 pin and IN− pin is pulled to V_{DD} pin as shown in Figure 57.

For non−inverting input logic signal is applied to IN+ while the IN− input can be used as an enable function. If IN− is pulled HIGH, the driver output remains LOW state, regardless of the state of IN+. To enable the driver output, IN− should be tied to GND1 through a few ten kΩ resistor (e.g.10 kΩ) or can be used as an active LOW enable pull down.

- Non−inverting input IN+ controls the driver output while inverting input IN− is set to LOW
- Inverting input IN− controls the driver output while non−inverting input IN+ is set to HIGH

An RC filter is recommended to be added on the input signal pins to reduce the impact of system noise and ground bounce, the time constant of the RC filter as shown in Figure 57. Such a filter should use an R_{IN} in the range of 0 Ω to 100 Ω and a C_{IN} between 10 pF and 100 pF.

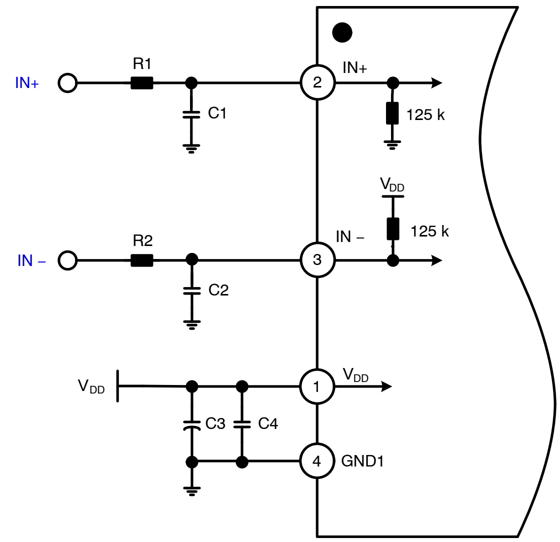


Figure 57. Schematic of Input Stage

Output Stage

The output driver stage of the NCV51752 features a pull−up structure and a pull−down structure.

The pull up structure of the consists of a PMOS stage ensuring to pull all the way to the V_{CC} rail and the pull−down structure of the consists of a NMOS device as shown in Figure 58. The output voltage swing between V_{CC} and V_{EE} provides rail−to−rail operation with respect to GND2 pin when used the GND2 pin connect to the emitter or source of power device. The power device is turned off with a negative voltage on the gate with respect to the source pin. This configuration prevents the power device from unintentionally turning on because of current induced from the Miller effect.

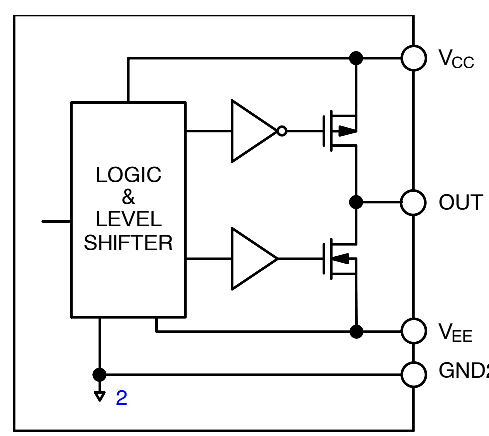


Figure 58. Schematic of Output Stage

The output impedance of the pull−up and pull−down switches shall be able to provide about +4.5 A and −9 A peak currents typical at 25°C and the minimum sink and source peak currents are −7 A sink and +2.6 A source at 125°C.

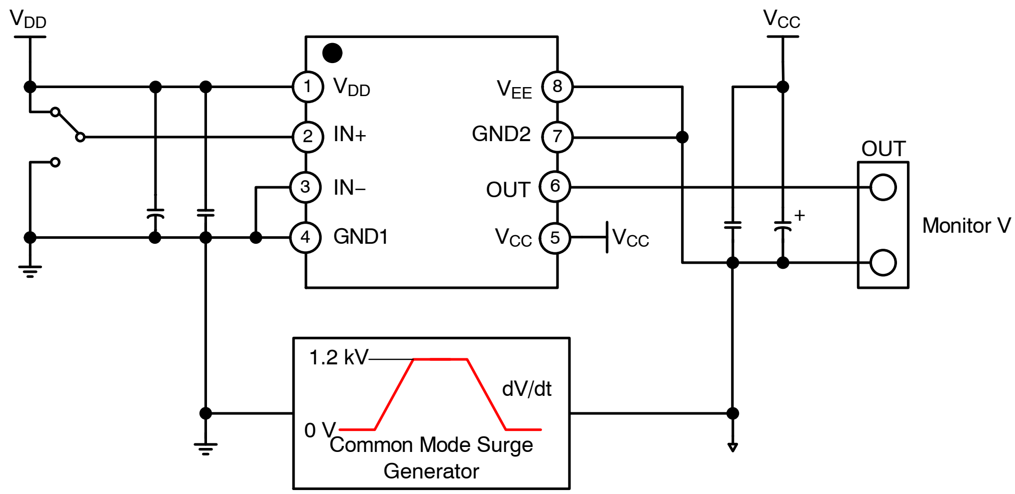


Figure 59. Common Mode Transient Immunity Test Circuit

PCB Layout Guideline

To improve the switching characteristics and efficiency of design, the following should be considered before beginning a PCB layout.

Component Placement

- Keep the input/output traces as short as possible. Minimize influence of the parasitic inductance and capacitance on the layout. (To maintain low signal−path inductance, avoid using via.)
- Placement and routing for supply bypass capacitors for V_{DD}, V_{CC} and V_{EE}, and gate resistors need to be located as close as possible to the gate driver.
- The gate driver should be located switching device as close as possible to decrease the trace inductance and avoid output ringing.

Grounding Consideration

- Have a solid ground plane underneath the high−speed signal layer.

High−Voltage (VISO) Consideration

To ensure isolation performance between the primary and secondary side, any PCB traces or copper should be not placed under the driver device as shown in Figure 60.

A PCB cutout is recommended to avoid contamination that may impair the isolation performance of NCV51752.

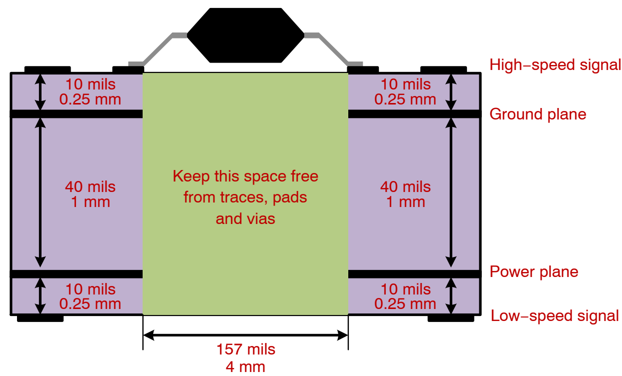


Figure 60. Recommended Layer Stack

Figure 61 shows the 3D layout of the top view of an evaluation board. The component's location of the PCB cutout between primary and secondary sides ensures isolation performance.

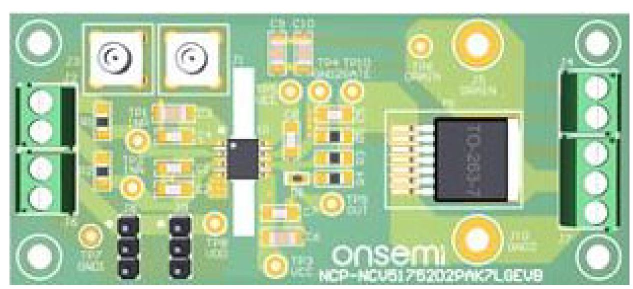
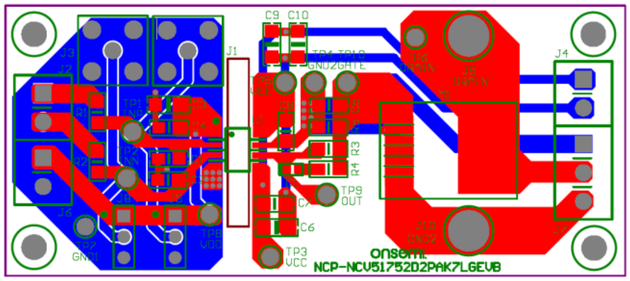
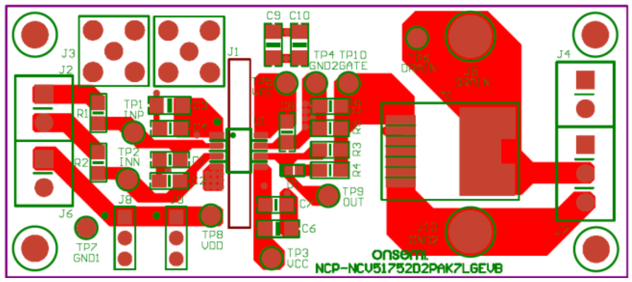


Figure 61. 3−D PCB View

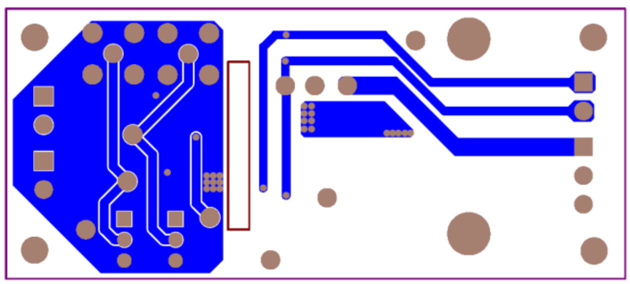
Figure 62 shows the top and bottom layer traces and copper of printed circuit board layout.



(A) Top & Bottom View



(B) Top View



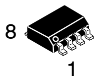
(C) Bottom View

Figure 62. Printed Circuit Board

ORDERING INFORMATION

Device	Description	Package	UVLO	GND2 − VEE	Shipping†
NCV51752AADR2G*	High current single isolated MOS driver with GND2−VEE control	SOIC−8 NB (Pb−Free)	6 V	2 V	2500 / Tape & Reel
NCV51752ABDR2G*				3 V	2500 / Tape & Reel
NCV51752ACDR2G*				4 V	2500 / Tape & Reel
NCV51752ADDR2G*				5 V	2500 / Tape & Reel
NCV51752BADR2G*		SOIC−8 NB (Pb−Free)	8 V	2 V	2500 / Tape & Reel
NCV51752BBDR2G*				3 V	2500 / Tape & Reel
NCV51752BCDR2G*				4 V	2500 / Tape & Reel
NCV51752BDDR2G*				5 V	2500 / Tape & Reel
NCV51752CADR2G*		SOIC−8 NB (Pb−Free)	12 V	2 V	2500 / Tape & Reel
NCV51752CBDR2G				3 V	2500 / Tape & Reel
NCV51752CCDR2G*				4 V	2500 / Tape & Reel
NCV51752CDDR2G				5 V	2500 / Tape & Reel
NCV51752DADR2G*		SOIC−8 NB (Pb−Free)	17 V	2 V	2500 / Tape & Reel
NCV51752DBDR2G*				3 V	2500 / Tape & Reel
NCV51752DCDR2G*				4 V	2500 / Tape & Reel
NCV51752DDDR2G*				5 V	2500 / Tape & Reel

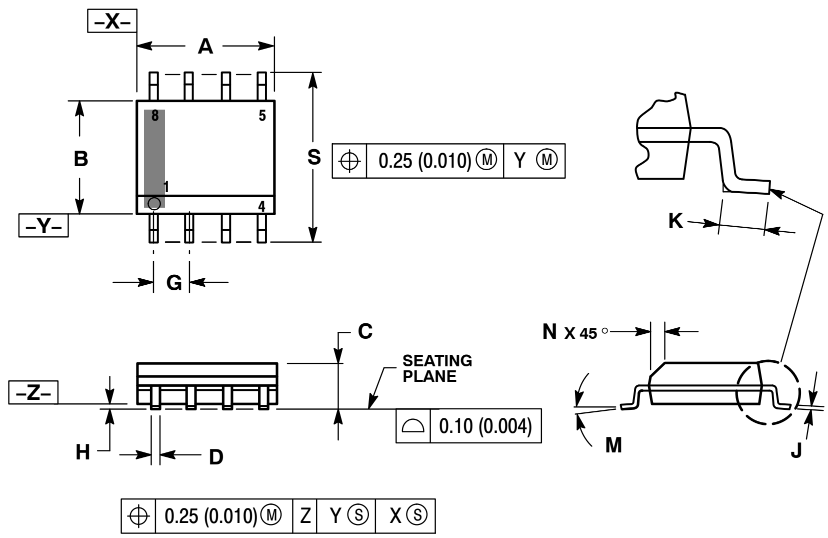
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*Option on demand



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

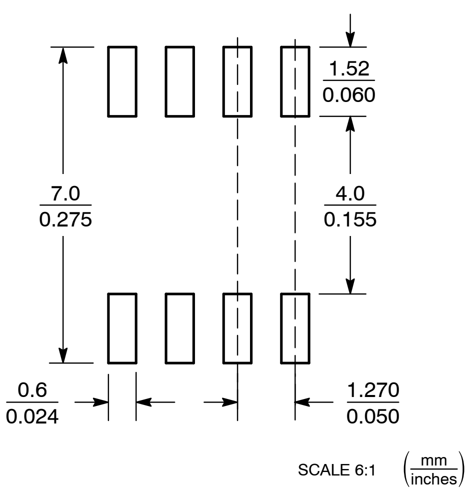
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

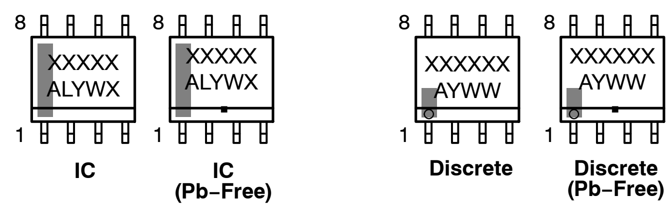
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOIC−8 NB	PAGE 1 OF 2

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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