STISO620

Datasheet

Dual channel digital isolator

SO8N

Product status link

STISO620

Product label

SUSTAINABLE TECHNOLOGY

Features

- Dual channel digital isolator with 2 – 0 channel directionality
- High data rate up to 100 Mbps
- Wide T_{amb} range operation:- 40ºC to 125ºC
- High common-mode transient: >50k V/µs
- From 3 V to 5.5 V supply levels
- 3.3 V and 5 V level translation
- Low power consumption
- Pulse width distortions < 3ns
- 4.8k V galvanic isolation in SO8N package
- Available in 8-pin SOIC narrow-body
- Safety and regulatory approvals
  - UL1577 certified, file number: E362869
  - V_{IORM} (Maximum repetitive isolation voltage) 1.2k V_{PEAK}
  - V_{IOTM} (Maximum transient isolation voltage) 4k V_{PEAK}
  - V_{IOSM} (Maximum surge isolation voltage) 5.2k V_{PEAK}
  - V_{ISO} (Isolation withstand voltage) 2.8k V_{RMS}

Application

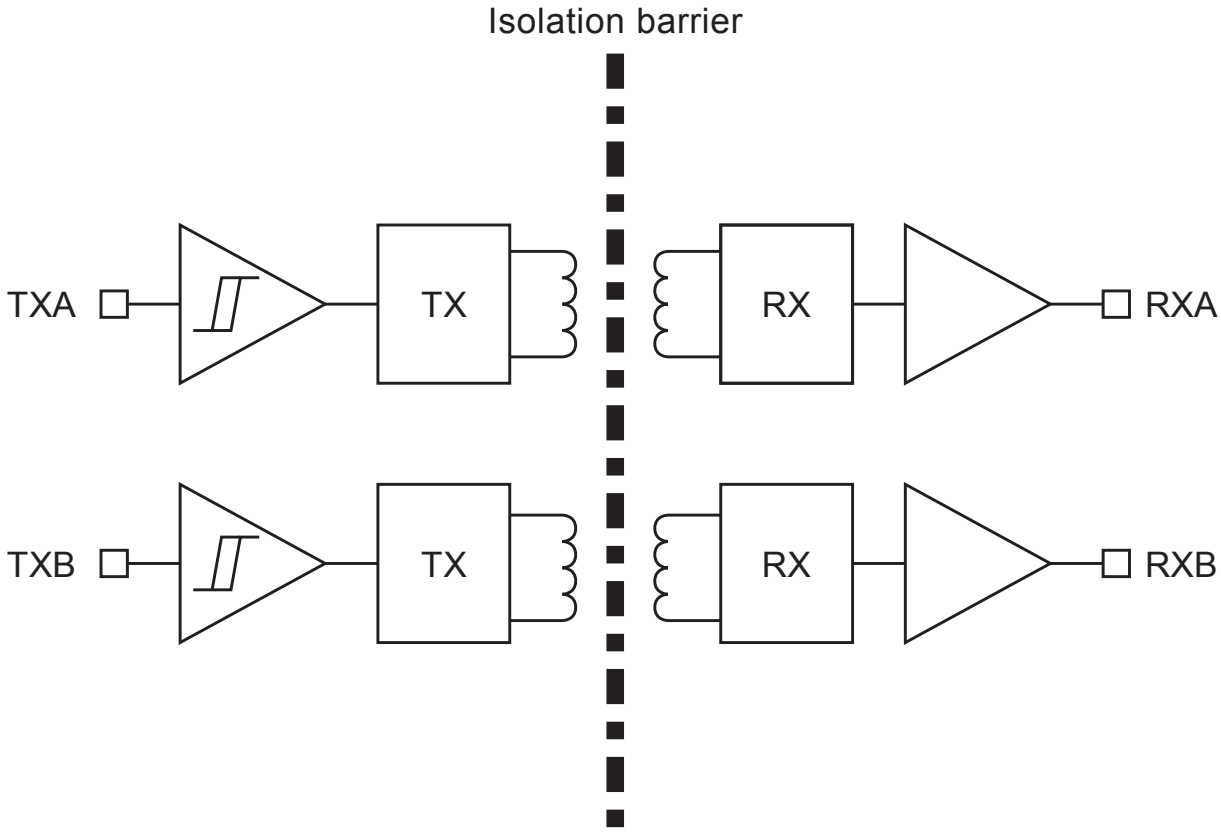
- Optocoupler replacement in industrial application
- Industrial field bus isolation
- Battery monitor and motor drive
- Size-critical multichannel isolation

Description

The STISO620 is a dual-channel digital isolator based on the ST thick oxide galvanic isolation technology. The device provides two independent channels in the same direction with Schmitt trigger input, providing robustness to noise and high speed input/output switching time.

1 Block diagram

Figure 1. **Block diagram**



2 Electrical data

2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Test Condition	Value	Unit
V_{DDX}	Supply voltage (each side)		-0.3 to 5.5	V
V_{IN}	Logic input voltage		-0.3 to 5.5	V
I_O	Output current		5	mA
T_j	Junction temperature		-40 to 150	°C
T_{stg}	Storage temperature		-50 to 150	°C

2.2 Electrical sensitivity

Table 2. ESD protection ratings

Symbol	Parameter	Test Condition	Class	Value	Unit
HBM	Human Body Model	Conforming to ANSI/ESDA/JEDEC JS-001-2014		+/- 2	kV
CDM	Charge Device Model	All pins Conforming to ANSI/ESDA/JEDEC JS-002-2014		+/- 1000	V
MM	Machine Model	Conforming to EIA/JESD22-A115-C		+/- 200	V

2.3 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DDX}	Supply voltage (each side)		3		5.5	V
V_{IN}	Logic input voltage		0		5	V
T_{amb}	Ambient temperature		-40		125	°C

2.4 Electrical characteristics

Table 4. Electrical characteristics at VDD1 = VDD2 = 3 V and 5V

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DDXon}	V_{DDX} on threshold	V_{DDX} rising from 2 V to 3 V			2.75	V
$V_{DDXhyst}$	V_{DDX} off hysteresis	V_{DDX} falling from 5 V			0.2	V
V_{IHL}	Low level Schmitt trigger threshold	Logic input falling Full supply range	0.8			V
V_{ILH}	High level Schmitt trigger threshold	Logic input rising Full supply range			2	V
V_{OL}	Low level output voltage	I_{OH} = 4 mA			0.35	V
V_{OH}	High level output voltage	I_{OL} = 4 mA	V_{DDX} – 0.35			V
Z_O	Output impedance	T_{amb} = 25 °C V_{DD2} = 3.3 V	40	50	60	Ω
$f_{IN,MAX}$	Maximum data rate	V_{IH} = 5 V	100			Mbps
t_r	Output rise time	C_L = 20 pF T_{amb} = 25 °C See Figure 3		2		ns
t_f	Output fall time	C_L = 20 pF T_{amb} = 25 °C See Figure 3		2		ns
t_{DHL}	Propagation delay H to L	Tamb = 25°C See Figure 3		25		ns
		Full temperature range			42	
t_{DLH}	Propagation delay L to H	Tamb = 25°C See Figure 3		25		ns
		Full temperature range			42	
t_{POWUP}	Power up time				30	µs
$t_{REFRESH}$	Refresh time(1)			1	2	µs
t_{WD}	Watchdog timeout		2		8	µs
PWD	Pulse width distortion $\lvert t_{DHL} - t_{DLH} \rvert$	Tamb = 25°C		1.7	2.6	ns
		Full temperature range			3	
CMTI	Common mode transient immunity	(2)	50	65		kV/µs

1. *A refresh function ensures the persistence of the transmitted data across the isolation. The state of TX is periodically transmitted every $t_{REFRESH}$*
2. *Not tested in production. Limit is guaranteed by characterization on a limited number of samples and simulations.*

Note: ***Testing conditions: Typical values are defined at Tamb = 25°C, VDD1 = VDD2 = 3 V and 5V, minimum and maximum limits applies to the full temperature range (Tested in production at T_{amb} = 25°C and the limits in the full temperature range are guaranteed by characterization on a limited quantity of samples), unless otherwise specified.***

Table 5. Supply current at VDD1 = VDD2 = 2.75 V

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{DD1}	Supply current (TX side)	DC		0.66	0.72	mA
		10 Mbps, 50 % duty cycle, C_L = 20 pF, VDD1 = 2.75 V		1.6	3	
		100 Mbps, 50 % duty cycle, C_L = 20 pF, VDD1 = 2.75 V		13	16	
I_{DD2}	Supply current (RX side)	DC		2.6	2.8	mA
		10 Mbps, 50 % duty cycle, C_L = 20 pF, VDD2 = 2.75 V		3.4	4.5	
		100 Mbps, 50 % duty cycle, C_L = 20 pF, VDD2 = 2.75 V		13	15	

Table 6. Supply current at VDD1 = VDD2 = 5 V

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{DD1}	Supply current (TX side)	DC		0.66	0.72	mA
		10 Mbps, 50 % duty cycle, C_L = 20 pF, VDD1 = 5 V		1.7	4	
		100 Mbps, 50 % duty cycle, C_L = 20 pF, VDD1 = 5 V		13	18	
I_{DD2}	Supply current (RX side)	DC		2.6	2.8	mA
		10 Mbps, 50 % duty cycle, C_L = 20 pF, VDD2 = 5 V		4.3	7	
		100 Mbps, 50 % duty cycle, C_L = 20 pF, VDD2 = 5 V		20	25	

3 Thermal data

Table 7. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{th\ j\text{-}\ amb}$	Thermal resistance, junction to ambient (1)	97(2)	°C/W
$R_{th\ jc\text{-}\ top}$	Thermal resistance, junction to top case (3)	47	°C/W

1. *As per JESD51-7*
2. *Maximum power dissipation = 670mW (@T_{amb} = 85°C, T_J < 150°C)*
3. *As per JESD51-3*

4 Isolation characteristics

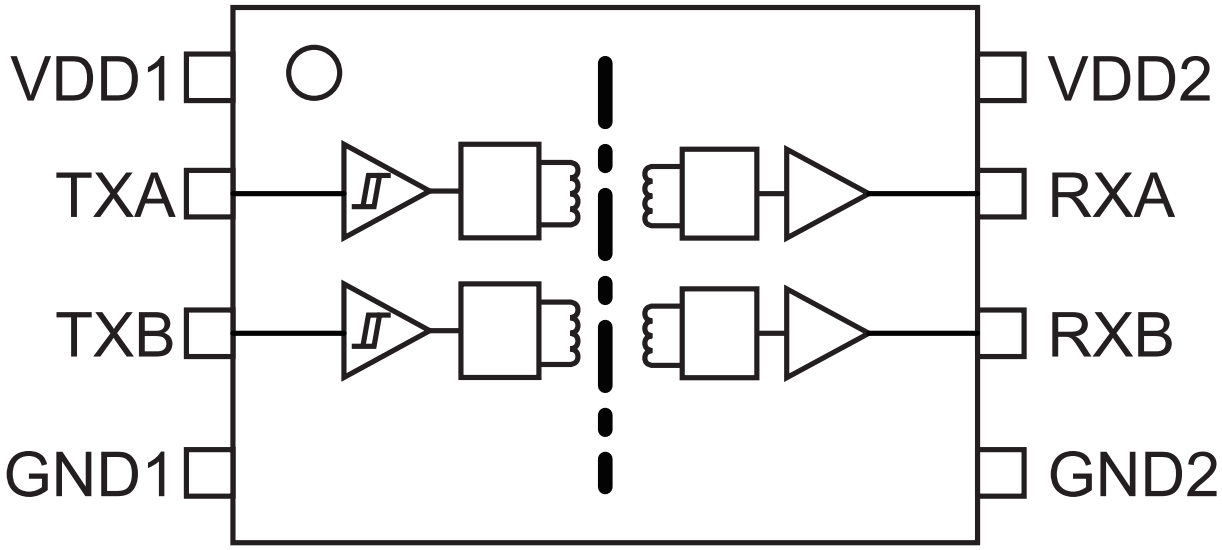
Table 8. Isolation and safety specification

Symbol	Parameter	Test conditions	Value	Unit
General				
CLR	Clearance (minimum external air gap)	Measured from input terminals to output terminals, shortest distance trough air	4	mm
CPG	Creepage (minimum external tracking)	Measured from input terminals to output terminals, shortest distance path along body	4	mm
CTI	Comparative tracking index (tracking resistance)	IEC 60112	≥ 400	V
-	Material group	According to IEC 60664-1	II	-
-	Overvoltage category per IEC 60664-1	Rated mains voltages ≤ 150 V_{RMS}	I - IV	-
		Rated mains voltages ≤ 300 V_{RMS}	I - III	-
		Rated mains voltages ≤ 600 V_{RMS}	I - II	-
		Rated mains voltages ≤ 1000 V_{RMS}	I	-
DIN EN IEC 60747-17 (VDE 0884-17)				
V_{IORM}	Maximum repetitive isolation voltage	AC voltage	1200	V_{PEAK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave)	849	V_{RMS}
		DC voltage	1200	V_{PEAK}
V_{PR}	Partial discharge test voltage	Method a, type and sample test t_m= 10 s Partial discharge < 5 pC	1920	V_{PEAK}
		Method b1, 100% production test t_m = 1 s Partial discharge < 5 pC	2250	V_{PEAK}
V_{IOTM}	Maximum transient isolation voltage	Method a, type and sample test, t_{ini} = 60 s	4000	V_{PEAK}
$V_{IOTM,test}$	Transient isolation voltage test	Method b1, 100% production test $V_{IOTM,test} = V_{IOTM} \times 1.2$, t_{ini} = 1 s	4800	V_{PEAK}
V_{IMP}	Maximum impulse voltage	Type test; tested in air 1.2/50 µs waveform per IEC 62368-1	4000	V_{PEAK}
V_{IOSM}	Maximum surge isolation voltage	Type test; tested in oil 1.2/50 µs waveform per IEC 62368-1 $V_{IOSM} \geq V_{IMP} \times 1.3$	5200	V_{PEAK}
R_{IO}	Isolation resistance	Type test V_{IO} = 500 V; T_{amb} = 25°C	> 10^{12}	Ω
		Type test V_{IO} = 500 V; $T_{amb,max}$= 125°C	> 10^{11}	
		Type test V_{IO} = 500 V; $T_{amb} = T_S$ = 150°C	> 10^{9}	
Parameter definitions and test conditions in accordance to IEC 60747-17				

Symbol	Parameter	Test conditions	Value	Unit
UL 1577				
V_{ISO}	Isolation withstand voltage	60 s; type test	2828 / 4000	V_{RMS}/V_{PEAK}
$V_{ISO,test}$	Isolation voltage test	1 s; 100% production	3394 / 4800	V_{RMS}/V_{PEAK}
Recognized under the UL 1577 component recognition program. File number E362869				

5 Pin connection

Figure 2. **Pin connection (top view)**



6 Pin list

Table 9. **Pin description**

N.	Name	Type	Function
1	VDD1	Supply	Supply voltage side 1
2	TXA	Logic input	Transmit data channel A
3	TXB	Logic input	Transmit data channel B
4	GND1	Ground	Ground side 1
5	GND2	Ground	Ground side 2
6	RXB	Logic output	Receive data channel B
7	RXA	Logic output	Receive data channel A
8	VDD2	Supply	Supply voltage side 2

7 Device description

The STISO620 is a dual high-speed isolated communication channel. It integrates two channels in the same direction and provides low levels of pulse width distortion in the full operation range.

7.1 Device operation

The device operation is described in the following table:

Table 10. Device operation table

VDD1	VDD2	Tx	Rx
Above UVLO	Above UVLO	H	H
		L	L
Below UVLO	Above UVLO	X	L(1)
Above UVLO	Below UVLO	X	Tri-state
Below UVLO	Below UVLO	X	Tri-state

1. *Safe state imposed by default after the watchdog timeout.*

When both sides of the device are powered (above UVLO threshold), the device operates as an isolated buffer between the Tx input, and the respective Rx output (see Figure 3). In this figure t_W is the minimum pulse width of the TX pulse, so that the internal logic circuitry doesn't filter the pulse itself. According to the $f_{IN,MAX}$ in Table 4, this value is $t_{W,min} \geq 10ns$.

Figure 3. Timing diagram

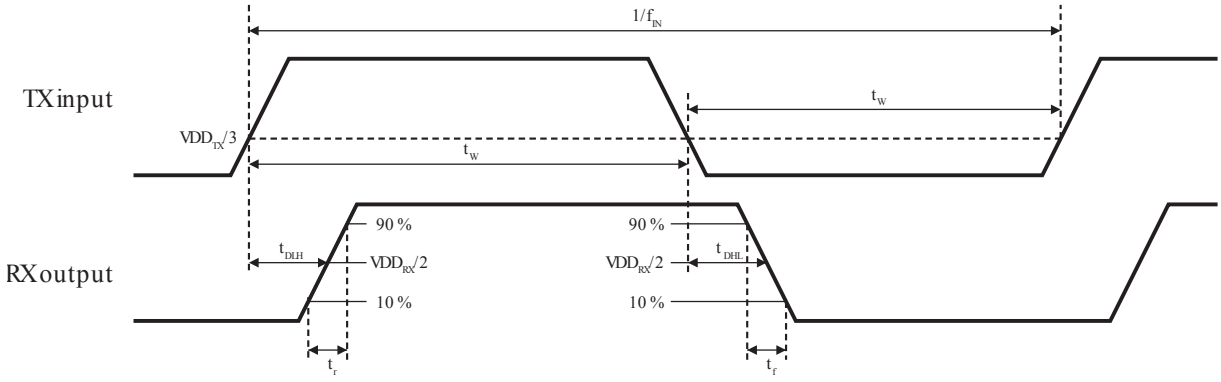
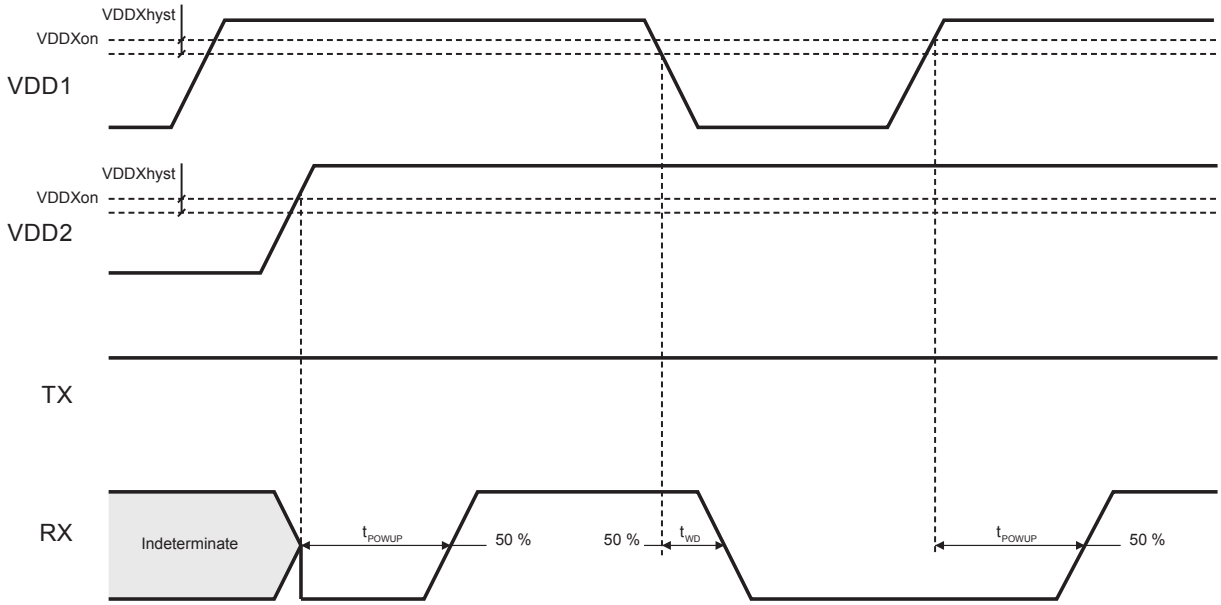


Figure 4. Timing diagram – power-up and power-down

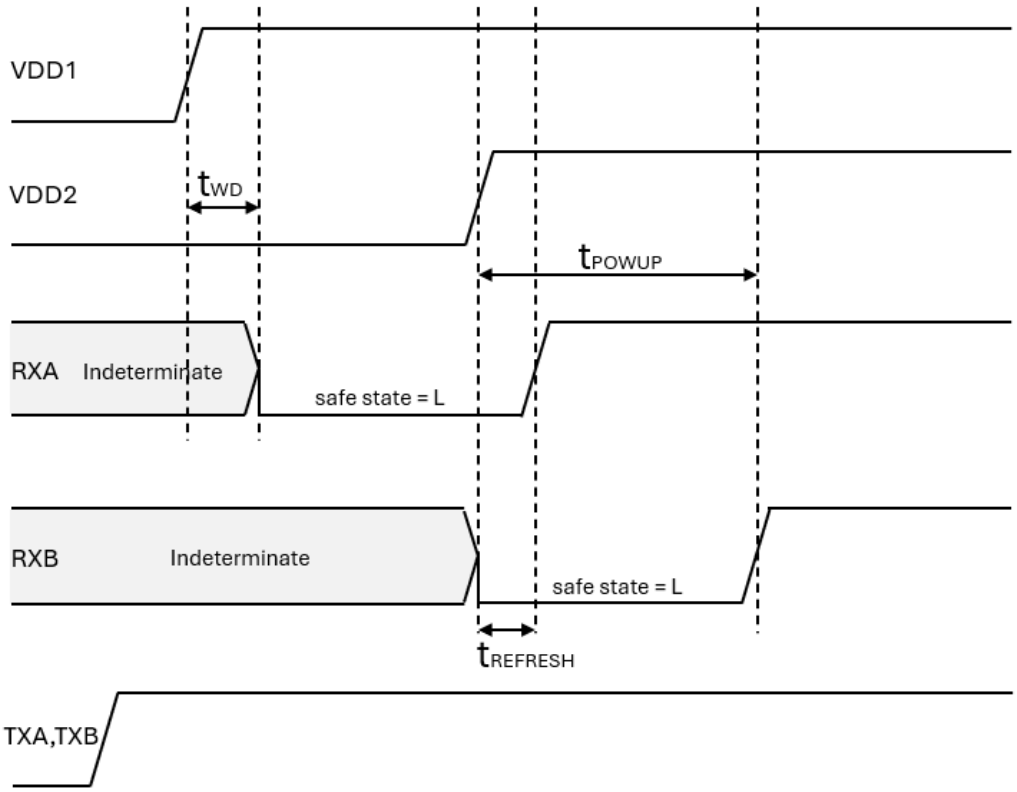


In Figure 4 t_{POWUP} is the power-up time after that the device is operative as reported in Table 10 when VDD1 and VDD2 are both above the UVLO (normal operation) .

7.2 Watchdog and safe state

A watchdog function is present to set the output in a safe state if no data are received from one side to another for a time longer than t_{WD}. A typical application of this function is at the start-up of STISO620. If the supply of one side rises slower than the other one, the output of the faster side is set to the safe state until the other side is in off state. A logic level low is forced as safe state: see Figure 5. Another condition is when the supply of one side is suddenly missing.

Figure 5. Watchdog



8 Characterization graphs

Following data are based on characterization tests on a limited number of samples.

Figure 6. tr/tf thermal drift normalized at 25°C

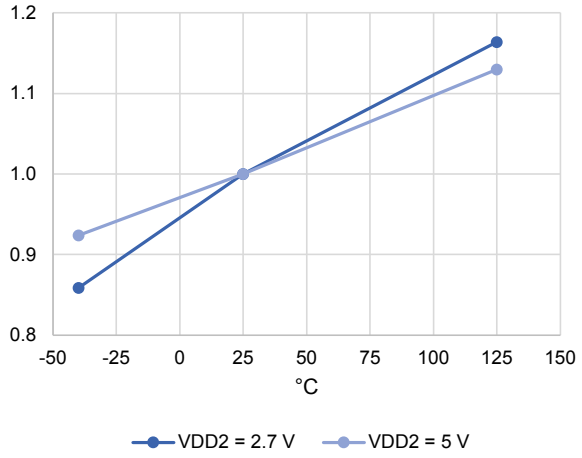
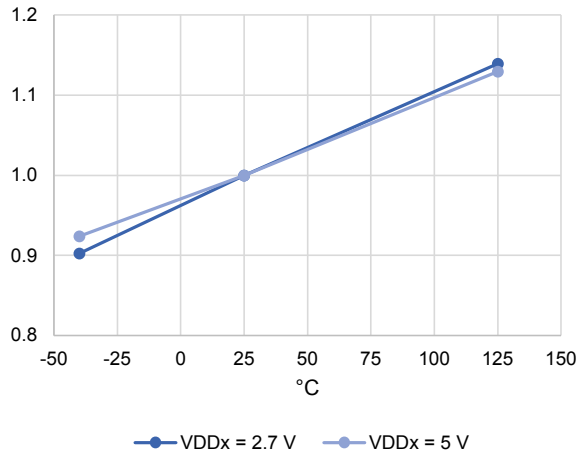


Figure 7. Propagation delay thermal drift normalized at 25°C



9 Package mechanical data

Table 11. **SO8 narrow package dimensions**

Symbol	Min.	Nom.	Max.
A	1.35		1.75
A1	0.10		0.25
b	0.35		0.49
c	0.19		0.25
D	4.80		5.00
e		1.27BSC	
E1	3.80		4.00
E	5.80		6.20
L	0.40		1.25
h	0.25		0.50
θ	0°		7°
Θ1	2°		12*
aaa		0.25	
bbb		0.25	
ccc		0.10	

Figure 8. **SO8 package drawings**

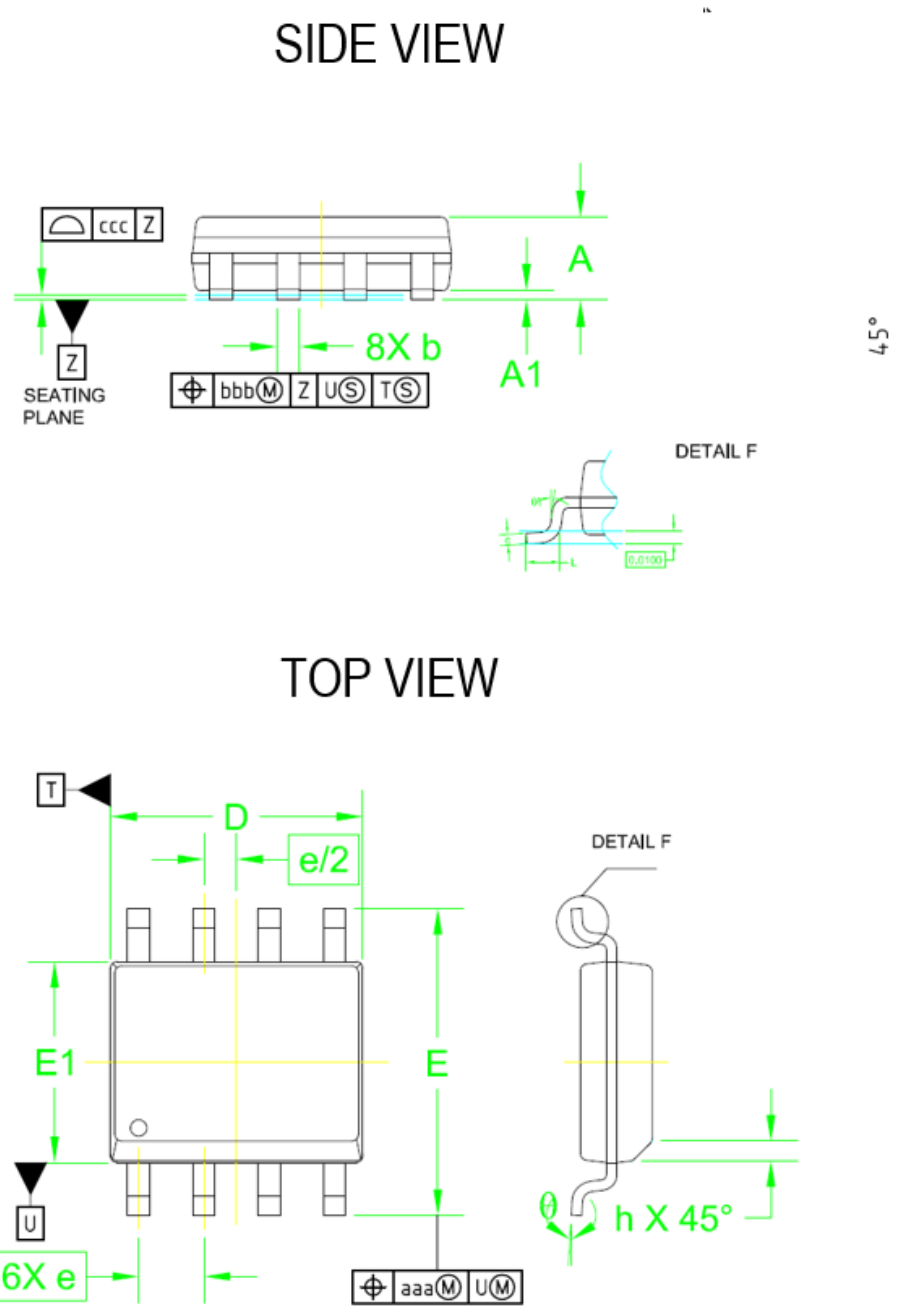
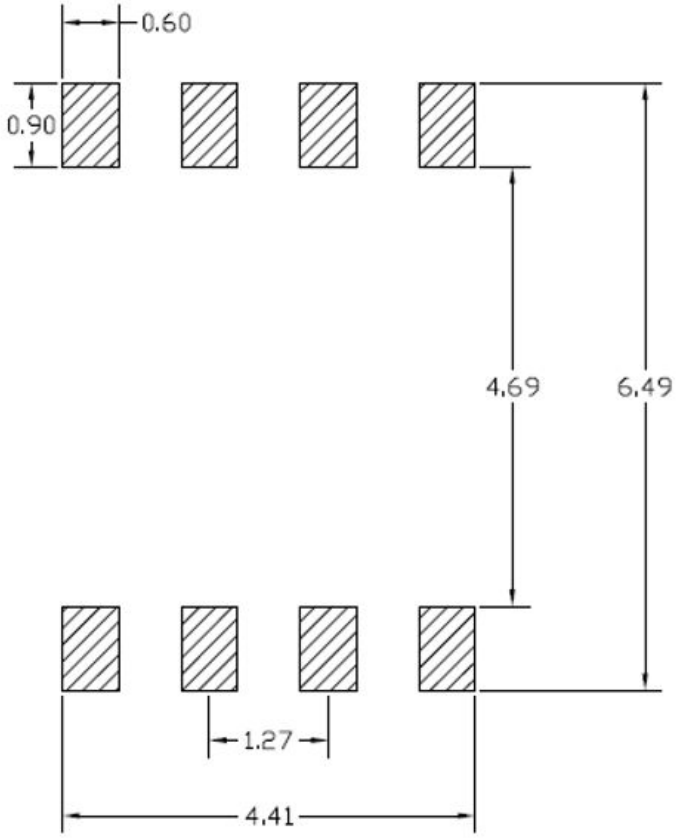


Figure 9. **SO8 package recommended footprint**



10 Order Information

Table 12. **Order Information**

Order Code	Package	Packing
STISO620	S08 narrow body	Tray
STISO620TR	S08 narrow body	Tape and Reel

Revision history

Table 13. **Document revision history**

Date	Version	Changes
07-Nov-2022	1	Initial release.
09-Jan-2023	2	RXA and RXB pin order corrected in Table 9
13-Jan-2025	3	Front page, features section: changed order list and added isolation parameters tested in accordance with IEC 60747-17; reorganized Table 4 in Table 4, Table 5 and Table 6; in Table 4 added a footnote regarding $t_{REFRESH}$ parameter. Added Table 7 with package thermal data. Table 5 and Table 6 in Rev 2 replaced by Table 8. In section 7.1 added a description of parameters t_W in Figure 3 and t_{POWUP} in Figure 4. Added Section 7.2 with Figure 5. Formatting changes for Table 9, Table 10, Table 11, Table 12.

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