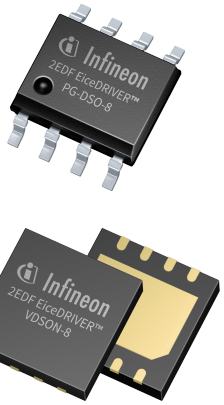
EiceDRIVER™ 2EDF5215F, 2EDF5215G

250 V, 5 A/9 A high-side and low-side gate driver ICs

EiceDRIVER™ 2EDF5215F and 2EDF5215G are designed to drive low-side and high-side MOSFETs. A strong output stage, together with a low part-to-part skew and fast signal propagation makes these products ideal for use in fast-switching power systems. The inputs are independently controlled and can overlap enabling the use in synchronous rectifiers and full-bridge with diagonal driving scheme. The outputs are matched with a maximum 4 ns propagation delay enabling the use of lower dead-time in half-bridge and perfect synchronization in diagonal driving.

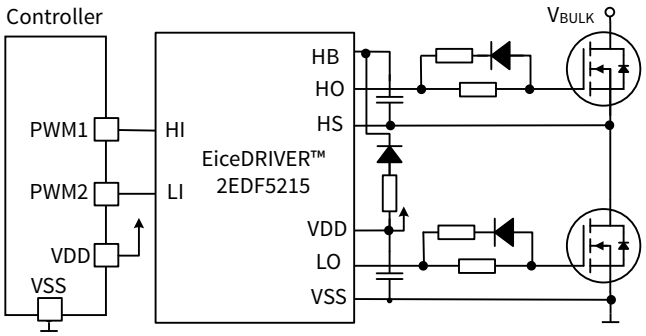
Features

- 250 V high and low-side gate driver
- -250 V negative HS transient immunity due to galvanic isolation
- 100 V/ns dV/dt robustness due to CT technology
- 5 A / 9 A source / sink capability
- +9 ns /-5 ns delay accuracy
- 4 ns maximum delay matching
- 1.2 V output clamping threshold in UVLO condition
- <2 µs fast start-up time in bootstrap operation
- Available in DSO-8 (5 mm x 6 mm) and VDSON-8 (4 mm x 4 mm)



Product validation

Fully qualified for industrial grade applications.



Potential topologies

- Half-bridge/Full-bridge
- Full-bridge with diagonal driving scheme
- Two switch and active clamp forward converter

Potential applications

- Server and telecom DC-DC converter
- Synchronous rectification for SMPS
- Motor drives and power tools
- Low-speed electric vehicles (LSEV)
- Solar optimizers and micro-inverters

Table 1 EiceDRIVER™ 2EDF5215x product family portfolio

Part number	Source/sink current	UVLO ON/OFF	HS voltage capability	DV/DT robustness	Package
2EDF5215F	5 A/9 A	7/6.4 V	± 250 V	100 V/ns	PG-DSO-8
2EDF5215G	5 A/9 A	7/6.4 V	± 250 V	100 V/ns	VDSON-8

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1 Pin configuration and description

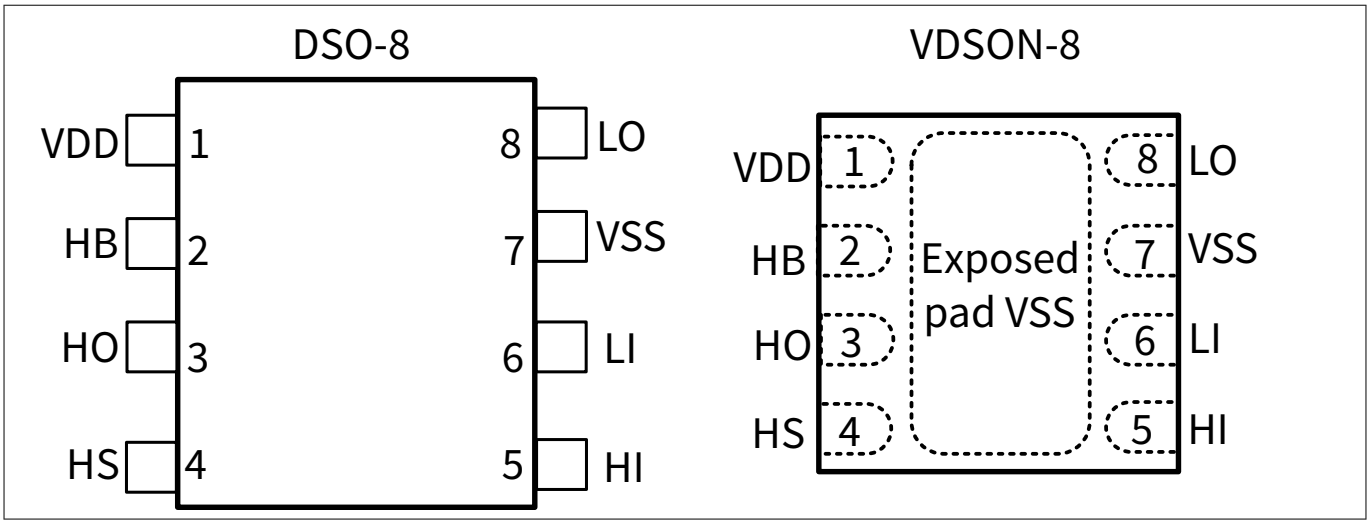


Figure 1 **Pin configuration for PG-DSO-8 and VDSON-8 (top side transparent view)**

Table 2 **Pin description for PG-DSO-8 and VDSON-8**

Pin #	Symbol	Description
1	VDD	Supply voltage for low-side channel
2	HB	Supply voltage for high-side channel (external bootstrap diode is required)
3	HO	Output for high-side channel
4	HS	Ground return path for high-side channel (switching node)
5	HI	Input (non-inverting) for high-side channel
6	LI	Input (non-inverting) for low-side channel
7	VSS	Ground return path for low-side channel (microcontroller ground)
8	LO	Output for low-side channel

For package drawing details see Chapter 7.

2 Functional description

2.1 Block diagram

A simplified functional block diagram for EiceDRIVER™ 2EDF5215x is given in Figure 2.

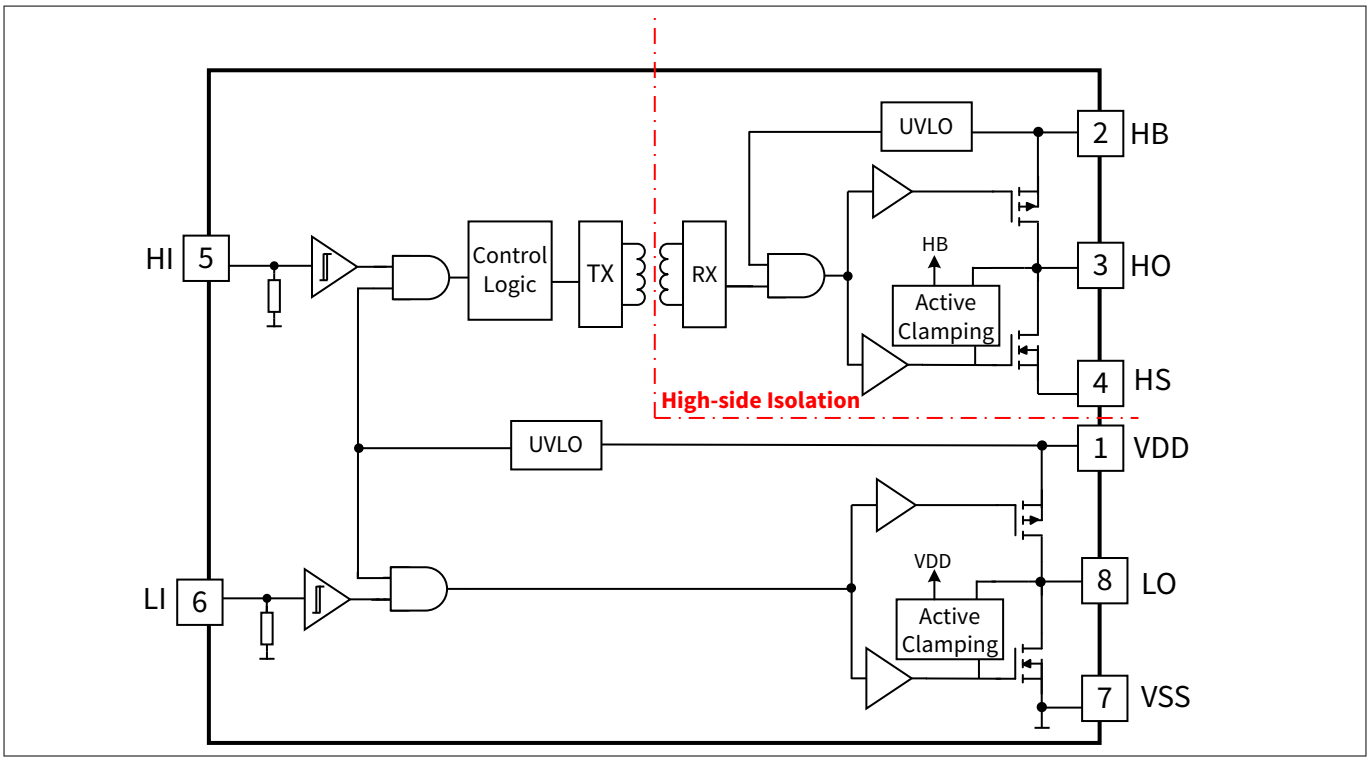


Figure 2 Block diagram

2.2 Introduction

EiceDRIVER™ 2EDF5215 is a high-speed gate driver intended to drive low-side and high-side MOSFETs.

2EDF5215 exploits magnetic isolation, instead of common level-shifter technology, to generate the high-side floating domain. Infineon Coreless Transformer (CT) technology enables robust high-side isolation and reliable operation in case of significant over/under-shoots (+- 250 V) on the switching node during normal operation. Additionally, it enables switching node transitions up to to 100 V/ns with no failures or input distortion because of industry benchmark common-mode transient immunity (CMTI).

EiceDRIVER™ 2EDF5215 features two independent channels without interlock to enable usage in synchronous rectifiers or full-bridge with diagonal driving scheme. A low propagation delay matching and propagation delay accuracy ensures perfect timing synchronization of the gate signals (e.g. in diagonal driving) and dead-time optimization with benefit on system reliability and efficiency performance.

With accurate timings and strong output stage, enabling MOSFET paralleling, the EiceDRIVER™ 2EDF5215 is best suited for use in high-switching high-power applications.

2.3 CT communication and high-side data transmission

A coreless transformer (CT) based communication module is used to transfer the PWM signal transfer between controller and high-side channel. A proven high-resolution pulse repetition scheme in the transmitter side combined with a watchdog timeout at the receiver side enables recovery from communication fails and ensures safe system shut-down in failure cases.

EiceDRIVER™ 2EDF5215 exploits a double coil on-chip transformer to mitigate the effect of outer fields. Opposite current flow in the two coils enables field compensation and thus high robustness against Magnetic Field Interference (MFI). The double coil transformer also ensures high CMTI. Any fast transient induced current is

terminated into the double coil´s mid node (CT_GND) that is connected to ground whilst the receiver only detects the differential signal.

2.4 Supply voltages

Low-side and high-side channels are powered via two independent supply voltages, V_{DD} and V_{HB}. The minimum supply voltage is set by the Undervoltage Lockout (UVLO) function.

Two ceramic bypass capacitors must be placed between VDD and VSS and between HB and HS in close proximity to the device. A minimum capacitance of 20 x C_{iss} (MOSFET input capacitance) is recommended to ensure an acceptable ripple (5% of V_{DDO}) on the supply pin.

Both the low-side channel and input logic are supplied from VDD leading to the higher VDD versus HB current. The input logic contribution is linked to the conversion of the input signal (HI) into a train of repetitive current pulses to drive the coreless transformer. Due to the chosen robust encoding scheme, the average repetition rate of these pulses and thus the average supply current depends on the switching frequency, f_{sw}. However this effect is rather small as can be seen in Figure 13.

2.5 Undervoltage Lockout (UVLO)

Both the high-side and low-side channels feature Undervoltage Lockout (UVLO) function, which ensures that the outputs can be switched to their high level only if the respective supply voltage exceeds the UVLO threshold voltage. Thus it can be guaranteed that the power switch is not operated if the driving voltage is too low to achieve a complete and fast transition to the "on" state, ensuring operation in Safe Operating Area (SOA).

The UVLO function also guarantees that the power switch is operated above the thermal inversion point reducing the risk of thermal runaway for example in case of paralleled MOSFETs.

The UVLO level for both channels is set to a typical value of 7 V (with hysteresis). In bootstrap operation this value guarantees enough margin from UVLO shutdown in a worst-case scenario (for example 47 nF small bootstrap capacitor with 10 V gate-to-source driving, see Chapter 6.2). At the same time it guarantees good margin from typical thermal inversion point of the MOSFETs.

2.5.1 UVLO times - Driver start-up and activation

When the supply approaches the UVLO in a falling or rising event, the driver output reacts with certain delay described by the parameters t_{START} and t_{STOP}.

In bootstrap operation the high-side activation and deactivation are given by $t_{START,HB}$ (case A) and $t_{STOP,HB}$ (case A´) respectively (see Figure 3). In operation with independent supplies (See Figure 4), the rising and falling of V_{DD} and V_{HB} may be not synchronized. If V_{DD} is not available (< $UVLO_{VDD,on}$), the input logic is not supplied and the PWM cannot be transferred to the high-side channel via CT communication; thus the high-side output is not generated even in case of HB UVLO already released (V_{HB}>$UVLO_{HB,on}$). In this case the high-side output will react only after a time $t_{START,HB}$ + Δ + 3.5 us (case B). If the VDD is ramping down while the HB UVLO is inactive (V_{HB}>$UVLO_{HB,on}$), the high-side output will react only after 800 ns (case B´) once the VDD reached 2.7 V.

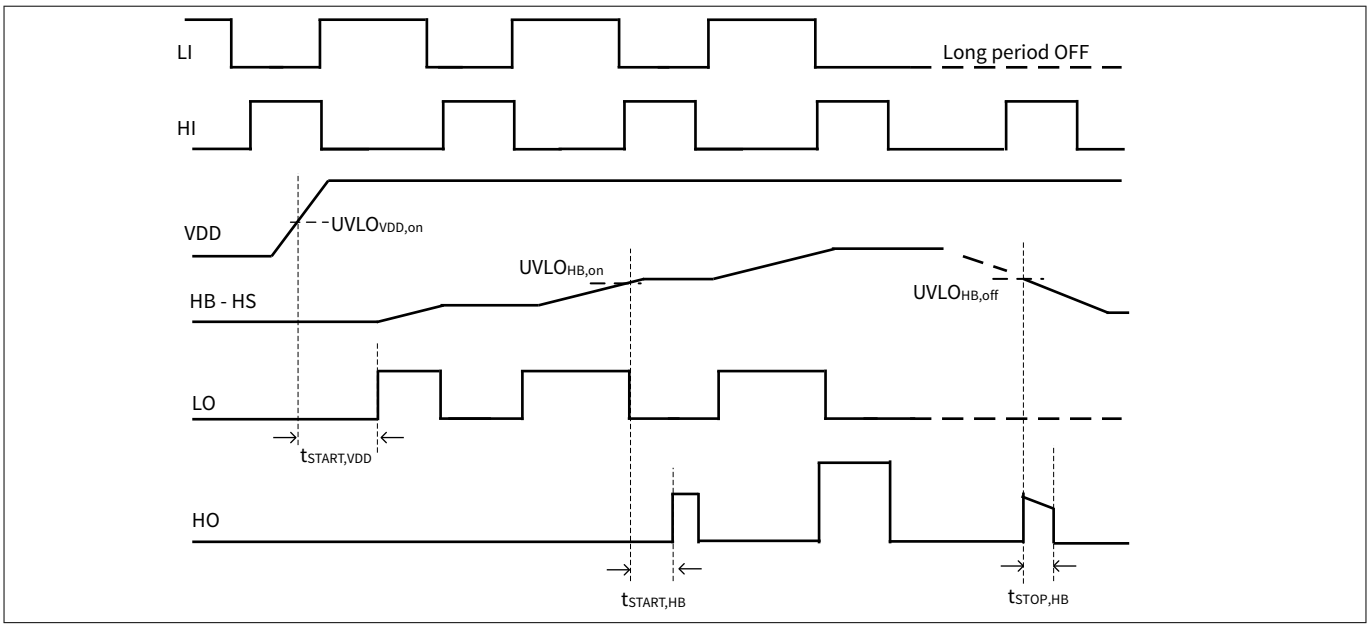


Figure 3 **UVLO start-up behavior in bootstrap operation**

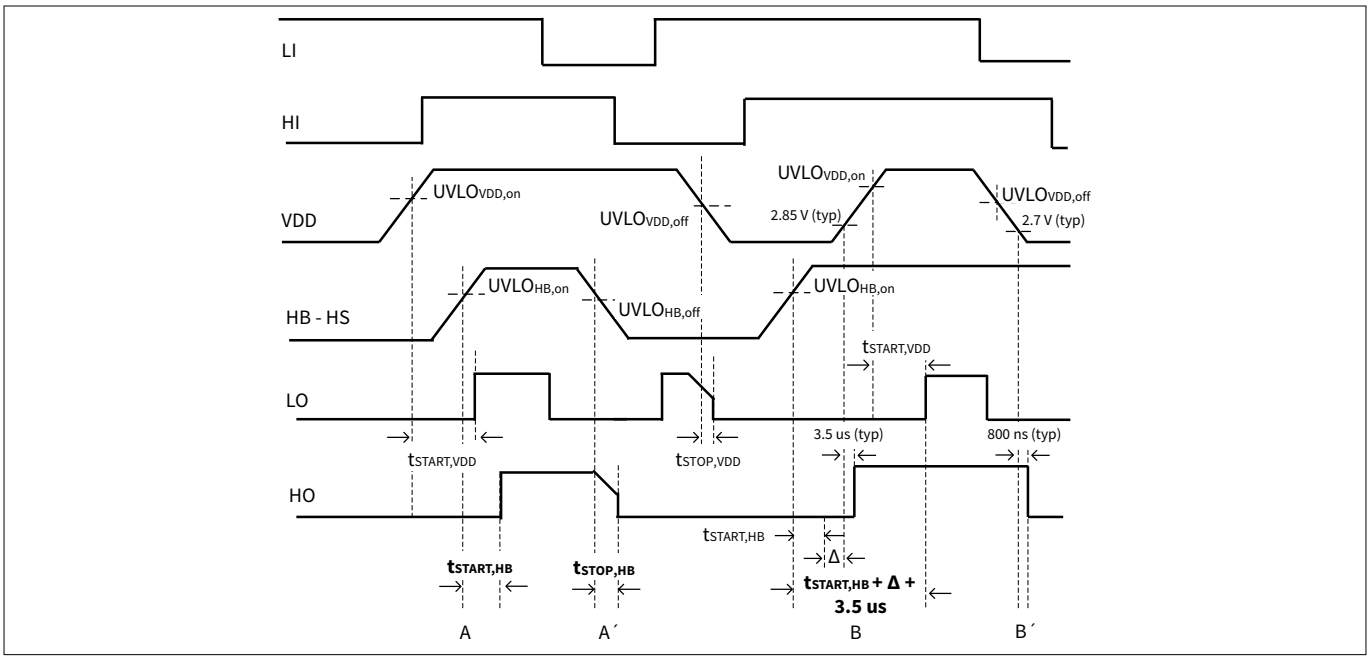


Figure 4 **UVLO start-up behavior in operation with independent VDD and HB supplies (example with synchronous rectification)**

2.6 Input stage and logic table

The inputs HI and LI control two independent PWM channels. The input signal is transferred non-inverted to the corresponding gate driver outputs HO and LO. The inputs are compatible with low voltage TTL threshold levels and provide a hysteresis of typically 0.8 V. The hysteresis is independent of the supply voltage V_{DD}.

The PWM inputs are internally pulled down to a logic low voltage level (V_{SS}). In case the microcontroller signals have an undefined state during the power-up sequence, the gate driver outputs are forced to the off-state (low). Table 3 shows the LI, HI driver logic in case of sufficiently high supply voltage.

Table 3 also shows the functionality in case of insufficient supplies; the outputs of the driver are actively held low by the undervoltage lockout (UVLO) and active output clamping functionalities (see Chapter 2.8).

Table 3 Logic table

Inputs		Supplies	Outputs		Note
HI	**LI**	**V_{DD}, V_{HB}**	**LO**	**HO**	
L	L	> $UVLO_{VDDx,HB,on}$ (active)	L	L	–
L	H		L	H	–
H	L		H	L	–
H	H		H	H	–
Left open	Left open		L	L	Input pins internally pulled down via driven output-side nMOS
x	x	1.2 V < V_{HB} < $UVLO_{HB,on}$	x	L	HO noise is pulled down in few tens of ns via active clamping (see Chapter 2.8)
x	x	1.2 V < V_{DD} < $UVLO_{VDD,on}$	L	x	LO noise is pulled down in few tens of ns via active clamping (see Chapter 2.8)

2.7 Driver outputs

The rail-to-rail output stage realized with complementary MOS transistors is able to provide a typical 5 A sourcing and 9 A sinking peak current for a 12 V supply. The low on-resistance coming together with high driving current is particularly beneficial for fast switching of very large MOSFETs. With a R_{on} of ~ 1.2 Ω for the sourcing pMOS and 0.6 Ω for the sinking nMOS transistor, the driver can, in most applications, be considered as a nearly ideal switch. The p-channel sourcing transistor enables real rail-to-rail behavior without suffering from the voltage drop unavoidably associated with nMOS source follower stages.

In case of floating inputs or insufficient supply voltage not exceeding the UVLO thresholds, the driver outputs are actively clamped to the "low" level (VSS, VHS) as mentioned in Table 3.

2.8 Fast active output clamping under UVLO conditions

The Undervoltage Lockout (UVLO) ensures no driver operation for supplies below the UVLO thresholds. However, this is not sufficient to guarantee that the output of the driver is kept low. Transients or noise in the power stage may pull-up the output node of the driver and the gate voltage causing an unwanted turn-on of the switch; this is particularly critical in system using bootstrapping since, during start-up, the supply of the high-side channel is delayed, while the low-side MOSFETs are already switching. In resonant topologies (as LLC), the half-bridge switching node may be pulled up after the turn-off of the low-side switch. When this is turned on again, the dv/dt induced increase of the high-side gate voltage cannot be clamped by the driver $R_{DSON,sink}$ if the the bootstrap supply is not yet available.

With a fast active clamping circuit in the output stage, EiceDRIVER™ 2EDF5215 ensures safe operation in all UVLO situations. This structure allows fast reaction and effective clamping of the output pins (LO, HO). The exact reaction time depends on the output supply (V_{DD}, V_{HB}) and on the output voltage levels; however, already for very low supply levels (~1 V), the active clamping is able to react in some tens of nanoseconds.

2 Functional description

Undervoltage Lockout together with the Fast Active Output Clamping ensures that the outputs are actively held low in case of insufficient supply voltages.

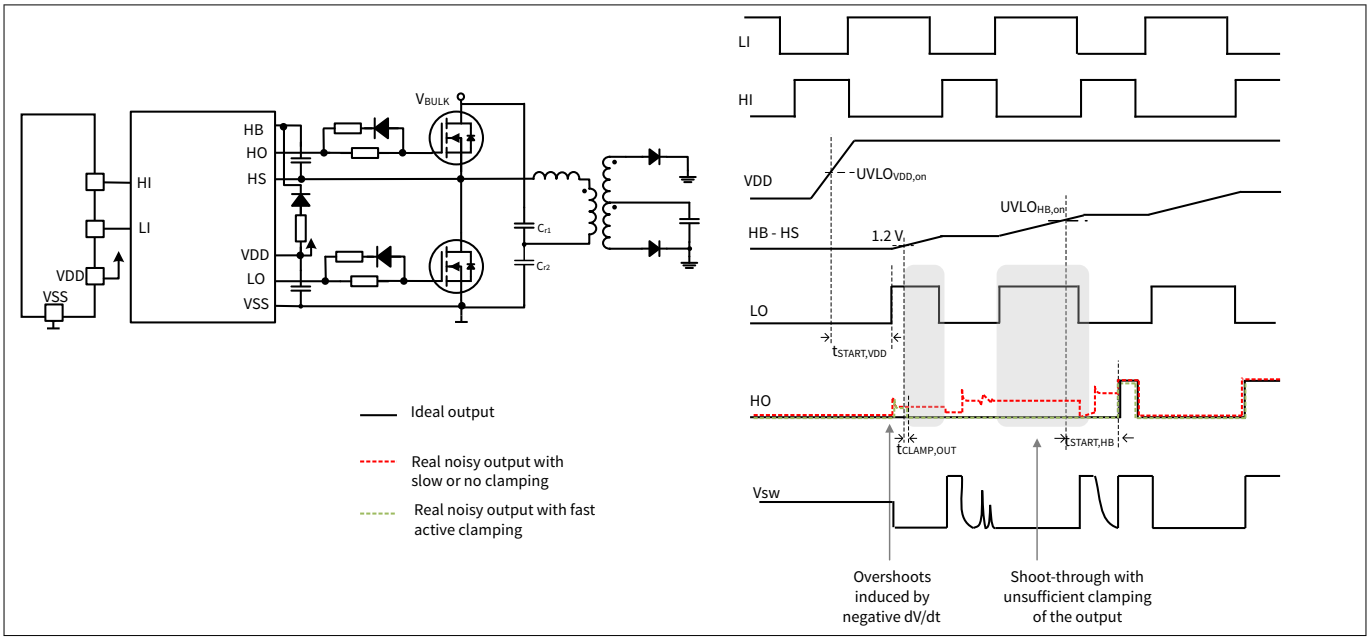


Figure 5 Active output clamping feature

3 Electrical characteristics

3.1 Absolute maximum ratings

Table 4 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Low-side supply voltage	V_{DD}	-0.3	–	18	V	–
High-side supply voltage	V_{HB} - V_{HS}	- 0.3	–	22	V	–
Voltage at pin HS	V_{HS}	-250	–	250	V	–
Voltage at pins HI, LI (DC)	V_{HI}, V_{LI}	-0.3	–	18	V	–
Voltage at pins HI, LI (transient)	V_{HI}, V_{LI}	-5	–	–	V	transient for 50 ns
Voltage at pin LO (DC)	V_{LO}	-0.3	–	V_{DD} + 0.3	V	–
Voltage at pin LO (transient)	V_{LO}	-2	–	V_{DD} + 1.5	V	transient for 200 ns
Voltage at pin HO (DC)	V_{HO}	V_{HS} - 0.3		V_{HB} + 0.3		–
Voltage at pin HO (transient)	V_{HO}	V_{HS} - 2		V_{HB} + 1.5		transient for 200 ns
Reverse source current peak at pins LO, HO	I_{SRC_rev}	-5	–	–	A_{pk}	transient for 500 ns
Reverse sink current peak at pins LO, HO	I_{SNK_rev}	–	–	5	A_{pk}	transient for 500 ns
Junction temperature	T_J	-40	–	150	°C	–
Storage temperature	T_{STG}	-55	–	150	°C	–
Soldering temperature	T_{SOL}	–	–	260	°C	reflow [1]
ESD capability	V_{ESD_CDM}	–	–	1	kV	Charged Device Model (CDM) [2]
ESD capability	V_{ESD_HBM}	–	–	2	kV	Human Body Model (HBM) [3]

1) According to JESD22A111.
2) According to ANSI/ESDA/JEDEC JS-002.
3) According to ANSI/ESDA/JEDEC JS-001 (discharging 100 pF capacitor through 1.5 kΩ resistor).

3.2 Operating range

Table 5 Operating range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Low-side supply voltage	V_{DD}	7.6	–	17	V	Minimum defined by UVLO
High-side supply voltage	V_{HB} - V_{HS}	7.6	–	20	V	–
Voltage at pin HS	V_{HS}	-230	–	230	V	–
Voltage at pins LI, HI	V_{LI}, V_{HI}	-0.3	–	17	V	–
Voltage slew rate on HS that causes output distortion	$CMTI_{HS}$	100	–	–	V/ns	V_{CM} = 1500 V; static or dynamic HI
Junction temperature	T_J	-40	–	150	°C	*1)*
Ambient temperature	T_A	-40	–	125	°C	–

1) Continuous operation above 125°C may reduce lifetime.

3.3 Thermal characteristics

Thermal characteristics are obtained from simulation with 266 mW power applied to the low-side and 200 mW to the high-side channel.

Table 6 Thermal characteristics at TA = 25°C

Parameter	Symbol	Value		Unit	Note or condition
		PG-DSO-8 1)	VDSON-8 2)		
Thermal resistance junction-case (top) 3)	R_{thJC25}	53	48	K/W	package alone
Thermal resistance junction-ambient 4)	R_{thJA25}	103	57	K/W	1)
Thermal resistance junction-board 5)	R_{thJB25}	28	32	K/W	
Characterization parameter junction-top 6)	Ψ_{thJT25}	8	8	K/W	
Characterization parameter junction-board 6)	Ψ_{thJB25}	27	32	K/W	

1) Simulated with an high-K board as specified in JESD51-7 JEDEC-standard: four-layers board with 2-oz inner layers copper planes and with no thermal vias for cooling.

2) Simulated with an high-K board as specified in JESD51-7 JEDEC-standard: four-layers board with 2-oz inner layers copper planes. An array of 12 thermal vias (0.6 mm diameter) on the exposed pad has been considered.

3) Obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

4) Obtained by simulating a JEDEC-standard high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

5) Obtained by simulating a JEDEC-standard high K-board, as specified in JESD51-7, in an environment described in JESD51-8 with a ring cold plate fixture to control the PCB temperature.

6) Estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining Rth, using a procedure described in JESD51-2a (sections 6 and 7).

3.4 Electrical characteristics

Table 7 Power supply

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
IVDD quiescent current	I_{VDDq}	–	2.28	2.5	mA	LO = low (no switching)
IVDD operating current (100 kHz)	I_{VDD_100kHz}	–	2.76	3.20	mA	f_{sw} = 100 kHz, no load
IVDD operating current (500 kHz)	I_{VDD_500kHz}	–	4.27	4.75	mA	f_{sw} = 500 kHz, no load
IVDD operating current (1 MHz)	I_{VDD_1MHz}	–	5.98	6.75	mA	f_{sw} = 1 MHz, no load
IHB quiescent current (low)	$I_{HBq,low}$	–	0.62	0.86	mA	HO = low (no switching)
IHB quiescent current (high)	$I_{HBq,high}$		0.76	1.0	mA	HO = high (no switching)
IHB operating current (100 kHz)	I_{HB_100kHz}	–	0.86	1.25	mA	f_{sw} = 100 kHz, no load
IHB operating current (500 kHz)	I_{HB_500kHz}	–	1.78	1.98	mA	f_{sw} = 500 kHz, no load
IHB operating current (1 MHz)	I_{HB_1MHz}	–	2.95	4.33	mA	f_{sw} = 1 MHz, no load
HB to VSS current	I_{HB}	–	–	500	nA	operation at 250 V, frequency independent

Table 8 Undervoltage Lockout VDD, VHB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn-on threshold VDD	$UVLO_{VDD/HB,on}$	–	7.15	7.8	V	–

(table continues...)

Table 8 (continued) Undervoltage Lockout VDD, VHB

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn-off threshold VDD, VHB	$UVLO_{VDD/HB,off}$	5.9	6.5	–	V	–
UVLO threshold hysteresis VDD, VHB	$UVLO_{VDD/HB,hys}$	0.55	0.65	0.75	V	–

Table 9 Logic inputs LI, HI

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input voltage threshold for transition LH	V_{LIH}, V_{HIH}	–	2.0	2.37	V	–
Input voltage threshold for transition HL	V_{LIL}, V_{HIL}	0.9	1.2	–	V	–
Input voltage threshold hysteresis	V_{LI_hys}, V_{HI_hys}	0.35	0.8	1.2	V	–
High-level input leakage current	I_{LI}, I_{HI}	–	97	135	µA	LI/HI pin tied to $_{VDDI}$
Input pull-down resistor	$R_{IN,PD}$	–	150	–	kΩ	–

Table 10 Static output characteristics for VDSON-8

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High-level (sourcing) output resistance for LO	$R_{on\_SRC\_LO}$	0.7	1.2	2.0	Ω	I_{SNK} = 50 mA
High-level (sourcing) output resistance for HO	$R_{on\_SRC\_HO}$	0.7	1.1	1.8	Ω	I_{SNK} = 50 mA
Peak sourcing output current	I_{SRC_pk}	–	5	–	A	C_{LOAD} = 150 nF [1)]
Low-level (sinking) output resistance for LO	$R_{on\_SNK\_LO}$	0.2	0.55	1.25	Ω	I_{SRC} = 50 mA
Low-level (sinking) output resistance for HO	$R_{on\_SNK\_HO}$	0.2	0.4	0.7	Ω	I_{SRC} = 50 mA
Peak sinking output current	I_{SNK_pk}	–	-9	–	A	C_{LOAD} = 150 nF [1)]

1) Not subject to production test - specified by design / characterization.

Table 11 Static output characteristics for DSO-8

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High-level (sourcing) output resistance for LO	$R_{on\_SRC\_LO}$	0.8	1.4	2.25	Ω	I_{SNK} = 50 mA
High-level (sourcing) output resistance for HO	$R_{on\_SRC\_HO}$	0.8	1.2	1.85	Ω	I_{SNK} = 50 mA
Peak sourcing output current	I_{SRC_pk}	–	5	–	A	C_{LOAD} = 150 nF [1]
Low-level (sinking) output resistance for LO	$R_{on\_SNK\_LO}$	0.2	0.75	1.55	Ω	I_{SRC} = 50 mA
Low-level (sinking) output resistance for HO	$R_{on\_SNK\_HO}$	0.3	0.5	0.8	Ω	I_{SRC} = 50 mA
Peak sinking output current	I_{SNK_pk}	–	-9	–	A	C_{LOAD} = 150 nF [1]

1) Not subject to production test - specified by design / characterization.

Table 12 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
LI/HI to LO/HO turn-on propagation delay	t_{PDon}	33	38	47	ns	See Figure 6
LI/HI to LO/HO turn-off propagation delay	t_{PDoff}	30	36	46	ns	See Figure 6
Part-to-part turn-on propagation delay mismatch	$\Delta t_{PDon,p\text{-}p}$	0	–	6	ns	[1]
Part-to-part turn-off propagation delay mismatch	$\Delta t_{PDoff,p\text{-}p}$	0	–	8	ns	[1]
Channel-to-channel turn-on propagation delay mismatch	$\Delta t_{PDon,Ch\text{-}Ch}$	-4	–	4	ns	See Figure 7 [2]
Channel-to-channel turn-off propagation delay mismatch	$\Delta t_{PDoff,Ch\text{-}Ch}$	-5.5	–	4.5	ns	See Figure 7 [2]
Pulse width distortion	t_{PWD}	-5	2	5.5	ns	See Figure 8 [3]
Channel turn-off to channel turn-on propagation delay mismatch	t_{DTD}	-5	-2	1	ns	See Figure 9 [4] [5]

(table continues...)

Table 12 (continued) Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Rise time	t_{rise}	–	7.5	14	ns	C_{LOAD} = 1.8 nF, see Figure 6 5)
Fall time	t_{fall}	–	6	11	ns	C_{LOAD} = 1.8 nF, see Figure 6 5)
Minimum input pulse width that changes output state	t_{PW}	10	17	25	ns	See Figure 10
Low-side start-up time	$t_{START,VDD}$	–	3.5	5	µs	See Figure 11 5)
Low-side deactivation time	$t_{STOP,VDD}$	500	750	–	ns	See Figure 11 5)
High-side start-up time	$t_{START,HB}$	–	2.5	5	µs	See Figure 11 5)
High-side deactivation time	$t_{STOP,HB}$	500	850	–	ns	See Figure 11 5)
Activation time of output clamping in UVLO condition	$t_{CLAMP,OUT}$	–	20	–	ns	See Figure 5, Figure 12 5)

1) The parameter gives the difference in the propagation delay between different samples switching in the same direction under same conditions, including same ambient temperature; therefore, is an indication of the production spread. The limits given are valid for all channels combination: t_{PD_HO} - t_{PD_HO}, t_{PD_LO} - t_{PD_LO}, t_{PD_HO} - t_{PD_LO}, t_{PD_LO} - t_{PD_HO}
2) The parameter gives the difference in the propagation delay of channel HO and channel LO switching in the same direction in the same sample.
3) The parameter gives the difference between ON and OFF propagation delay in the same channel (HO or LO), in the same sample at same ambient temperature.
4) The parameter gives the difference between the ON propagation delay of one channel and the OFF propagation delay of the other channel, in the same sample at same room temperature.
5) Not subject to production test - verified by design/characterization.

4 Timing diagrams

Figure 6 shows the definition of rise, fall and delay times as observed at the capacitively loaded output.

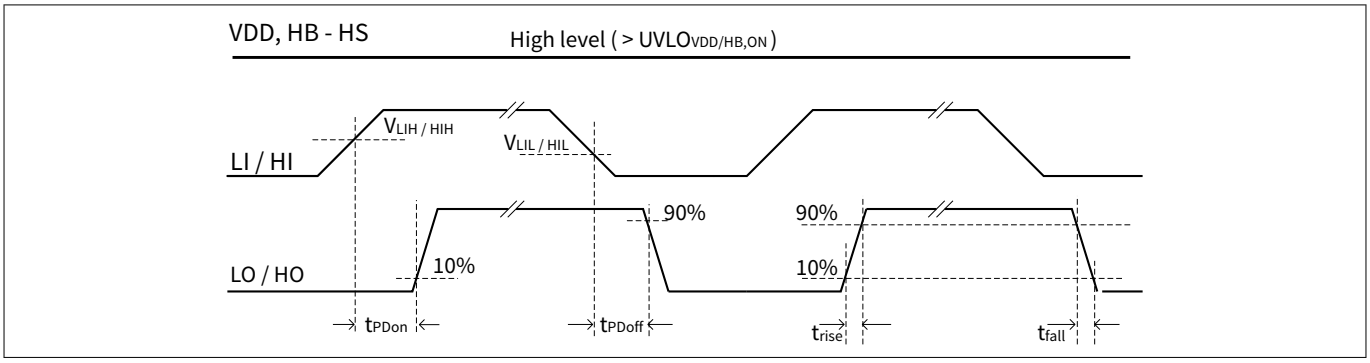


Figure 6 INx to OUTx propagation delays, rise and fall times

Figure 7 illustrates the channel-to-channel propagation delay mismatch at the unloaded outputs. This parameter is relevant when the channels drive parallel switches as it represents the delay in the two driving signals.

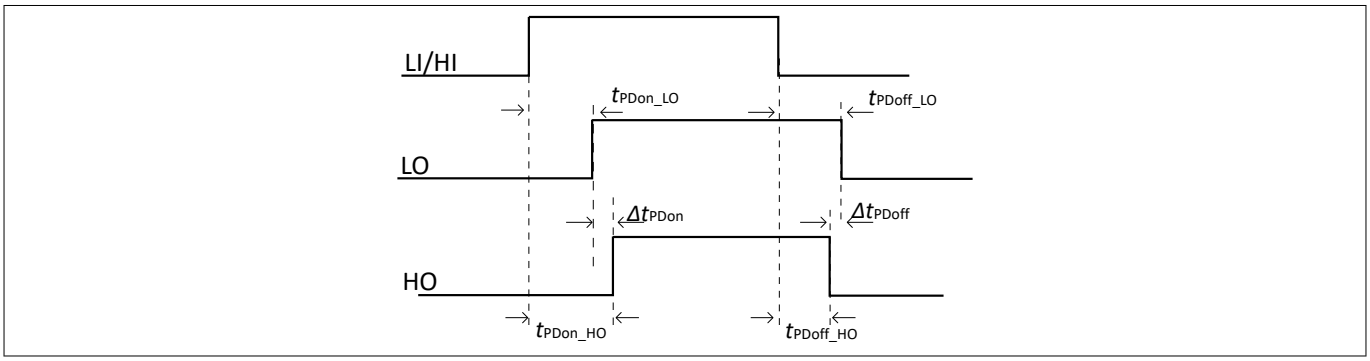


Figure 7 Channel-to-channel propagation delay mismatch

Figure 8 illustrates the pulse width distortion at the unloaded output. Ideally the width of the input pulse (t_{PW_INx}) equals the width of the output pulse (t_{PW_OUTx}); however, the driver introduces an output pulse distortion t_{PWD} given by the difference between ON and OFF propagation delay.

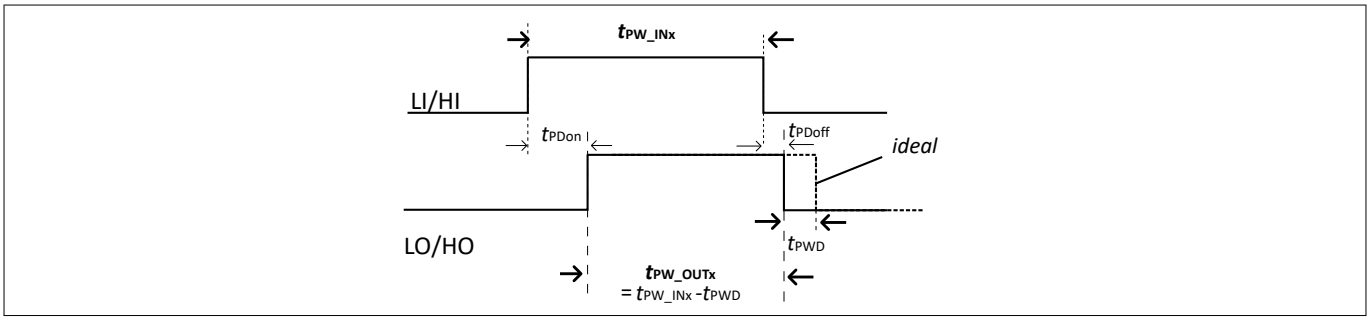


Figure 8 Pulse width distortion

Figure 9 illustrates the dead-time distortion at the unloaded outputs. This parameter is relevant in operation with complementary signals, as for the half-bridge driving when a certain dead-time t_{DT_INx} is set on the inputs LI, HI. Ideally the dead-time on the driver output (t_{DT_OUTx}) equals the input dead-time; however, the driver introduces a distortion t_{DTD} given by the difference between the OFF propagation delay of one channel and the ON propagation delay of the other channel.

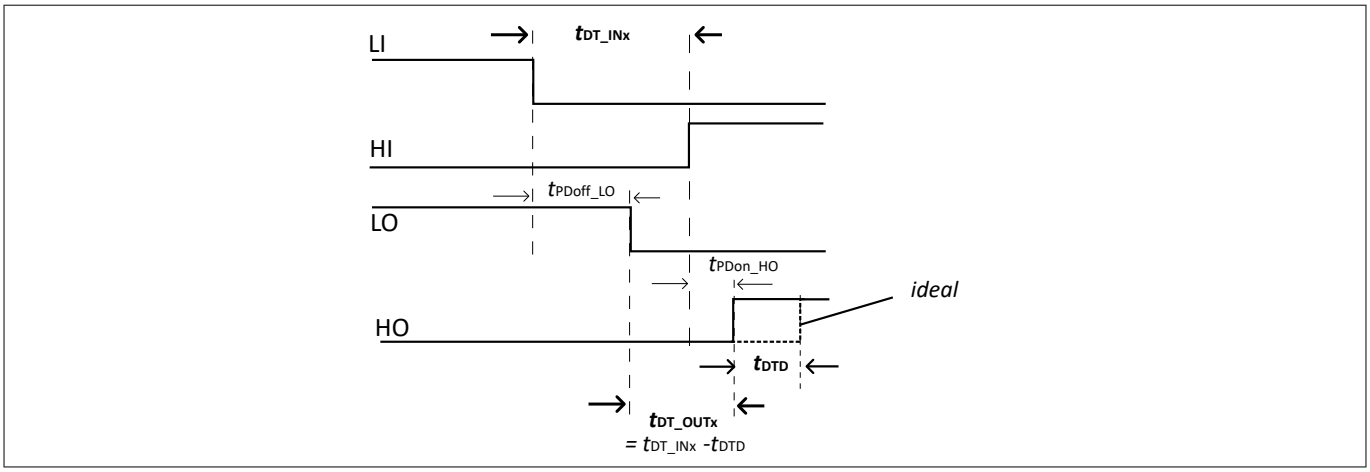


Figure 9 Channel turn-off to channel turn-on propagation delay mismatch

Figure 10 illustrates the behavior or the deglitch filter that filters spurious pulses on LI, HI with duration shorter than t_{PWmin}.

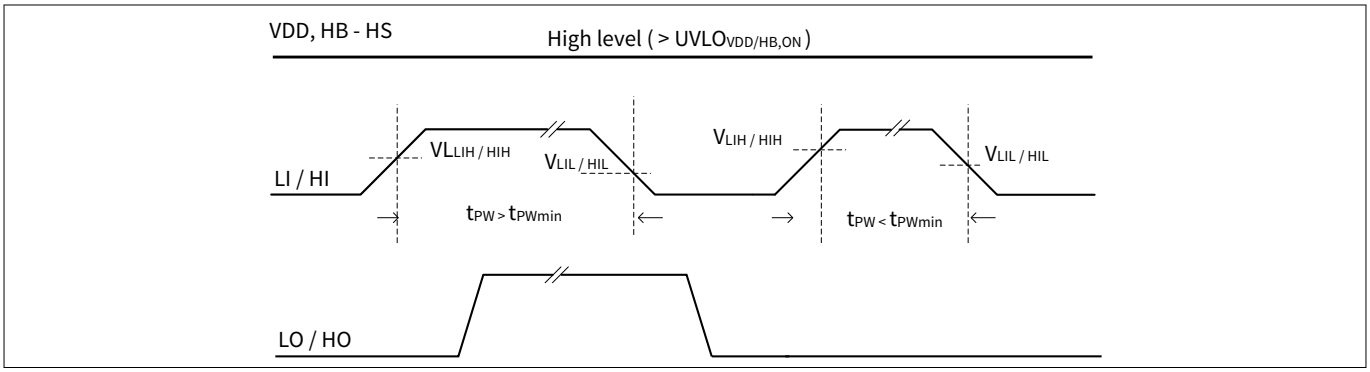


Figure 10 Minimum pulse that changes the output state

Figure 11 illustrates the supply UVLO behavior. It depicts the reaction time to UVLO events when the supply crosses the UVLO thresholds during rising or falling transitions (power-up, power-down, supply noise). The definition for $t_{START,HB}$ and $t_{STOP,HB}$ considers already available VDD, that supplies the logic input responsible of transmitting the high-side PWM via the CT isolation. For more details on the high-side activation and deactivation timing see also Chapter 2.5.1.

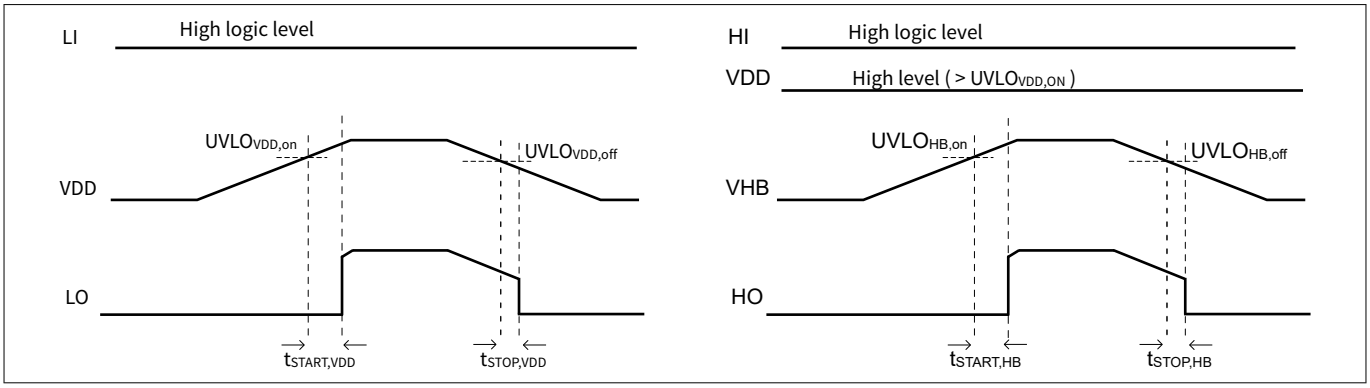
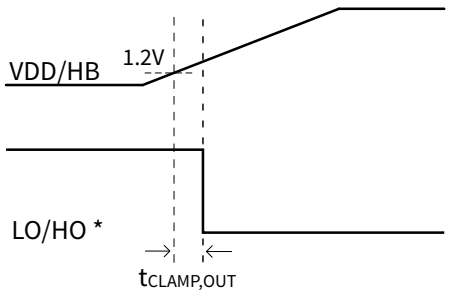


Figure 11

Figure 12 illustrates $t_{CLAMP,OUT}$, the time required to clamp potential output induced overshoots when the supplies are in UVLO condition (V_{DD}/V_{HB} < $UVLO_{VDD/HB,on}$)

4 Timing diagrams



* LO/HO may be pulled up via parasitic coupling on the MOSFET side in UVLO-conditions. As soon as the supply approaches 1.2 V, the driver is able to effectively clamp the overshoot in $t_{CLAMP,OUT}$.

Figure 12 Activation time of output clamping in UVLO conditions (unloaded output)

5 Typical characteristics

V_{DD} = V_{HB} = 12 V, T_A = 25°C, f_{sw} = 1MHz, no load unless otherwise noted.

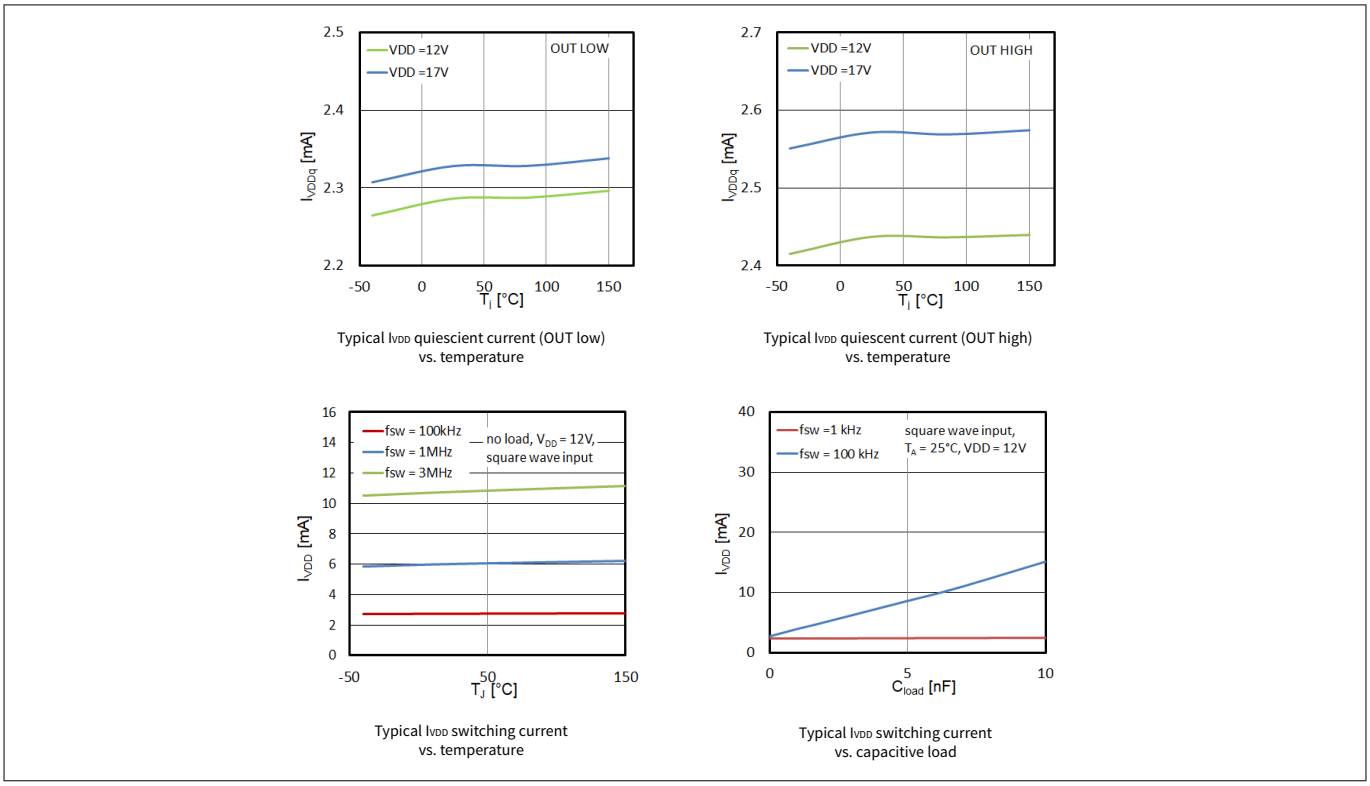
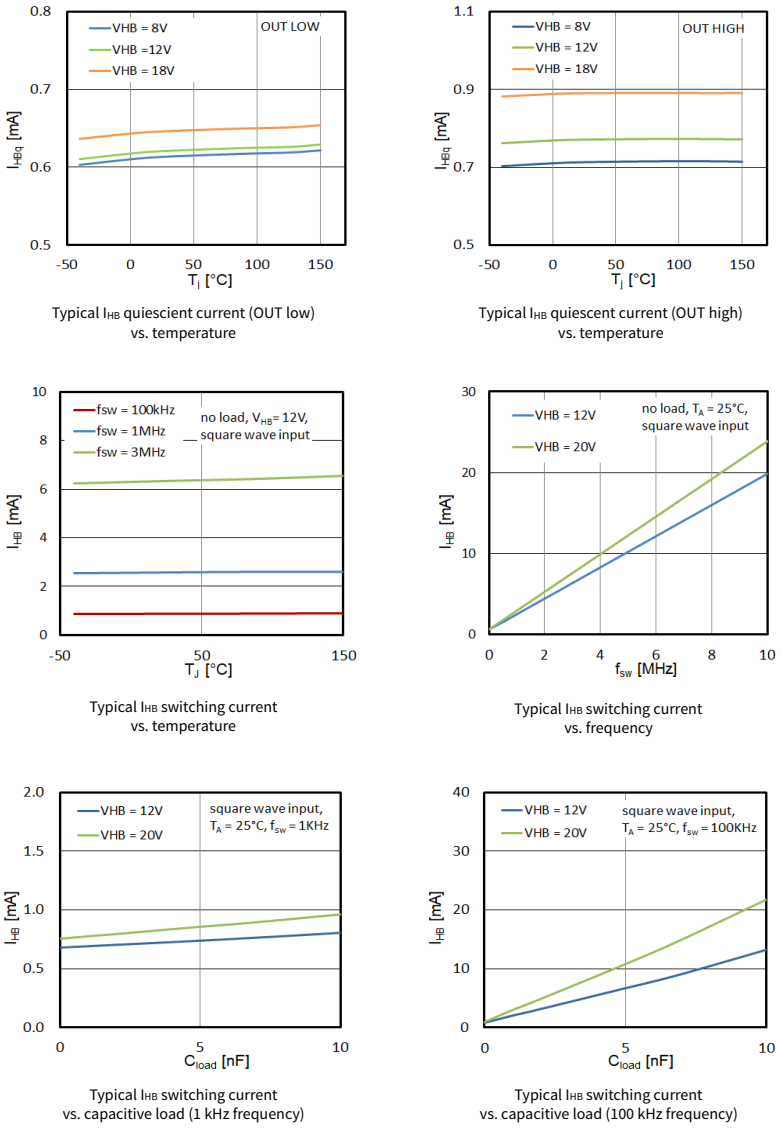


Figure 13 Low-side supply current

5 Typical characteristics



Typical I_{HB} quiescent current (OUT low) vs. temperature

Typical I_{HB} quiescent current (OUT high) vs. temperature

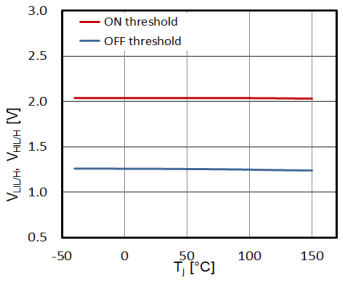
Typical I_{HB} switching current vs. temperature

Typical I_{HB} switching current vs. frequency

Typical I_{HB} switching current vs. capacitive load (1 kHz frequency)

Typical I_{HB} switching current vs. capacitive load (100 kHz frequency)

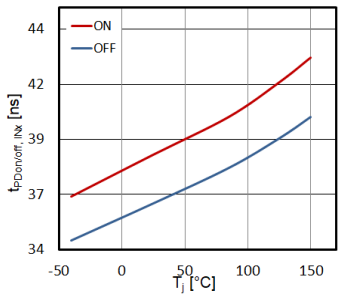
Figure 14 High-side supply current



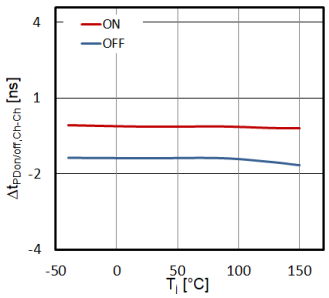
Typical input voltage thresholds vs. temperature

Figure 15 Logic input thresholds

5 Typical characteristics

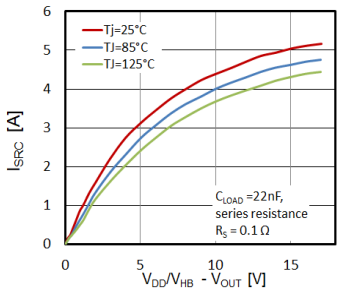


Typical input-to-output propagation delay vs. temperature

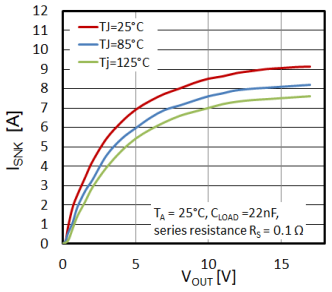


Typical channel-to-channel propagation delay mismatch vs. temperature

Figure 16 Input propagation delay and mismatch

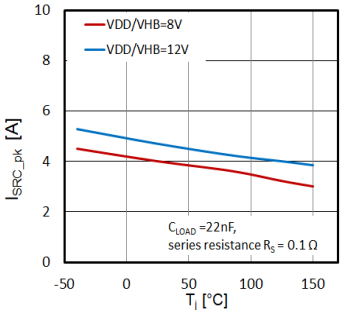


Typical sourcing output current vs. output voltage

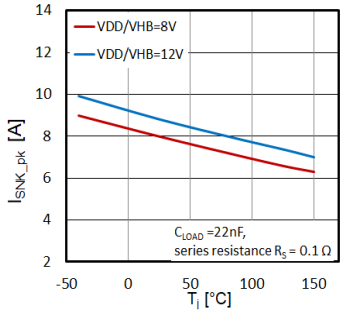


Typical sinking output current vs. output voltage

Figure 17 Source and sink current with output voltage

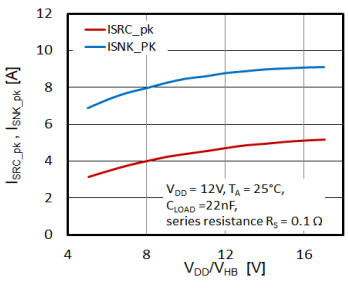


Typical peak sourcing output current vs. temperature



Typical peak sinking output current vs. temperature

Figure 18 Peak source and sink current with temperature



Typical peak output current vs. supply voltage

Figure 19 Peak source and sink current with output supply

6 Application information

***Note**: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

6.1 Output current calculation

The graphs of Figure 17 provide information on the transfer characteristics of the driver output stage nMOS and pMOS thus allowing the user to calculate the real current delivered from the driver in the application. The parameters I_{SRC_pk}, I_{SNK_pk} of Table 10 describe the peak source and sink current delivered from 2EDF5215 when there is no resistive load. In a real circuit the gate resistance is never 0 Ω as the power switch itself contributes with its intrinsic gate resistance. This current, limited by the external resistance, can be calculated based on transfer characteristic as shown in Figure 20 with reference to the turn-on of BSC077N12NS3G.

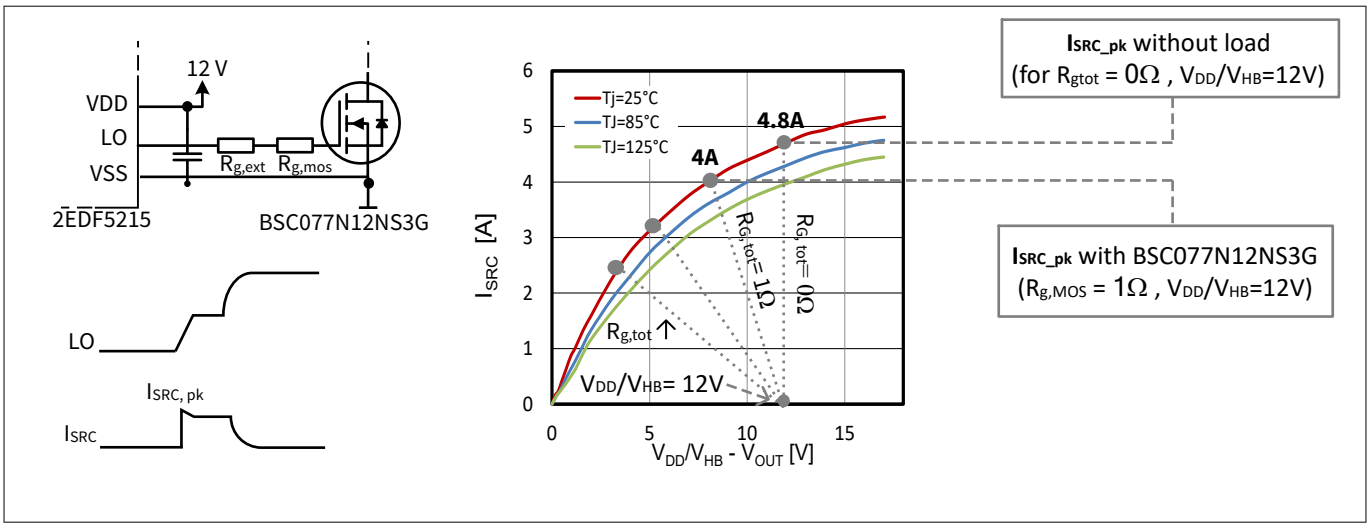


Figure 20 Peak current with resistive load

The current provided by the driver changes over time during a turn-on/-off transition as the gate is charged/ discharged and the voltage drop on the driver output pMOS/nMOS changes consequently. By using the graphs of Figure 17, it is possible to calculate the transition current at any time and thus estimating the switching time. In Figure 21 as example the Miller Plateau current and time is calculated.

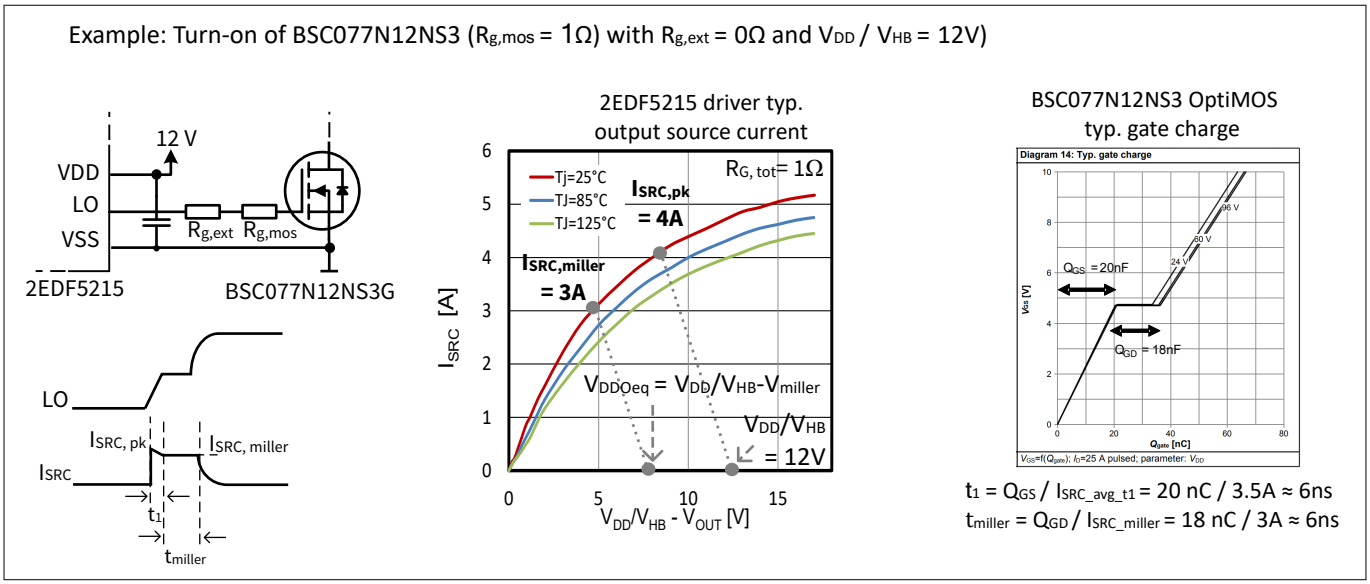


Figure 21 Driver current during the turn-on transition

The calculation is ideal and does not take parasitics into account.

6.2 Bootstrap voltage calculation

2EDF5215 offer an Undervoltage Lockout (see Table 8) optimized for the typical applications based on the following aspects:

- Thermal inversion point of the driven MOSFET
- Miller plateau of the driven MOSFET
- Voltage drop on the bootstrap capacitor, when bootstrap is used to supply HB

The thermal inversion point of the MOSFET transfer characteristic is where the thermal coefficient changes in polarity (see Figure 22). For gate-to-source voltages lower than the thermal inversion point, the current shows an increase with temperature thus leading to potential runaway in case of paralleled MOSFET. Typical OptiMOS™ thermal inversion points lay well below 6 V.

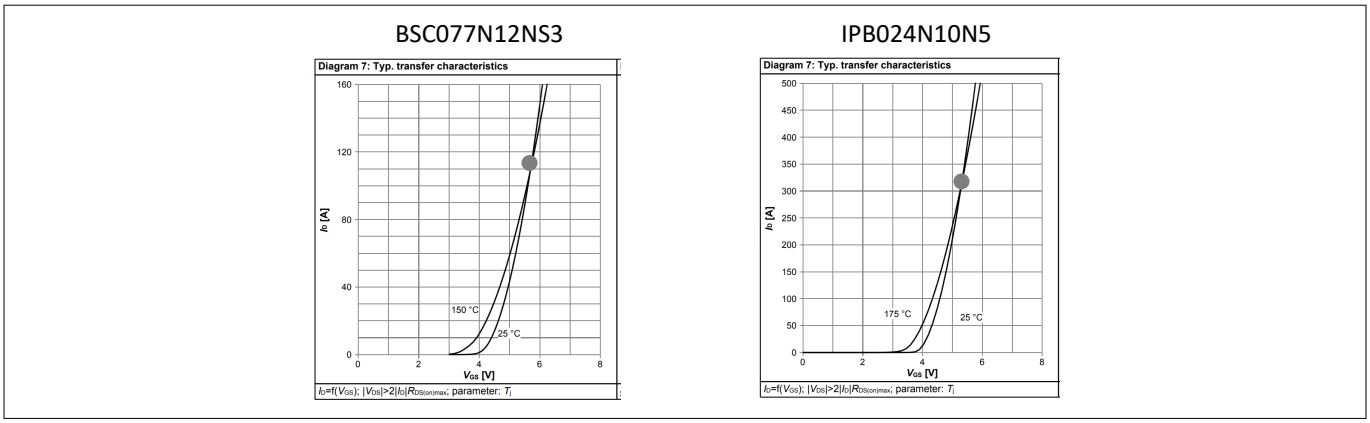


Figure 22 Example of thermal inversion point

When bootstrap is used, at any switching cycle the voltage on the bootstrap capacitor gets charged during low-side MOSFET on state and discharged during its off-state. The discharge is given by two contribution: the charge sunk by the driver to turn-on the high-side MOSFET and the discharge given by the driver ON-state quiescient current (I_{HBq}). Under conditions with long non-switching periods (for example burst-mode, system recovery), additional terms apply (see application note).

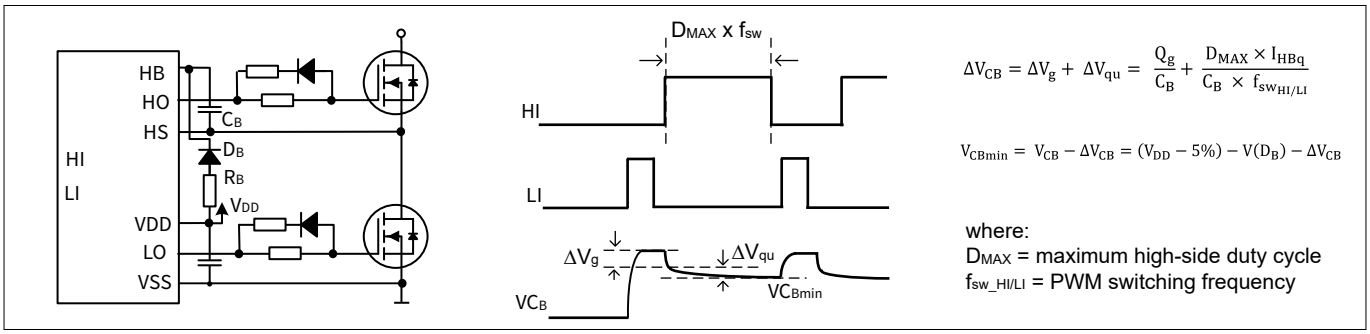


Figure 23 Voltage drop on bootstrap capacitor in normal operation

The selected UVLO for 2EDF5215 offers enough margin against V_{CBmin} in typical use cases with V_{GS} = 10 V even when a very small bootstrap capacitor (for example 47 nF) is considered. As an example, V_{CBmin} of 7.76 V is calculated when driving BSC077N12NS3 OptiMOS™ (Q_g = 26 nC for hard switching) considering $V(D_B)$ = 1 V, V_{DD} accuracy of 5% (0.5 V), $f_{sw\_LI/HI}$ = 100 kHz, D_{MAX} = 90% (for example buck-boost solar optimizers), I_{HBq} = 1 mA (maximum current as worst case), C_B = 47 nF.

6.3 Layout recommendations

For any fast-switching power system the PCB layout is crucial to achieve optimum performance. Among the many existing rules, recommendations, guidelines, tips and tricks, the ones of highest importance are listed as follow.

- Use low-ESR decoupling capacitances (CVDD, CHB) and place them as close as possible to the driver to support high peak currents during switching and to ensure stable supply voltages for the driver. The use of PCB planes at ground potential is also recommended to further reduce the inductance to ground.
- Minimize the gate loop inductance by placing the driver as close as possible to the driven transistor and by ensuring that the gate traces are always placed on top of a PCB plane at ground (GNDO) potential. Minimizing the power loop inductance is the key measure to limit voltage overshoots and enable fast switching.
- In case of bootstrapping, minimize the bootstrap loop inductance to ensure reliable operation and fast bootstrap charge. The bootstrap capacitor is, in fact, charged every cycle through the bootstrap diode and the turned-on low-side transistor and the loop is subject to potential high peak charging currents.
- Pay attention to keep any source of noise (like half-bridge high-current switching traces) away from the driver to avoid any coupling capacitance.
- Connect the driver ground pin to proper PCB planes to reduce the junction-to-board resistance and support the spread of heat outside the driver.

A layout recommendation for EiceDRIVER™ 2EDF5215F is given in Figure 24.

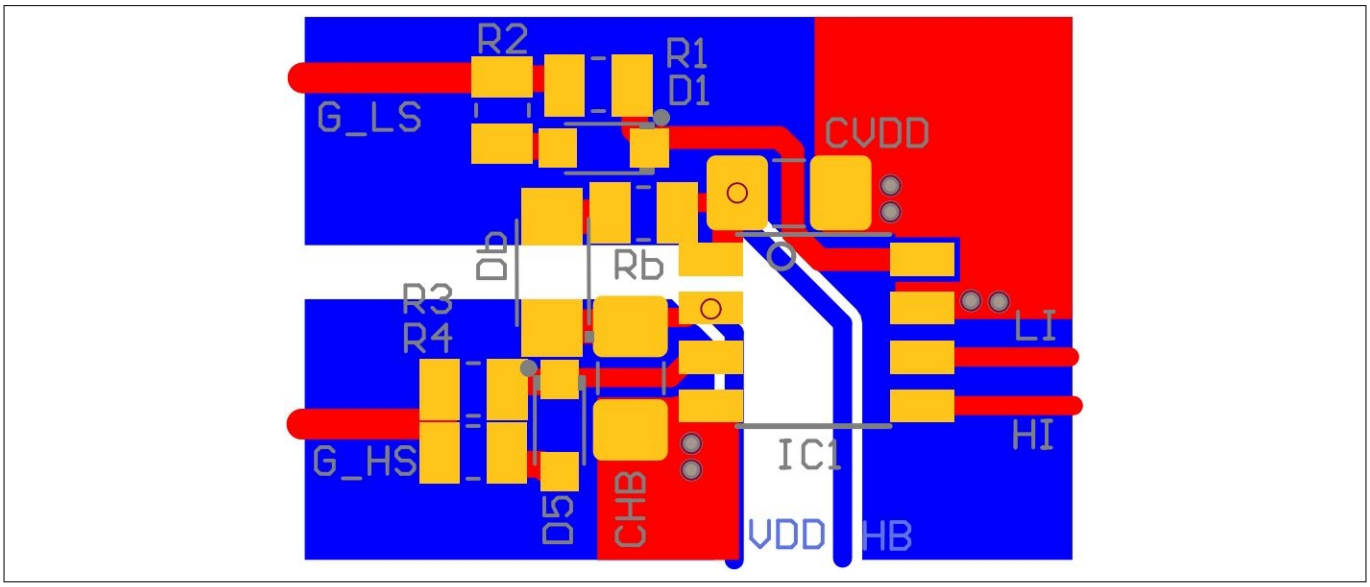


Figure 24 2EDF5215F Layout recommendation

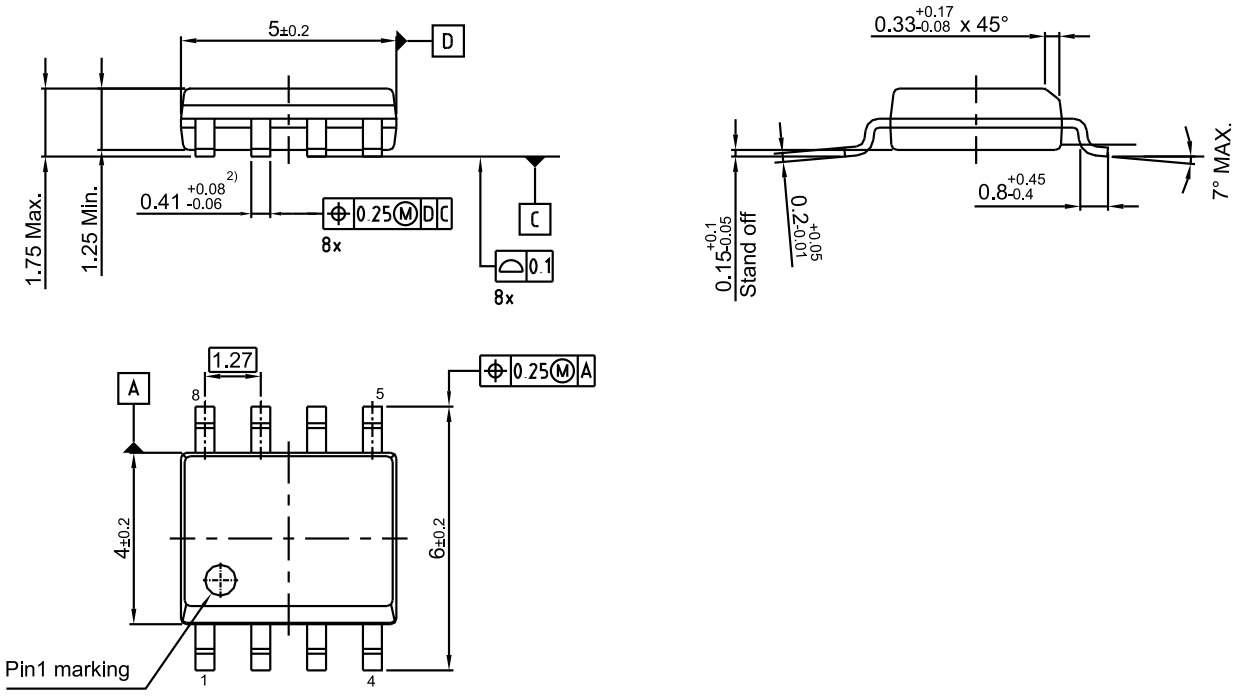
7 Package

7.1 Device numbers and markings

Table 13 Device numbers and markings

Part number	Orderable part number (OPN)	Device marking
2EDF5215F	2EDF5215FXUMA1	2F5215B
2EDF5215G	2EDF5215GXUMA1	2F5215B

7.2 Package PG-DSO-8



1) Does not include plastic or metal protrusion
2) Does not include dambar protrusion of 0.127 Max. in excess of the lead width dimension
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]
Drawing according to ISO 8015 general tolerances ISO 2768-mk

Figure 25 PG-DSO-8 outline

7 Package

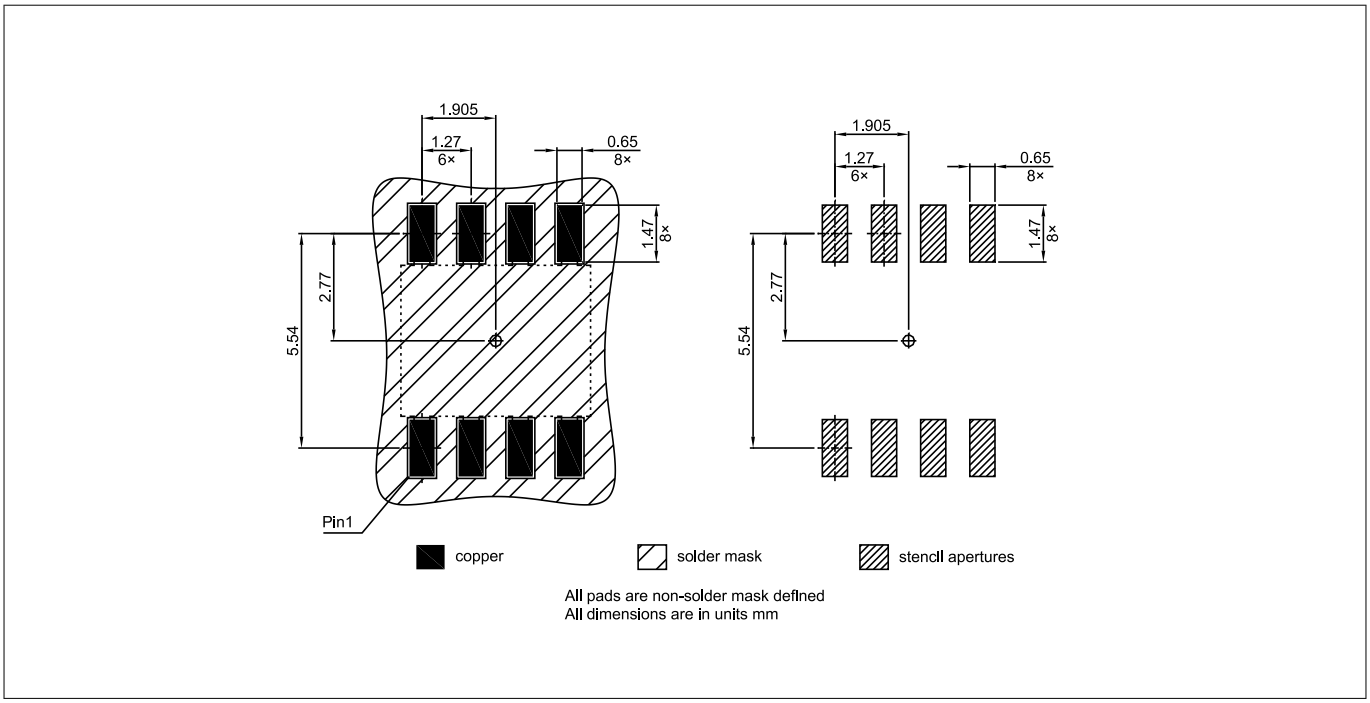


Figure 26 PG-DSO-8 footprint

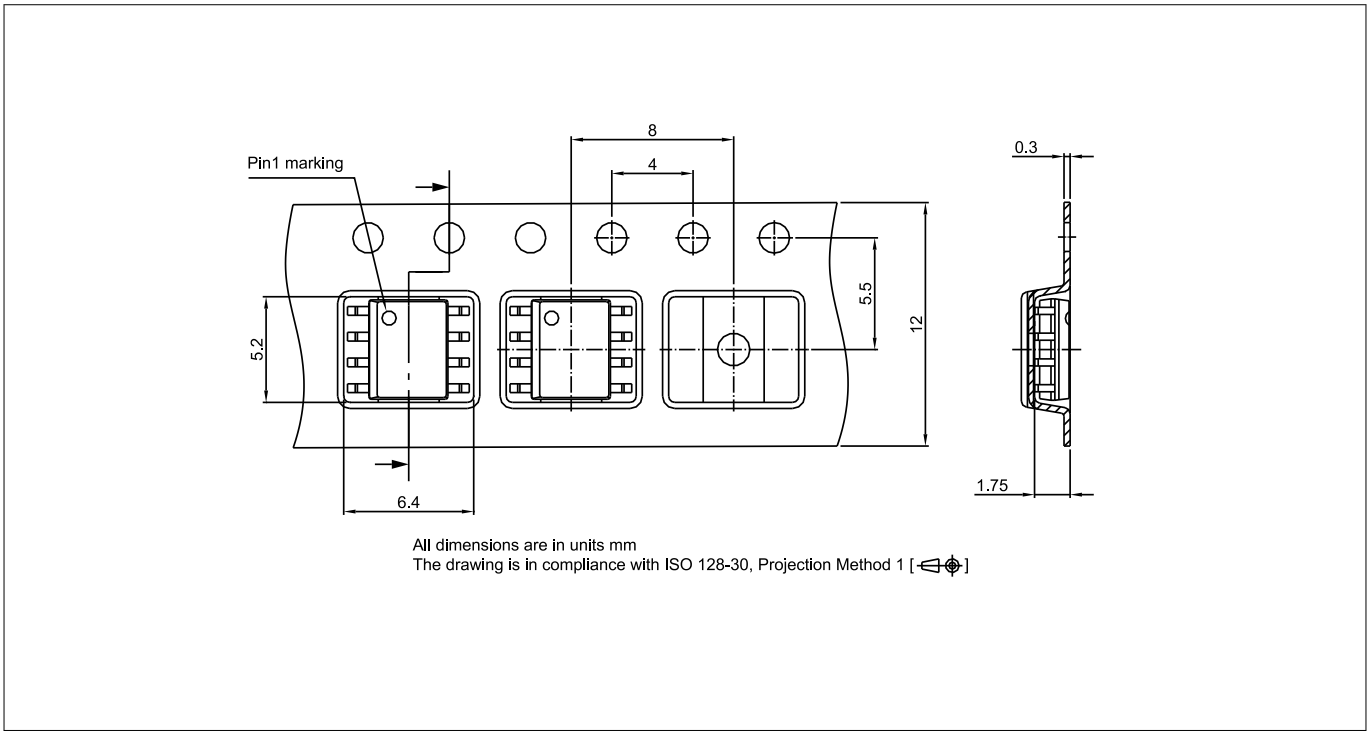


Figure 27 PG-DSO-8 packaging

7.3 Package VDSON-8

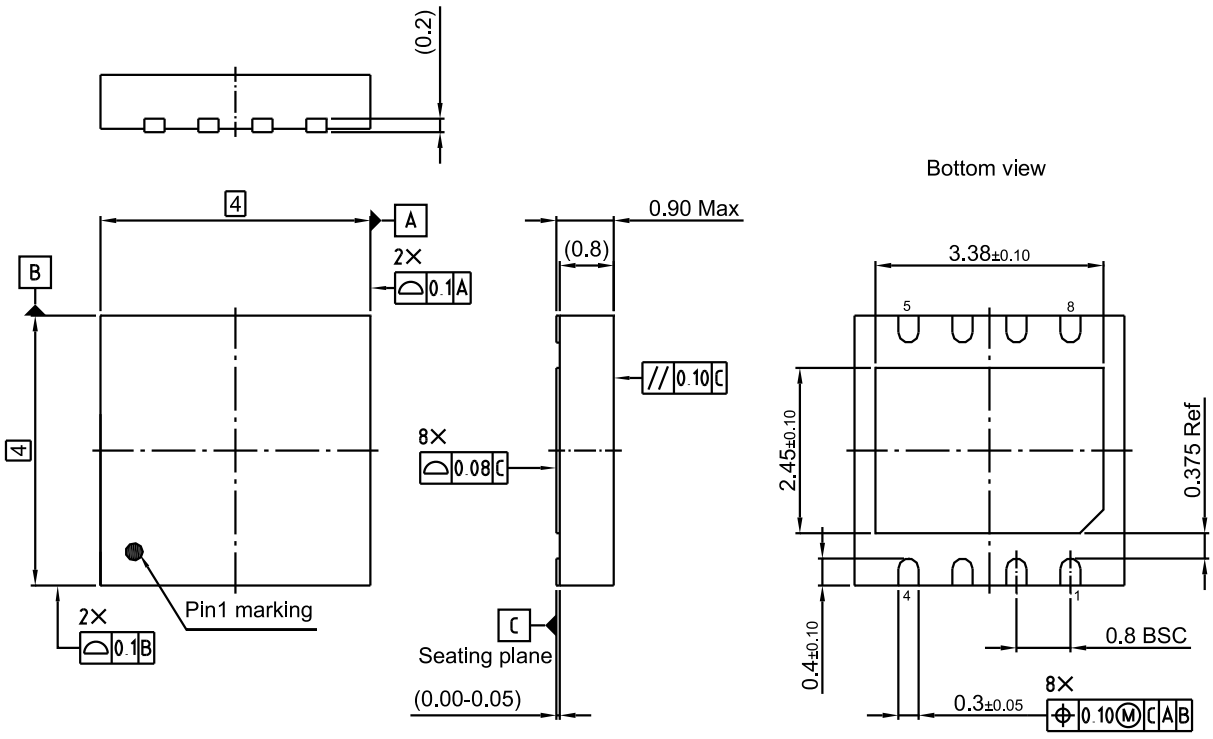


Figure 28 VDSON-8 outline

7 Package

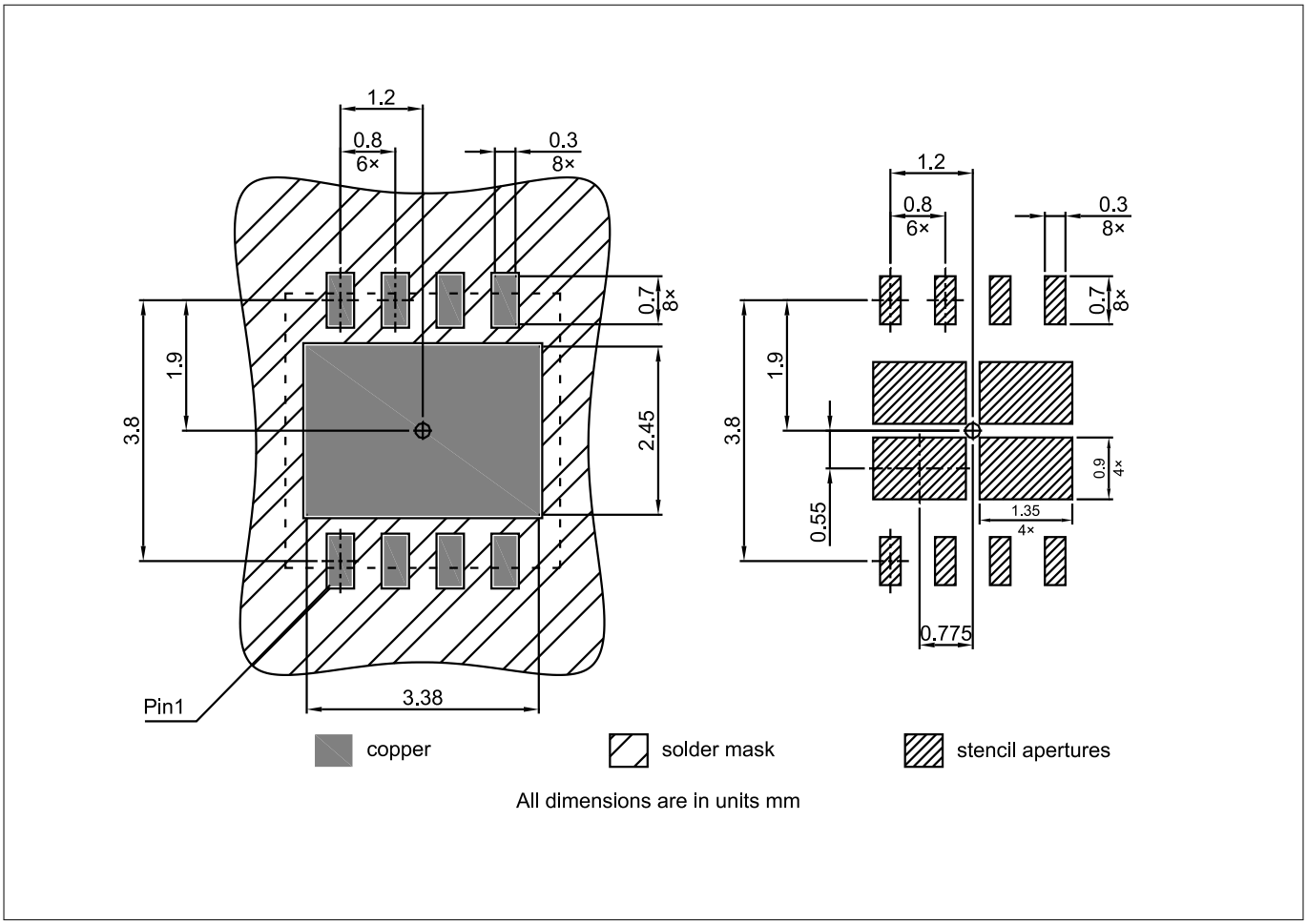


Figure 29 VDSON-8 footprint

7 Package

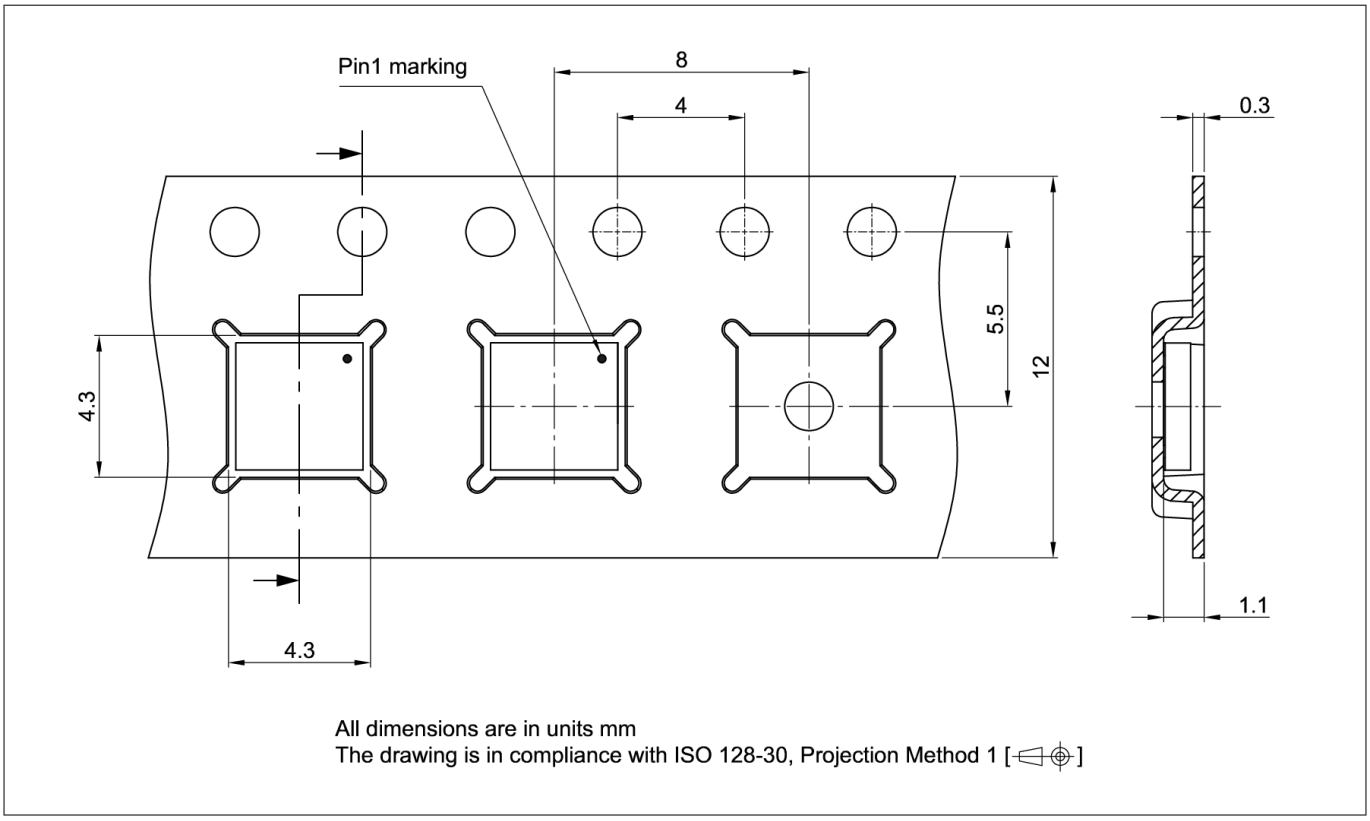


Figure 30 VDSON-8 packaging

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020). Further information on packages: https://www.infineon.com/packages

8 Revision history

Table 14 Revision history

Revision	Date	Description of changes
Rev.1.0	2024-06-07	Initial release

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