

# CDM10V

## Flexible 0-10V Dimming Solution

### Features

- Simplest 0-10 V design on the market. CDM10V comes with default settings:
  - 5% minimum duty cycle
  - 1kHz PWM frequency
  - 200µA Dimmer/Resistor Bias current
  - Dim-To-Off disabled
- The simple one time programmable option allows setting in a wide range:
  - Minimum duty cycle: 1%, 2%, 5%, 10%
  - PWM output frequency: 200Hz, 500Hz, 1kHz, 2kHz
  - Dimmer/Resistor Bias Current: 50µA, 100µA, 200µA, 500µA
  - Dim-to-Off: disabled/enabled
- Wide input  $V_{CC}$  range from 11 to 25 V
- Transparent PWM mode (PWM Bypass Mode in DIM-TO-OFF enabled mode)
- Replaces many external components with a single chip reducing BOM and PCB space
- Minimum variation from device to device

### Applications

- LED Drivers needing 0-10 V Dimming Circuits
- Industrial and Commercial Dimmable Applications:
  - Luminaires, Troffers, Downlights, Sconces, Undercabinet, Office Lighting, Signage applications, Dali applications

Product Type	Package
CDM10V	SOT23-6

### Description

CDM10V is a fully integrated 0-10 V dimming interface IC and comes in a SOT-23-6 package to cover space requirements on small PCBs.

The device is targeted for various dimming applications in lighting. The IC can be used to transmit analog voltage based signals from a 0-10 V dimmer or potentiometer to the dimming or PWM input of a lighting controller IC in the form of a 5 mA current based PWM signal to drive an external opto-coupler. It replaces many components in a traditional solution and reduces BOM and PCB space significantly.

The CDM10V IC outputs a 0 - 100% PWM current signal at programmable frequency with an amplitude value of 5 mA.

The duty cycle of the PWM signal can be limited to a dedicated minimum value. Dim-to-off feature is supported as well and can be enabled on demand.

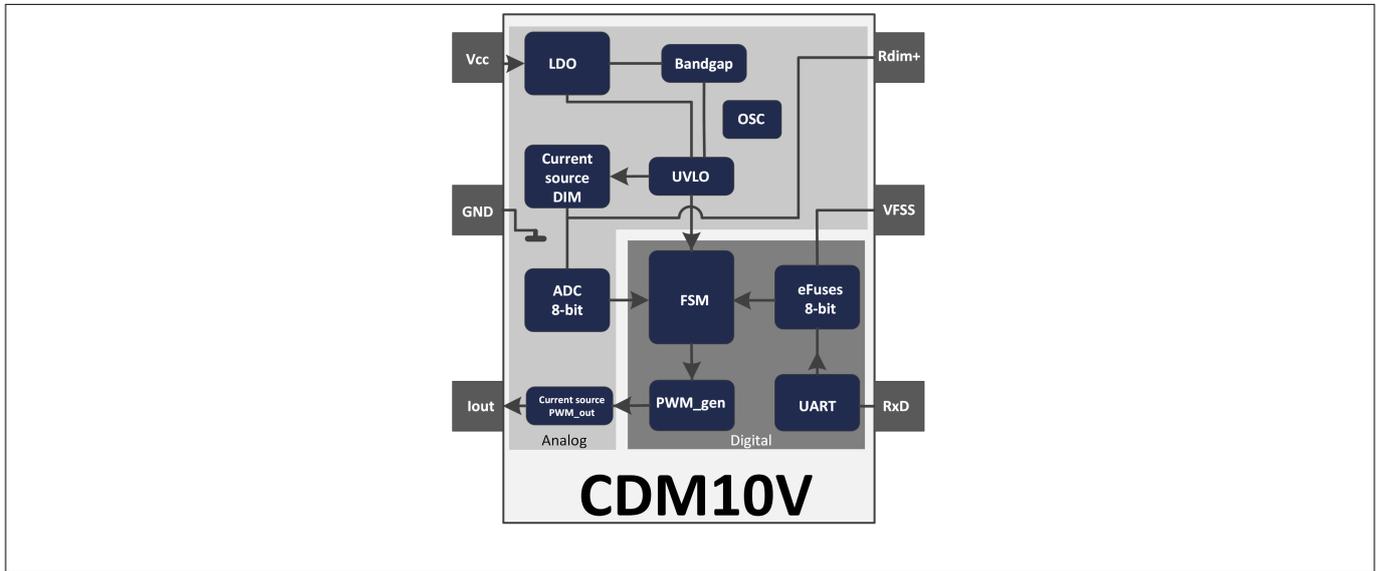
Embedded digital signal processing maintains minimum variations from device to device.

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**Block Diagram**

**1 Block Diagram**



**Figure 1 Block Diagram of the CDM10V**

**2 Pin Configuration**

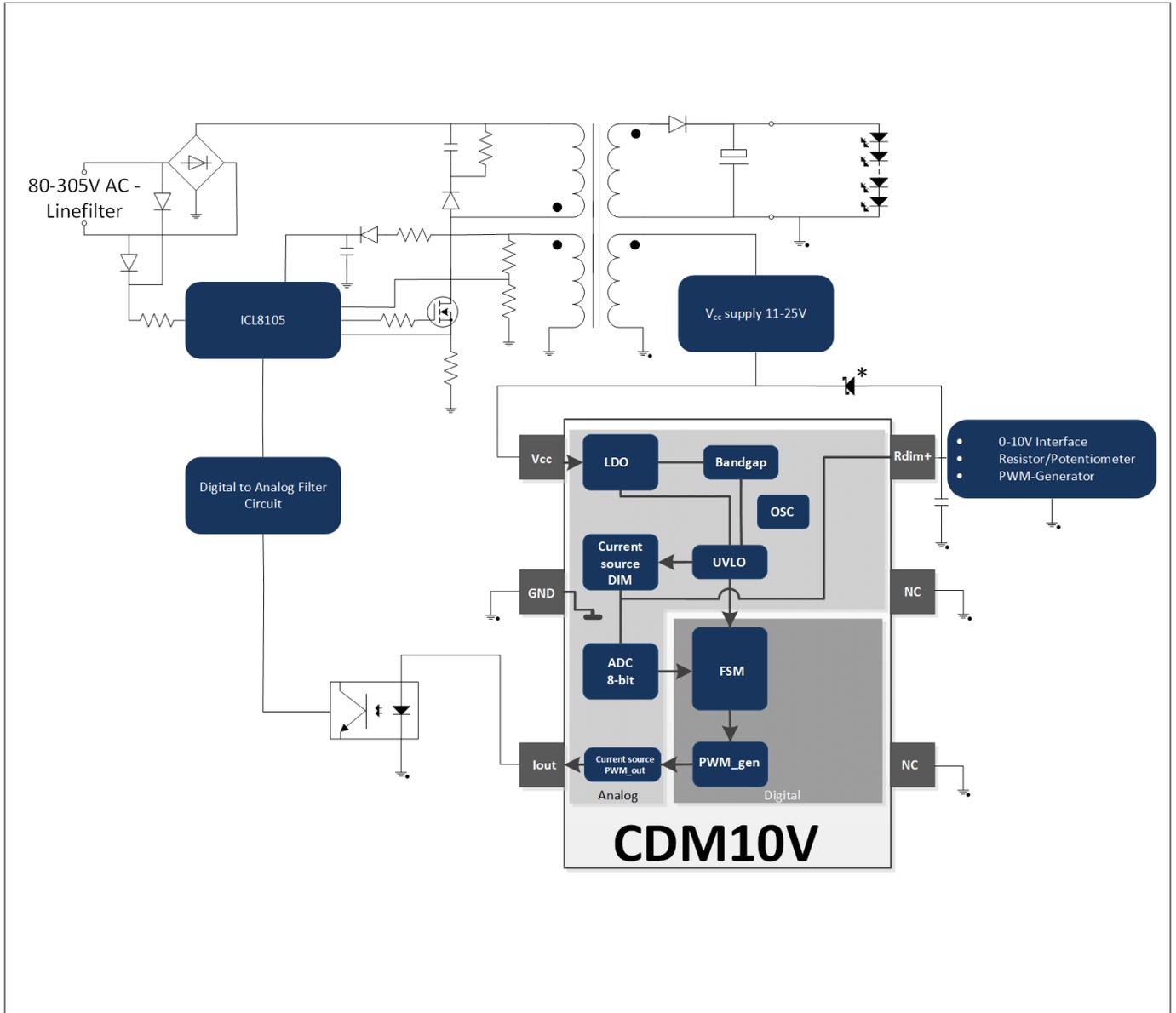
**Table 1 Pin configuration**

Pin	Name	Function
1	V <sub>CC</sub>	Input voltage 11V - 25V
2	GND	GND
3	I <sub>out</sub>	PWM output current 5mA
4	RxD	RxD for eFuse programming, connect to GND for normal operation
5	V <sub>FSS</sub>	Fusing voltage (4,1V) eFuse programming, connect to GND for normal operation (internal pull-down)
6	R <sub>dim+</sub>	Dimmer current output /Voltage sense

**Functional Description**

**3 Functional Description**

**Typical Application Circuit**



**Figure 2 Typical Application Circuit**

*Note:* The Diode marked with \* is for the protection of the  $R_{dim+}$ -Pin when active dimming is used. This is because the voltage on this Pin is not allowed to be higher than  $V_{CC}+0.5V$ . It is advised to use a low leakage, low reverse current Schottky-Diode in order to not influence the dimming performance (e.g. MMSD301T1G).

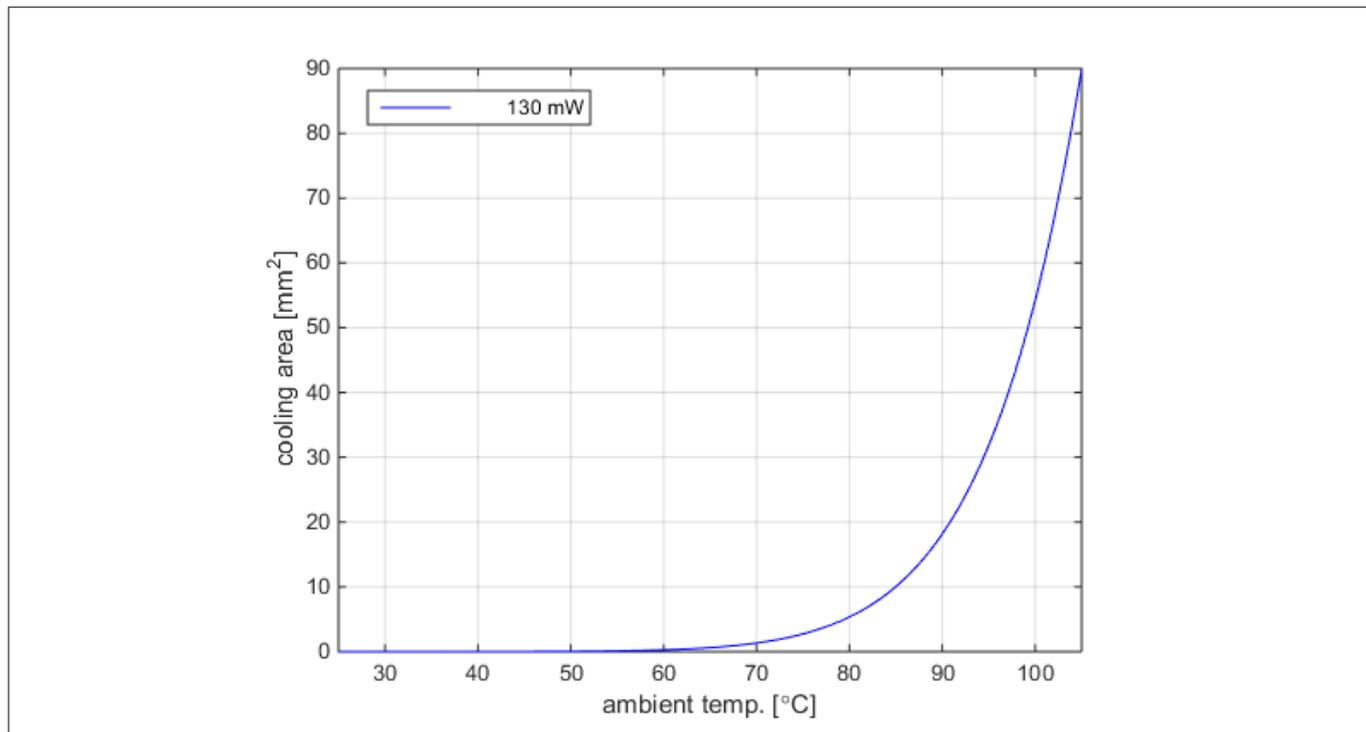
*Note:* The capacitor connected to the  $R_{dim+}$ -Pin reduces the amount of coupled noise to the dimming signal. The size of this capacitance should be in the range of 2.2 - 10 nF (typ. 4.7 nF), where a small capacitor allows steeper edges of the dimming signal, a larger capacitor enhances the noise reduction.

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**Functional Description**

**Recommended cooling area**

In order to guarantee the full functionality of the CDM10V device, the required cooling area has to be selected according to the graph in [Figure 3](#).



**Figure 3 Cooling area over ambient temperature CDM10V**

**Functional Description**

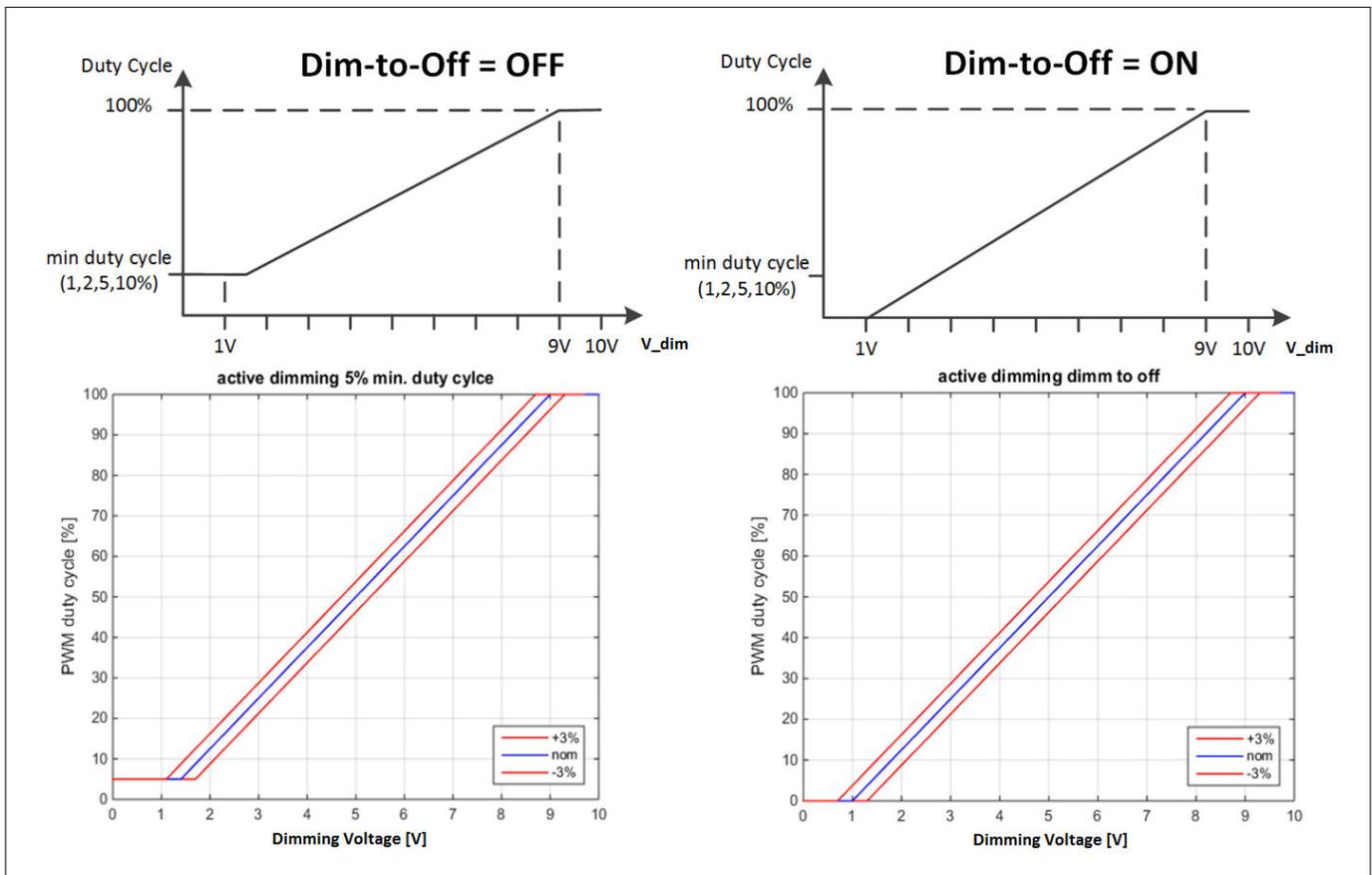
**Dimming Characteristic**

**Table 2** PWM Output current referring to  $R_{dim+}$ -Pin Voltage

$R_{dim+}$	$I_{out}$
<1 V	PWM @ min duty cycle or Dim-to-OFF
1 - 9 V	min duty cycle (@ 1V)...100% (@ 9V)
>9V (max. applicable Voltage: $V_{CC}$ )	Always active

Calculation of the lower dimming voltage boundary for entering min duty cycle:

$$1\text{ V} + \text{min Duty Cycle} \times 8\text{ V}$$



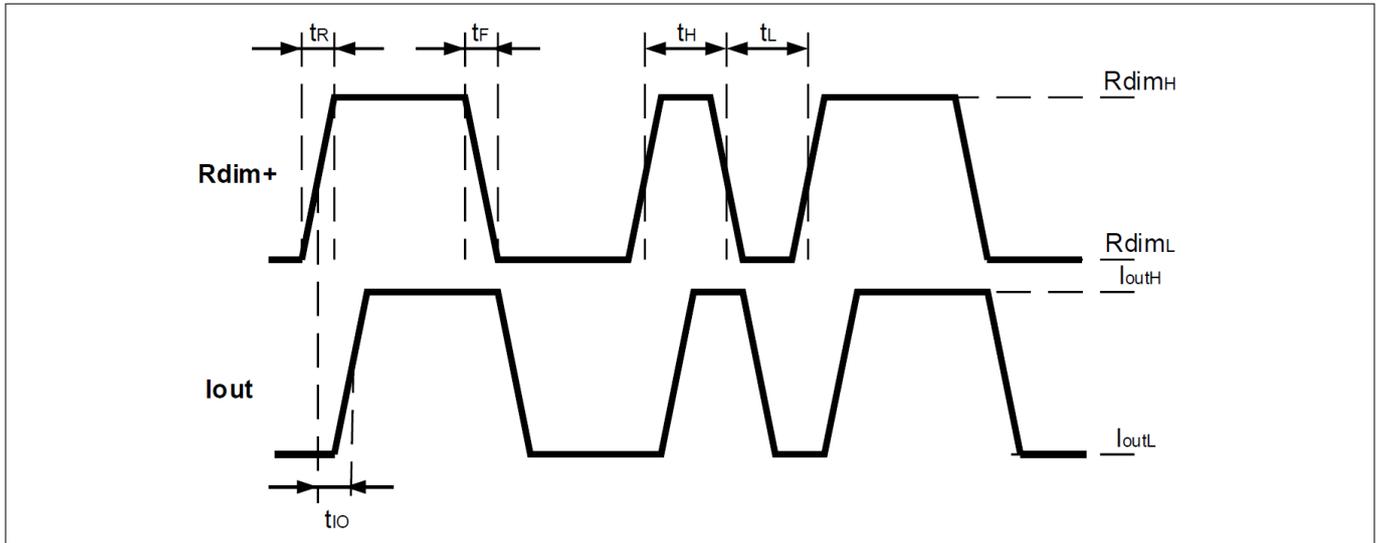
**Figure 4** Dimming Characteristic

**Functional Description**

**Transparent Mode**

CDM10V device can be configured for usage in transparent mode. In this mode the PWM signal on R<sub>dim+</sub> input will be provided directly to I<sub>out</sub>.

Pre-condition to enable the transparent mode is to fuse the DIM2OFF bit to HIGH and PWM frequency to 2 kHz, PWM minimum duty cycle is not used in this mode and can stay in default configuration.



**Figure 5** Transparent mode timing diagram

**Table 3** Conditions for the transparent mode

Condition	Name	Min	Nom	Max
R <sub>dimH</sub>	R <sub>dim+</sub> High Value	9.3 V		V <sub>CC</sub> +0,5V
R <sub>dimL</sub>	R <sub>dim+</sub> Low Value	-0.5 V		0.5 V
I <sub>outH</sub>	I <sub>out</sub> High Value		R <sub>Iout</sub> * 5mA <sup>1</sup>	
I <sub>outL</sub>	I <sub>out</sub> Low Value		0.0 V	
t <sub>IO</sub>	Propagation delay		8.8 μs	
t <sub>H</sub>	Min puls width High	2.6 μs		
t <sub>L</sub>	Min puls width Low	2.6 μs		
t <sub>R</sub>	Rising edge time			1.8 μs
t <sub>F</sub>	Falling edge time			1.8 μs

Note: <sup>1</sup> R<sub>Iout</sub> is the resistance connected between the I<sub>out</sub> and the GND-PIN

**Image** shows the maximum I<sub>out</sub> resolution versus the R<sub>dim+</sub> frequency. The dependency can be calculated using following formula:

$$f_{Rdim} = \frac{I_{out} \text{ resolution}}{100 \times 2.6 \mu s}$$

For 1% resolution we get:

$$f_{Rdim} = \frac{1}{100 \times 2.6 \mu s} \approx 3.85 \text{ kHz}$$

Functional Description

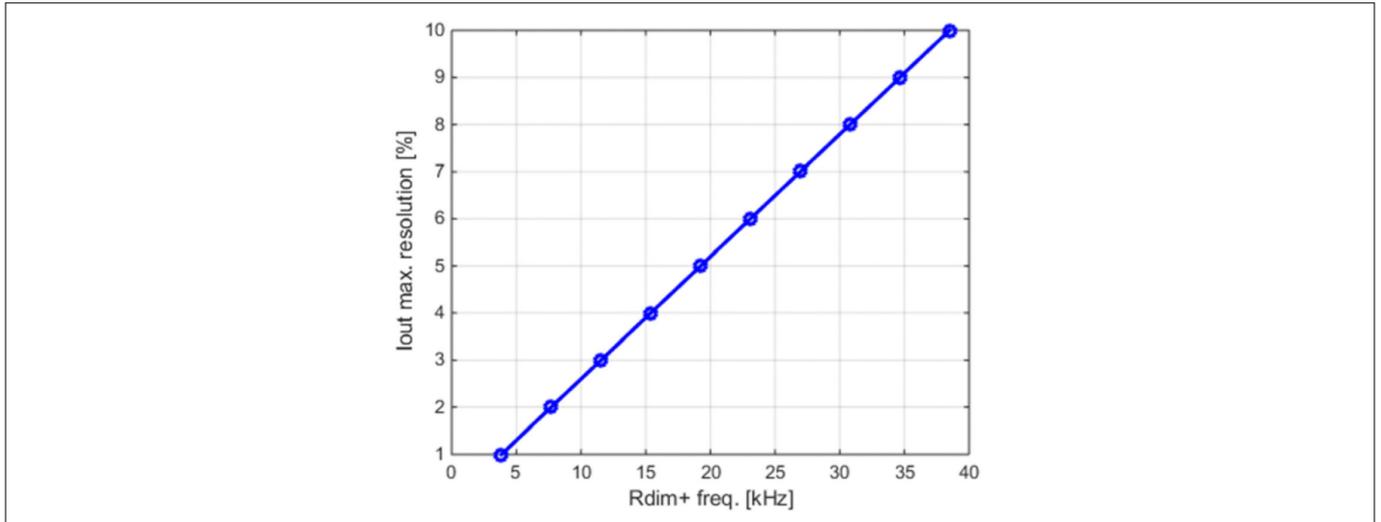


Figure 6 I<sub>out</sub> resolution versus the R<sub>dim+</sub> frequency

**Functional Description**

**Optocoupler Selection Guide**

CDM10V converts an analog dimming signal into a PWM waveform. In the majority of applications the dimming signal needs to be isolated from the rest of the application and an optocoupler is used to implement either functional or reinforced isolation. Optocouplers are an excellent choice since they are very cost effective but nevertheless able to comply with virtually all safety standards.

The most common and cost effective optocouplers are four-pin devices consisting of a LED and a photo-sensitive BJT. With four pin devices only collector and emitter of the BJT are connected to pins. This limits device performance, especially switching times, as will be discussed later. Six-pin devices having the base of the BJT as well connected to a pin are seen less often. With these six-pin devices bandwidth of the transmission can be improved if necessary. Finally there are high-speed digital couplers available that are designed for very high data rates and offer a buffered output with a nearly perfect PWM signal. While offering superior performance high speed couplers are considerably more expensive than simple LED-BJT couplers.

**Generating an Analog Signal from PWM**

Although the PWM signal itself can be used, either by implementing PWM dimming or using a dedicated SMPS controller that is able to extract the dimming information directly from the PWM waveform, in many applications a DC voltage that is proportional to the desired dimming level is needed. Fortunately it is easy to create an analog signal from PWM: a low pass filter with the right corner frequency will do the job.

As a rule of thumb a corner frequency of  $f_{PWM}/100$  for a first order filter and  $f_{PWM}/10$  for second order filter should be used. With this selection ripple on the generated DC signal is around  $150\text{ mV}_{pp}$  at medium dimming levels and goes down to a few  $10\text{ mV}_{pp}$  at very low and high dimming levels. The first order filter will have a slower time response due to the low corner frequency. Consequently, if for some reason a  $f_{PWM}$  lower than  $1\text{ kHz}$  has to be used, as second order filter will give the better response. With a third order filter it is possible to achieve either negligible ripple on the DC voltage or superior response time.

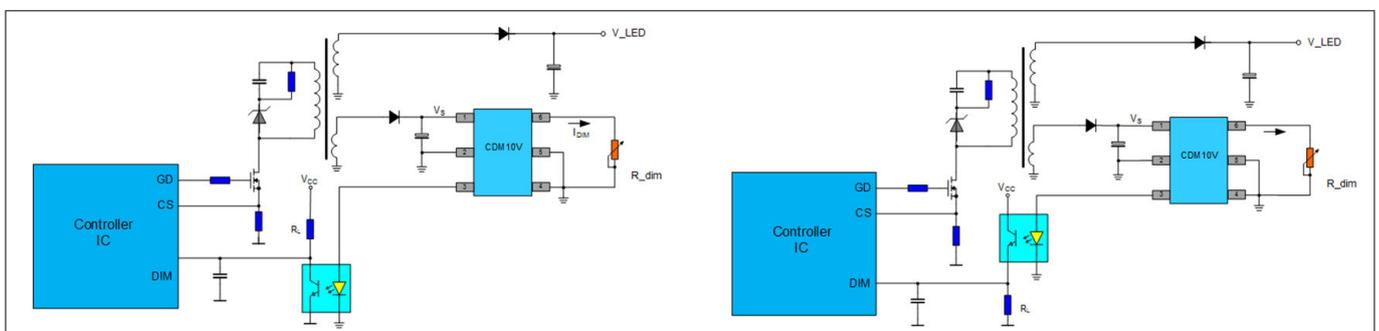
Since the generated DC voltage not only depends on the duty-cycle of the PWM signal but is directly proportional to its amplitude as well it is mandatory to stabilize the amplitude e.g. with a Zener-Diode.

*Image* shows a simplified schematic with second order filter. According to the design guideline given above, good starting values for  $C_1$  and  $C_2$  would be:

$$C_1 = C_2 = 150\text{ nF} \times \frac{1\text{ kHz}}{f_{PWM}}$$

*Note:* Using the ICL8105 the capacitor connected to the UART/Dim-Pin is not allowed to exceed  $1\text{ nF}$  in order to provide proper UART communication if needed.

**Inverted / Non-Inverted Output**



**Figure 7** Simplified schematic of CDM10V with inverted (left) and non-inverted (right) output signal. Both are equivalent in terms of performance

Optocouplers are most often used in the configuration shown on the left of *Image* i.e. the output signal is derived from the collector of the BJT and thus inverted compared to the input signal. An inverted signal is not favorable at all since it will result in an inverted dimming characteristic with the majority of controllers. An additional inverter stage could be used of course, resulting in the proper dimming curve. But there is a simpler

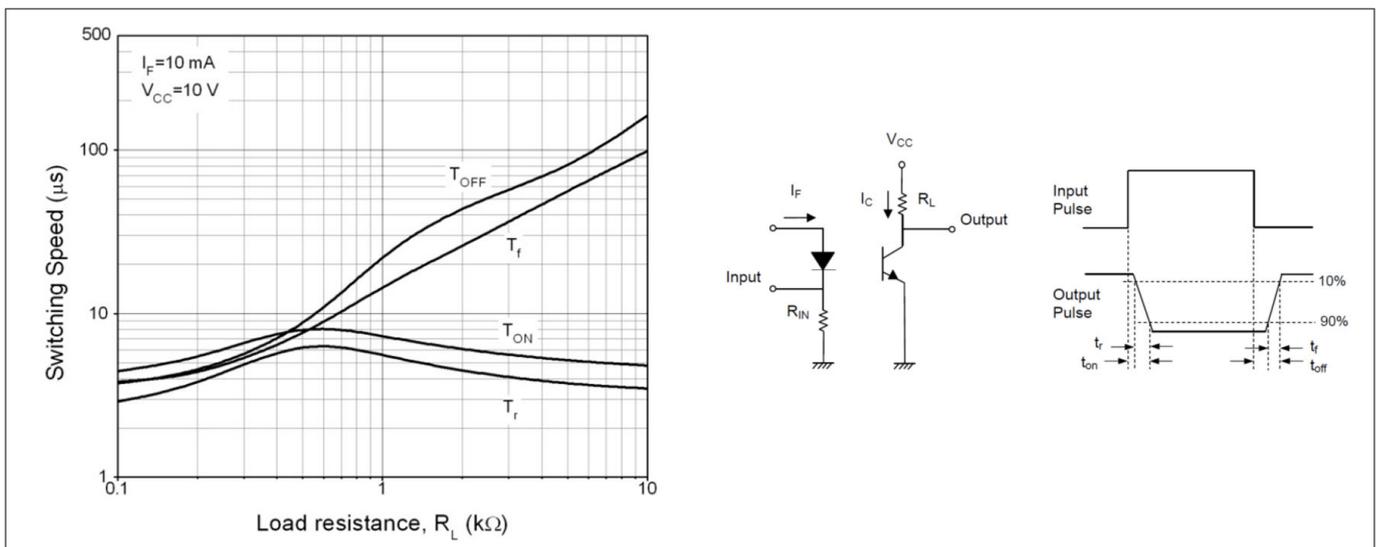
**Functional Description**

solution as well since the four pin optocoupler can be viewed as current controlled current source if  $V_{CE}$  of the BJT is sufficiently high. Consequently the load can be connected either to collector or emitter without significant change in parameters or performance. Therefore the configuration on the right of *Image* is favorable for most SMPS controllers.

**Optocoupler selection**

There are two parameters of an optocoupler that are most important for use with CDM10V: the current transfer ratio CTR and the switching times  $T_r$  and  $T_f$ .

*Image* is a typical plot of  $T_r$  and  $T_f$  vs,  $R_L$  taken from the data sheet of a widely used 4-pin optocoupler. Both parameters depend on the load resistance  $R_L$ . But while  $T_r$  doesn't vary too much and shows a moderate maximum for  $R_L$  of few hundred ohms,  $T_f$  is constantly increasing with  $R_L$ , reaching about 100  $\mu$ s for  $R_L$  around 10 k $\Omega$ . These times are much longer than the minimum pulse length generated by CDM10V shown in table *Table 4*. Consequently relative low values for  $R_L$  around 100  $\Omega$  seem to be necessary in order to achieve reasonable switching times. But it's important to mention, that switching times shown in *Image* are determined with saturated BJT (this means the load resistance limits the IC to a lower value than would be determined by LED current) and with non-saturated BJT switching times can be small, even with higher load resistance.



**Figure 8 Typical optocoupler switching times vs. load resistance together with test circuit.**

Before discussing influence of load resistance on switching performance further, the second important parameter of the coupler, CTR, needs investigation.

**Table 4 Shortest pulse length for different frequencies and minimum dimming levels of CDM10V**

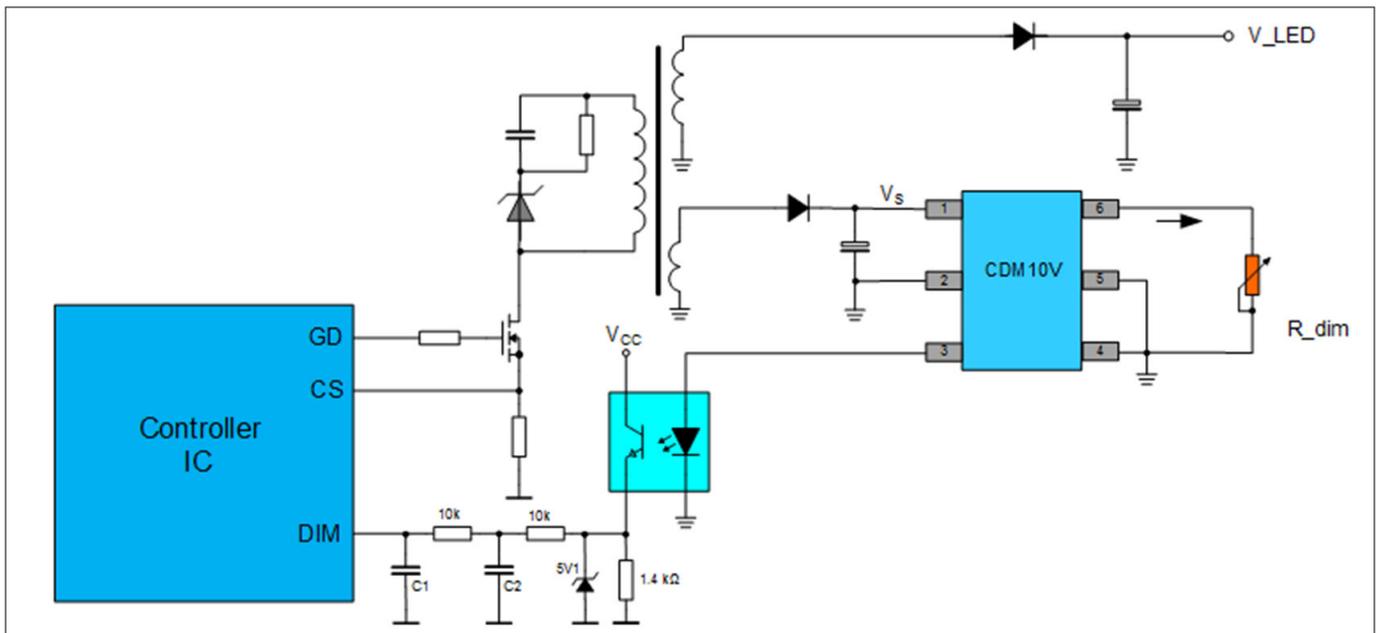
Frequency	Dim-to-off	1%	2%	5%	10%
200 Hz	1.2 $\mu$ s	50 $\mu$ s	100 $\mu$ s	250 $\mu$ s	500 $\mu$ s
500 Hz	7.84 $\mu$ s	20 $\mu$ s	40 $\mu$ s	100 $\mu$ s	200 $\mu$ s
1 kHz	3.92 $\mu$ s	10 $\mu$ s	20 $\mu$ s	50 $\mu$ s	100 $\mu$ s
2 kHz	1.96 $\mu$ s	5 $\mu$ s	10 $\mu$ s	25 $\mu$ s	50 $\mu$ s

As the name implies, CTR is simply the ratio between the forward current  $I_F$  of the LED and the resulting collector current  $I_C$  of the phototransistor and usually expressed in percent. A CTR of 50% for example means that the collector current is 50% or half of the LED current. CTR is of course not constant but depends on the LED current as well as on temperature. For many optocouplers CTR is specified for a nominal current of 5mA but can have considerably higher CTR at higher currents while being much lower at currents below 5 mA. Since CDM10V drives a constant current of 5 mA it fits very well to the most common couplers on the market. For a given coupler the CTR shows wide variation from device to device, varying for example from 50% to 600% for a

**Functional Description**

widely used coupler. Therefore selections are available with a CTR variation of 1:2 ranging e.g. from 100% to 200%.

As said before, the 4-pin coupler with phototransistor can be seen as a current-controlled current source and CDM10V is driving a current of 5 mA, resulting in a collector current (= emitter current) ranging from 2.5 mA to 30 mA for a non-selected coupler. With a 100 Ω load resistor the output signal thus would vary from 250 mV to 3V. This leads to the conclusion that small load resistance is desirable for good switching behavior but leads to small output signal and this signal varies too much with CTR instead of having a constant amplitude as requested initially. A solution for achieving constant amplitude could be to make the load resistance big enough that the transistor would go into saturation. The voltage drop across a BJT in saturation is small and doesn't vary much with temperature but switching speed is very poor in this condition.



**Figure 9 Simplified schematic showing second order filter and best configuration of coupler**

All of the above put together results in a set of simple rules of optocoupler selection:

1. Use the lowest PWM frequency that gives reasonable dimming response.  
Example: With  $f_{PWM} = 1\text{kHz}$  a second order filter with a corner frequency of 100 Hz should be used. The response time of this filter to a step from 10% to 90% dimming level is about 10 ms and after 20 ms the final level is reached.
2. Use an optocoupler with a selected CTR range like e.g. 100% to 200%.
3. Use a load resistance that allows the desired output voltage even with lowest CTR over all possible operating conditions.

Example:

$$CTR_{min} = 80\%, V_{Out} = 5\text{ V}, I_{LED, max} = 4.5\text{ mA}$$

$$R_L = \frac{V_{out}}{CTR_{min} \times I_{LED, min}} = \frac{5\text{ V}}{0.8 \times 4.5\text{ mA}} = 1.388\text{ k}\Omega$$

4. To prevent saturated switching, use a supply voltage  $V_{CC}$  that is at least 2V higher than the desired output voltage  $V_{Out}$ .  $V_{CC}$  shouldn't be too high on the other hand to limit power losses.

Example:

$$V_{CC} = 15\text{ V}, CTR_{max} = 200\%, I_{LED, max} = 5.45\text{ mA}, \text{Dimm-Level } 100\%$$

$$P_{Loss, max} = 2.2 \times 5.45\text{ mA} \times 15\text{ V} = 179.85\text{ mW}$$

Obviously with a  $V_{CC}$  of 7.5 V these losses would be halved to about 90 mW. It's important to keep in mind, that this is the maximum loss that only occurs at maximum light output. At minimum dimming level or dim-to-off the loss added by the optocoupler circuit will be negligible.

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**Functional Description**

5. Use a Zener diode to limit and stabilize the output voltage to the desired value. In the above example a 5.1 V Zener with 2% accuracy should be used.

A circuit that complies with all the above is shown in *Image*. An optocoupler device that complies with the above mentioned rules and has actually been tested in the application is VO617A-2 by Vishay Semiconductor. There are of course many devices available that have very similar, if not identical, technical data regarding switching times vs. load resistance and CTR selection. As an example devices as FOD817A, HCPL-817-xxAE or LTV-817A, EL817A or TLP183 GRL, to name only a few, can be used in this application. Nevertheless the desired performance has to be verified in the application in each single case.

**Electrical Characteristics and Parameters**

## 4 Electrical Characteristics and Parameters

**Table 5 Absolute Maximum Ratings**

Pin	Name	Values		Unit	Note or Test Condition
		Min.	Max.		
1	V <sub>CC</sub>	11	25	V	
2	GND	0	0	V	Point of reference
3	I <sub>out</sub>	-0.5	3.63	V	Depending on the optocoupler voltage @ 5mA
4	RxD	-0.25	0.1	V	Connect to GND during operation
5	V <sub>FSS</sub>	-0.25	0.1	V	During operation Connect to GND
6	R <sub>dim+</sub>	-0.5	V <sub>CC</sub> + 0.5	V	An applied voltage above max value leads to the destruction of the device. Also valid if V <sub>CC</sub> is 0 V.

Absolute maximum ratings (**Table 5**) are defined as ratings which when being exceeded may lead to destruction of the integrated circuit. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. These values are not tested during production test.

**Table 6 Electrical Characteristics**

Parameter	Programmable	Symbol	Values			Unit	Note or Test Condition
			Min.	Typ.	Max.		
Input Voltage		V <sub>in</sub>	11		25	V	Operating Voltage
Junction Temperature Range		T <sub>J</sub>	-40		135	°C	
Ambient Temperature Range		T <sub>A</sub>	-40		105	°C	
Power Dissipation		P <sub>tot</sub>	6.05 @ 1% duty cycle; 6.6 @ 2% duty cycle; 8.25 @ 5% duty cycle; 11 @ 10% duty cycle	130 @ 100% duty cycle 83.2 @ 70% duty cycle 54 @ 50% duty cycle 30.4 @ 30% duty cycle	160 @ 100% PWM & 25 V <sub>in</sub>	mW	Dimmer current included
Current Consumption		I <sub>CC</sub>			1	mA	Current Consumption of the IC for self supply

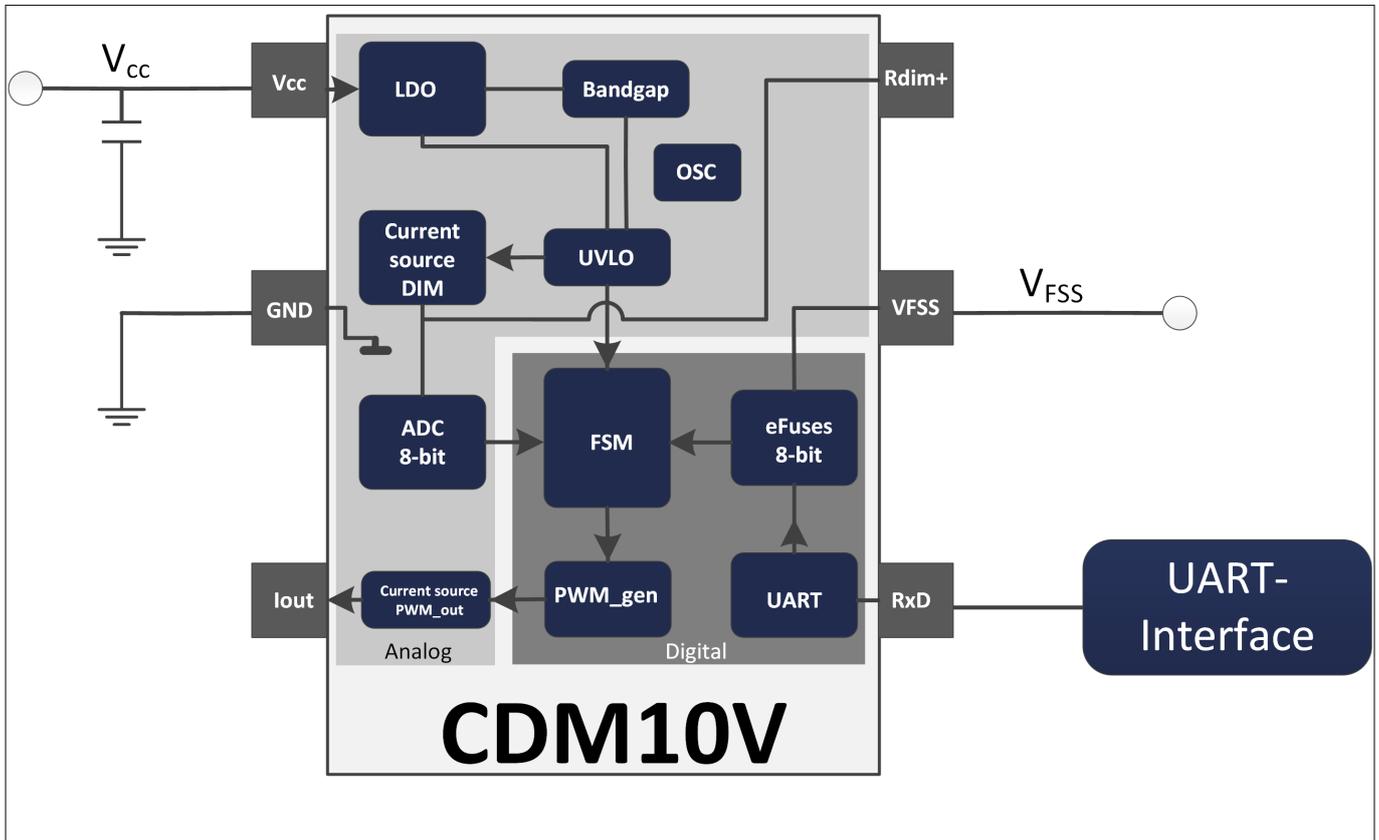
**Electrical Characteristics and Parameters**

**Table 6 Electrical Characteristics (continued)**

Parameter	Programmable	Symbol	Values			Unit	Note or Test Condition
			Min.	Typ.	Max.		
Output Current for Dimmer	yes	$I_{dim}$	-10%	50/100/200/500	+10%	$\mu\text{A}$	Current flow out of $R_{dim+}$ Pin
Output Current for Optocoupler		$I_{out}$	-10%	5	+10%	mA	
PWM frequency	yes	$f_{PWM}$	-6%	200/500/ 1000/2000	+6%	Hz	
Min. duty cycle	yes	$PW_{PWM}$	-0.2	1/2/5/10	+0.2	%	Percentage of the pulse width
Dimming accuracy			-3		+3	%	With active dimming incl. all variations
Fusing Voltage		$V_{FSS}$	4.0	4.1	4.2	V	For eFuse programming, connect to GND for normal operation
Wake-up Time		$t_w$			40	$\mu\text{s}$	Time from $V_{CC} = 11\text{ V}$ to first output current
ESD capability HBM		$V_{HAB}$			1500	V	according to ANSI/ESDA/ JEDEC JS-001
ESD capability CDM		$V_{CDM}$			500		according to JESD22 C101

## 5 Chip Configuration

### Typical eFuse programming Circuit



**Figure 10** Typical eFuse programming Circuit

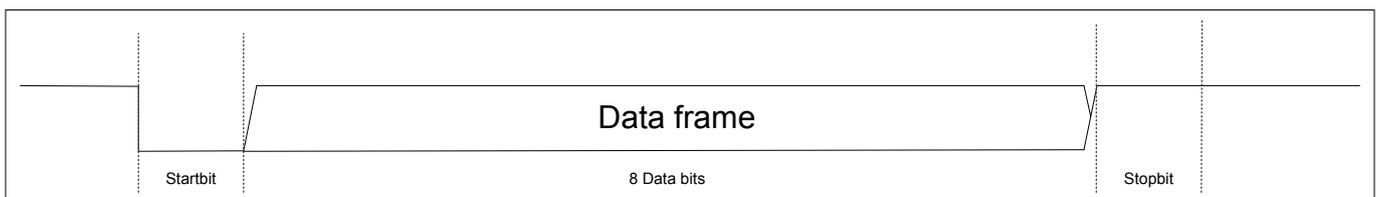
### Serial Port

The serial port enables a one time reconfiguration of parameters for device function.

Characteristics of the communication:

Baudrate: 9600Bd; one stop bit; no parity bit

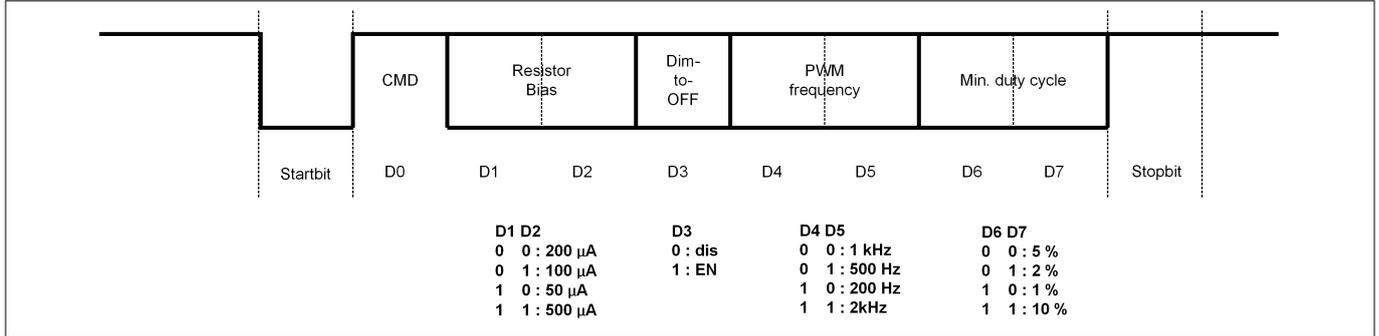
Timing diagram:



**Figure 11** Timing diagram for the serial communication

**Chip Configuration**

Data frame format:



**Figure 12 Data frame format for the Serial Communication**

**Table 7 Bit setting for the one time reconfiguration**

Bit group	Value	Meaning	Comment
CMD	1	Always high	reserved
Dimmer/Resistor Bias	00	<b>200 <math>\mu</math>A</b>	Default
	01	100 $\mu$ A	
	10	50 $\mu$ A	
	11	500 $\mu$ A	
Dim-to-Off	0	<b>NOT ENABLED</b>	Default
	1	Enable	
PWM Frequency	00	<b>1 kHz</b>	Default
	01	500 Hz	
	10	200 Hz	
	11	2 kHz	
Minimum duty cycle	00	<b>5 %</b>	Default
	01	2 %	
	10	1 %	
	11	10 %	



Package Dimensions

Footprint

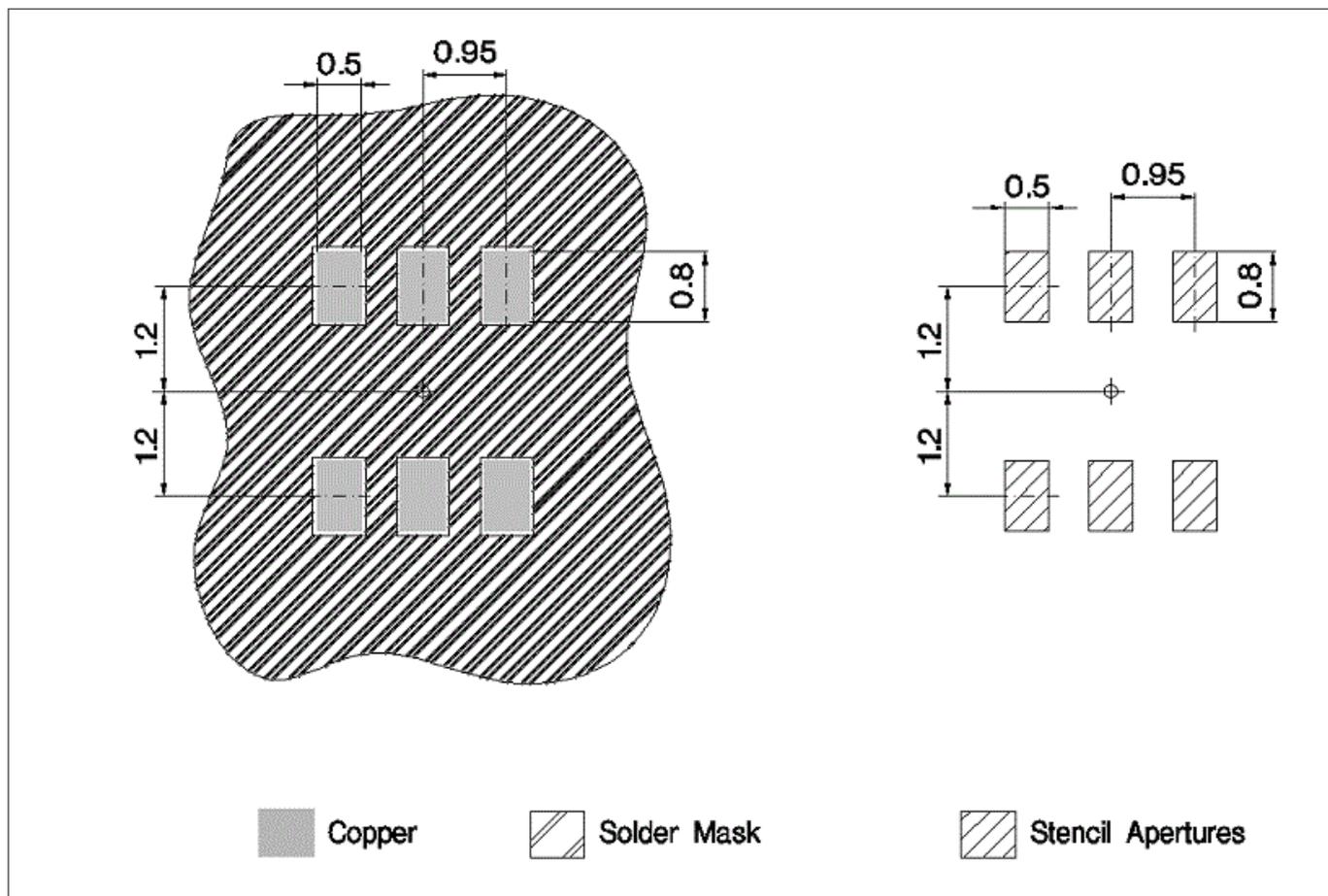


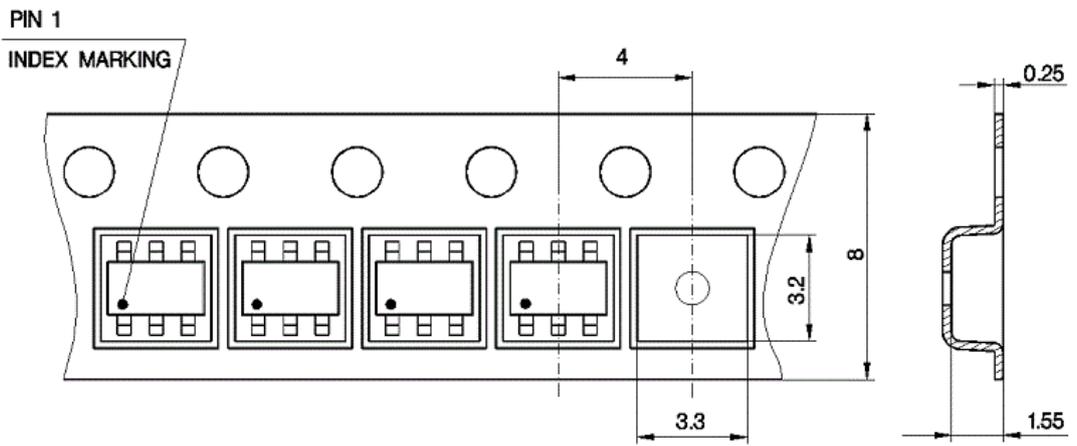
Figure 14 Footprint

**References**

**Packing Description**

**Packing Type**

Tape and Reel  
 Ø Reel: 180  
 Pieces / Reel: 3000  
 Reels / Box: 1



**Figure 15 Packing**

**7 References**

Additional support material can be found under the following link.

**Related information**

<http://www.infineon.com/CDM10V>

**Revision History**

Major changes since previous revision

**Revision History**

Reference	Description
v1.0	Initial Version
v1.1	Typos, added <a href="#">Table 5</a>
v1.2	Typos p 12, p 13
v1.3	Additional information about the max rating of Rdim-Pin ( <a href="#">Image</a> , <a href="#">Table 5</a> )

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