User manual for MERUS™ evaluation boards

EVAL_AUDIO_MA12070_B and EVAL_AUDIO_MA12070P_B

About this document

Scope and purpose

This user manual describes the EVAL_AUDIO_MA120xxx_B evaluation and demonstration board for **MA12070** and **MA12070P** proprietary multilevel amplifiers.

Intended audience

Audio amplifier design engineers

Attention: ***Please read through this user manual before operating the board. When powering up the board make sure to follow the instructions in the "Start sequence" section.***

Attention: ***Please observe proper electrostatic discharge (ESD) handling procedures. Failure to do so may result in damage to components on the board.***

Table of contents

1 Overview

This is an evaluation and demonstration board for MERUS™ audio MA12070 and MA12070P amplifiers.

It contains a variety of digital/analog input, output and setup/selection features. It also contains two onboard power supply generators (5 V and 3.3 V buck-converted) so only one external power supply (PVDD) is necessary.

The board can be used for evaluating or demonstrating key features/advantages of the MERUS™ technology:

- Energy efficiency
  - Power losses at normal user operating conditions (listening levels)
  - Idle power loss
- Adaptive power management system
- No output filter components
  - Solution cost and size reduction
- Audio performance
  - Total harmonic distortion (THD) performance and audio quality

1.1 Board features and audio performance

• Number of audio channels	2 x BTL, 1 x BTL + 2 x SE, 4 x SE
• Audio input format	
– MA12070	Analog
– MA12070P	Digital (I^2S)
• Amplifier gain	20 dB/Configurable 26 dB
• Supply voltage	PVDD
– Max. PVDD for MA12070/MA12070P	26 V
• Output noise level	
– MA12070	Less than 100 μV_{rms} (AW)
– MA12070P	Less than 150 μV_{rms} (AW)
• Dynamic range	
– MA12070	More than 100 dB
– MA12070P	More than 95 dB
• Idle consumption at PVDD = 18 V	
– MA12070	Less than 16 mA*
– MA12070P	Less than 19 mA*
• Crosstalk	Less than -85 dB
• Efficiency, full-scale, 8 Ω	91 percent

Note: *Idle consumption is the sum of output stage current and 5 V supply and 3.3 V supply current. As all the supplies are tied to PVDD, the efficiency of the buck-converted 5 V and 3.3 V should be considered when measuring idle current consumption directly from PVDD. Features on the EVK make it possible to break the 5 V and 3.3 V supply lines after the buck converters (see Table 1). Please refer to the MA12070/P device datasheet for exact current figures.*

1.2 EVK device type

The type of device (MA12070 or MA12070P) on the EVK is printed on the top of the board and is also stated on the serial number label on the bottom side of the EVK PCB.

2 Setup guide

Equipment required for operating and evaluating:

- Single power supply for PVDD
- Analog audio source or signal generator with line-level output (MA12070)
- Digital I²S audio source (MA12070P)
- Cables for input and output connectors
- Audio analyzer with measurement filter

2.1 Connections and interfaces

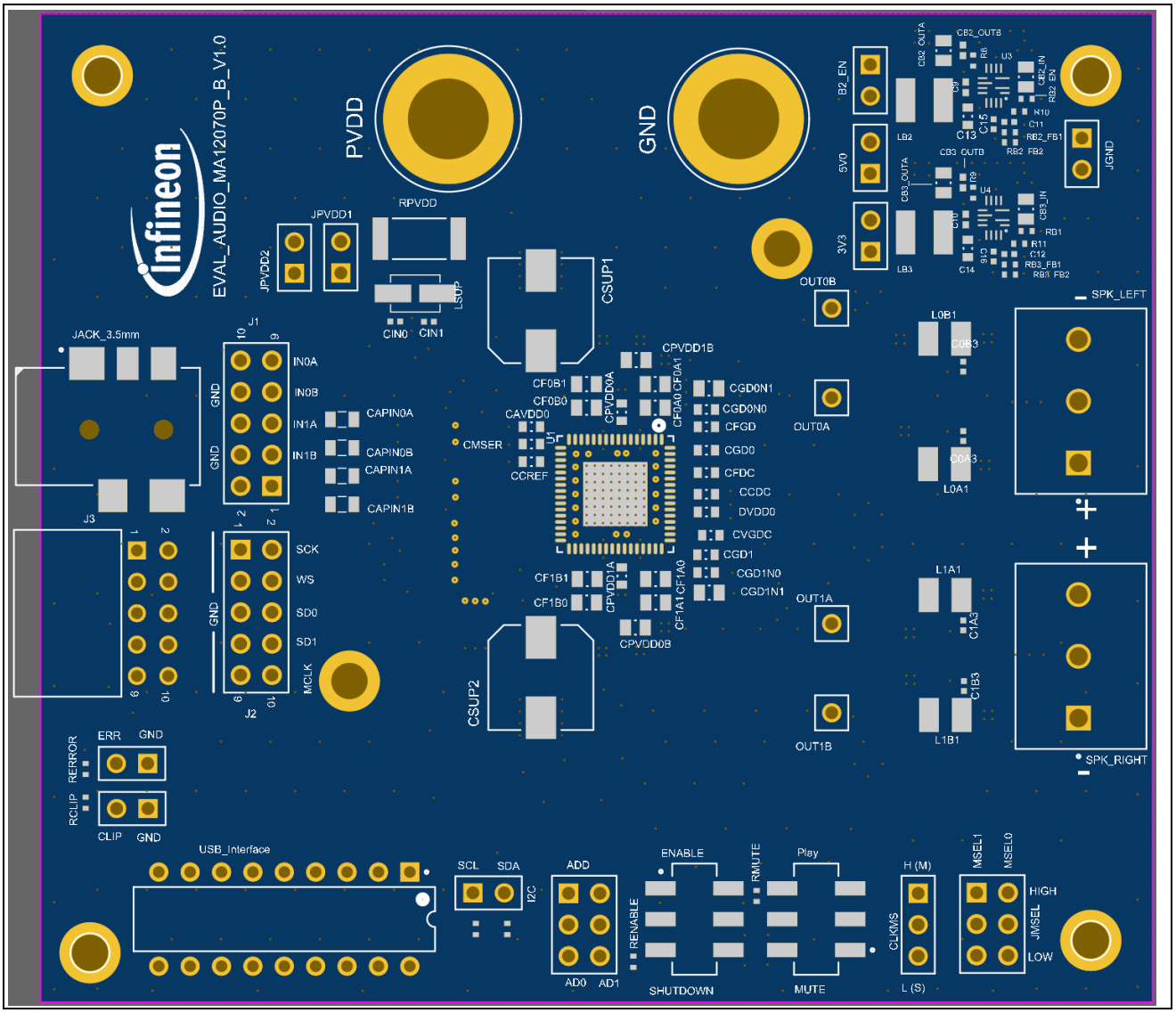

Figure 1 Top block view of EVK board

*Note: For schematic: see **Figure 5** on page 15.*

Table 1 EVK headers and connectors

Name	Schem. ref.	Description	Comment
MSEL0	JMSEL	Selects in conjunction with MSEL1 the output configuration (see Table 2).	Default: 2CH BTL. Jumpered high (H).
MSEL1	JMSEL	Selects in conjunction with MSEL0 the output configuration (see Table 2).	Default: 2CH BTL. Jumpered low (L).
/CLIP	CLIP	Audio clipping indicator (open drain output), pulled low when clipping occurs.	I/O pin. Do not jumper.
/ERROR	ERR	Error indicator (open drain output), pulled low when an error occurs.	I/O pin. Do not jumper.
CLKMS	CLKMS	Selects clock mode.	M = Master clock (non-P versions). S = Slave (external) clock (P versions).
AD0 AD1	ADD	Selects I²C address (see Table 3).	Default: I²C address 0B100000. Both jumpered low (GND).
B2_EN	B2_EN	When removed, enables 5 V and 3.3 V supply buck converters.	Default: Not jumpered (enabled)
PVDD MEAS	JPVDD1	Breaks PVDD for PVDD current measurements.	Default: Jumpered. Parallel with JPVDD2.
PVDD MEAS	JPVDD2	Breaks PVDD for current measurements.	Default: Jumpered. Parallel with JPVDD1.
5V MEAS	5V0	Breaks 5 V supply for 5 V circuit current measurements.	Default: Jumpered.
3V3 MEAS	3V3	Breaks 3.3 V supply for 3.3 V circuit current measurements.	Default: Jumpered.
GND GND	JGND	Two ground connections.	Default: Not jumpered.
SCL SDA	I2C	I²C bus serial clock and data.	I/O pin. Do not jumper.
CH0	SPK_LEFT	Channel0 speaker connection.	Three-way screw terminal with positive and negative speaker outputs. Center GND.
CH1	SPK_RIGHT	Channel1 speaker connection.	Three-way screw terminal with positive and negative speaker outputs. Center GND.
JACK	JACK_3.5mm	Single-ended, stereo analog audio input.	Tip = CH0. Ring = CH1. Sleeve = GND.
DIGITAL AUDIO1	J2	I²S digital audio input. Note: See Section 2.2 for setting up.	I/O pins. Do not jumper.

Name	Schem. ref.	Description	Comment
ANALOG AUDIO	J1	Balanced analog audio input connector. Also selects “JACK” input Note: See Section 2.2 for setting up	Jack input = All Jumpered Balanced input = Use pins for balanced analog audio input Note: Should NOT be jumpered for P (digital audio) versions
PVDD	PVDD	External power supply POSITIVE terminal	PVDD: +26 V max. (MA12070/-P)
GND	GND	External power supply GND terminal	GND
DIGITAL AUDIO2	J3	I^2S digital audio input Note: See Section 2.2 for setting up	I/O pins. Do not jumper.
OUT0A	OUT0A	Direct connection to device output node vsw_a0	Output measuring pin
OUT0B	OUT0B	Direct connection to device output node vsw_b0	Output measuring pin
OUT1B	OUT1B	Direct connection to device output node vsw_b1	Output measuring pin
OUT1A	OUT1A	Direct connection to device output node vsw_a1	Output measuring pin

Table 2 Signal configuration (JMSEL)

MSEL0	MSEL1	Configuration
L	L	Single-channel parallel bridge-tied load (PBTL)
L	H	Dual-channel single-ended (SE) load and single-channel bridge-tied load (BTL)
H	L	Dual-channel BTL
H	H	Four-channel SE load

Table 3 I²C address decoding (ADD)

I²C device address	AD0	AD1	7-bit I²C address
0x20	L	L	0b0100000
0x21	L	H	0b0100010
0x22	H	L	0b0100001

2.2 Notes to digital audio and analog audio headers

When using the “digital audio header” for digital I²S input stream (MA12070P), the connection scheme should appear as follows (from top to bottom, left side of the header):

- SCK: Word clock; also known as bit clock
- WS: Word select; also known as left right clock (LRCLK)
- SD0: Multiplexed data line 0 containing two digital input stream channels
- SD1: Multiplexed data line 1 containing two digital input stream channels
- MCLK: Master clock (typically 256 x fs)

When using analog input, the board has been set up to initially evaluate with an unbalanced input source (see “analog audio header”, jumpers connected). However, for full system performance evaluation it is recommended to apply a balanced analog input signal. This can be done by removing the four jumpers from the “analog input header” and connecting the analog balanced input signal as follows (from top to bottom, left side of the header):

- CH0 input in0a (+)
- CH0 input in0b (-)
- CH1 input in1a (+)
- CH1 input in1b (-)

3 Operating the demonstration board

3.1 Recommended operating conditions

Table 4 Recommended operating conditions

	Minimum	Nominal	Maximum	Unit
PVDD (MA12070/MA12070P)	5.5		26	V
Output peak current (MA12070/MA12070P)			8.0	A

3.2 Toggle switches

The board has two toggle switches. The toggle switches have the following functions:

Table 5 Switch function

	Function
Switch 1	Shutdown/Enable (default set to “shutdown”)
Switch 2	Mute/Play (default set to “mute”)

3.3 Speaker load

The demonstration board is configured as a filterless amplifier. This means that no LC filter is placed between the amplifier outputs and the load. In normal use the amplifier relies on the inherent inductance of the loudspeaker and therefore no extra inductance is needed.

Inductors for use in series with power resistors are included with the demonstration board. These can be used when making any measurements without a real loudspeaker as the load, and having no external low-pass filter (LPF) in front of the audio analyzer input section.

Please note that many audio measurement analyzers do not perform correctly when connected directly to a filterless amplifier output.

3.4 GUI

The demonstration board is used with graphical user interface (GUI) PC software to control the MA12070/P device. The GUI software is included with the demonstration board and runs on Windows PCs.

Unzip the file package on your PC in your preferred location. See the next section for the correct start-up sequence including starting the GUI.

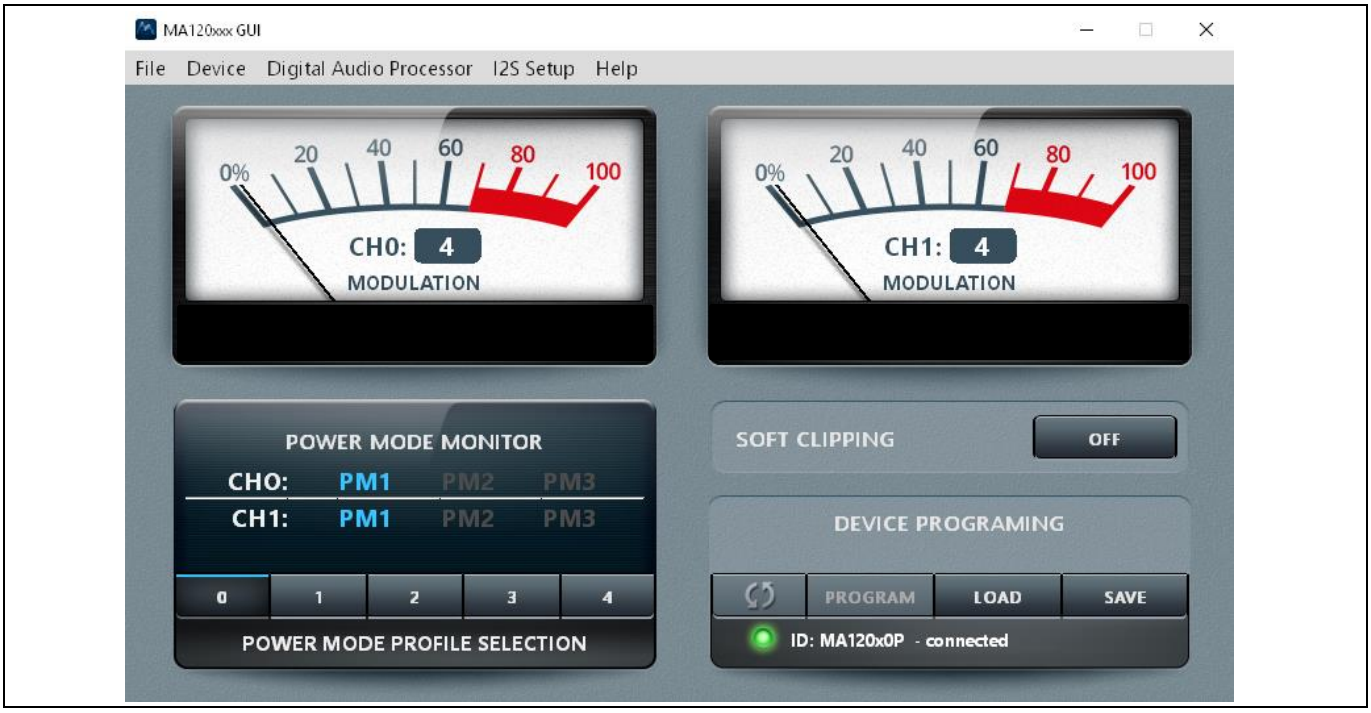

Figure 2 GUI main window

By default the MA12xx/P will automatically select the relevant power mode (PM1, PM2 or PM3), based on detection of audio level during operation. The selected power mode is indicated by a blue color in the power mode indicator.

A set of sliders are available above the power mode indicator. The first slider is used for setting the levels for transitions between PM1 and PM2. When setting the values at higher levels the transition from PM1 to PM2 will occur at a higher output power level. The second slider is used in the same way, for transitions between PM2 and PM3.

Power mode profiles can be selected in the “Power Mode Profile Select” section. This gives a specific profile to the amplifier for optimization on low idle power consumption, audio performance or EMI. Please refer to the specific device datasheet for more detailed information on power mode profiles.

The “Digital Audio Processor” button is for digital input (I^2S) use and will be discussed in the start-up section for I^2S configuration. Note that the digital audio processor part of the GUI can only be used with MA12070P devices.

3.5 Start sequence

Important – GUI software revisions: The current GUI software version is 6.5.0. Please note that the current GUI only accepts I^2C address 0x20.

3.6 Analog input configuration (MA12070 devices)

Follow this (recommended) sequence to start the EVK:

1. Make sure toggle buttons are in “shutdown” and “mute” positions.
2. Connect all cables, including the PC by USB cable.
3. Make sure active analog audio source is connected.
4. Turn on the PVDD supply.
5. Start the board by setting the toggle switch to the “enable” position.

6. Start the GUI software by running the executable file to monitor device status.
7. Make sure the GUI indicates a valid device ID and connection status (bottom right GUI).
8. Start playing music by setting the toggle switch to the “play” position.
9. Additional “optimized” settings can be programmed to the device: Hit “Load” → select config file in configs subfolder → hit “Program”.

Mute and turn off the PVDD power supply.

3.7 Digital (I^2S) input configuration (MA12070P devices)

Follow this (recommended) sequence to start the board:

1. Make sure toggle buttons are in “shutdown” and “mute” positions.
2. Connect all cables, including the PC by USB cable.
3. Connect I^2S to the I^2S audio input header.
4. Make sure the clock select jumper is set to “slave” mode.
5. Turn on the PVDD power supply.
6. Make sure the I^2S master clock is present before enabling the amplifier.
7. Start the board by setting the toggle switch to the “enable” position.
8. Start the GUI software by running the “MA Device GUI 6.5.0.exe” file.
9. Make sure the GUI indicates a valid device ID and connection status (bottom right GUI).
10. Open the “Digital Audio Processor” in the GUI.
11. In the DAP window check “Digital audio enable” and “Audio processor enable”.
12. The I^2S set-up window will open when clicking “I2S setup”. The correct I^2S settings should be set here.
13. Start playing sound by setting the toggle switch to the “play” position.
14. Additional “optimized” settings can be programmed to the device: Hit “Load” → select config file in configs subfolder → hit “Program”.

Mute and turn off the PVDD power supply.

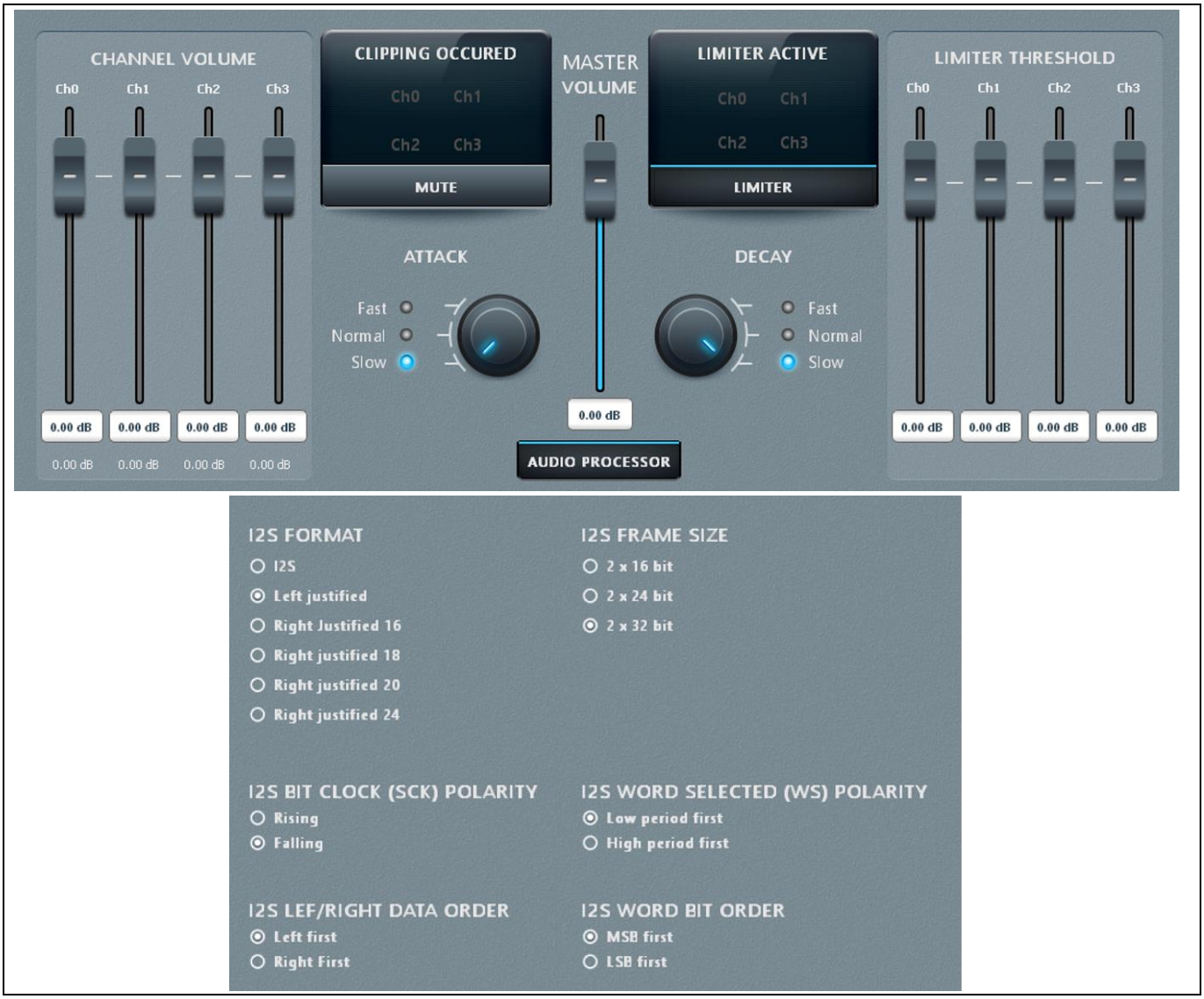

Figure 3 Digital audio processing window (top) and I²S setup window (bottom)

4 Measurement methods

Setting up a reliable measurement configuration for MA12070 or MA12070P takes a little bit more effort than linear amplifiers and even “regular” switching amplifiers. This is mainly because MA12070 and MA12070P are filterless amplifiers, which means they do not require an external (usually expensive and bulky) LC filter to remove switching residuals. The filterless application is enabled by the MERUS™ audio multilevel technique, which makes sure that the switching residual is orders lower compared to “regular” switching amplifiers. For more information on the multilevel switching technique, please refer to the datasheet.

To obtain reliable measurement results when measuring MA12070 or MA12070P devices requires a separate external LPF in front of the input stage of the audio analyzer. Most audio analyzers are bandwidth limited at their input stage, which means that they cannot follow the rapid changes of the amplifier’s output stage. This can result in inaccurate and high THD + N measurements.

Figure 4 shows the recommended measurement setup. The setup shows an LPF stage (AUX-2500) in front of the audio analyzer (APX-515). In this case the measurement setup has been built around Audio Precision hardware, but this can also be some other audio analyzer hardware. Please note that it is recommended to use both balanced input and output measurement configurations. Note that **Figure 4** shows the setup for analog input (MA12070). To use the setup for digital input (MA12070P), simply replace the balanced analog input path with the I^2S input path.

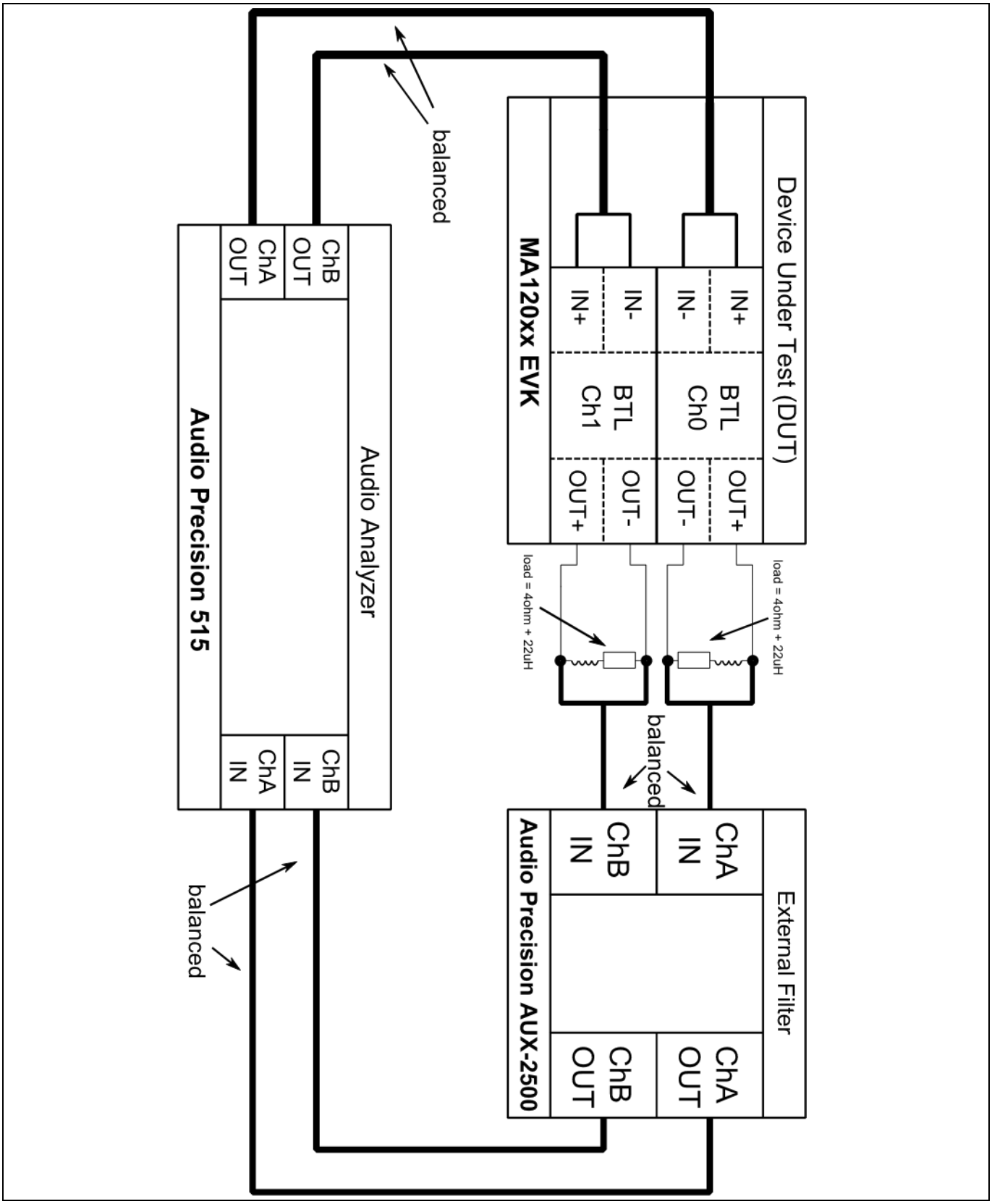

Figure 4 Recommended measurement setup for analog input (MA12070)

5 EVK schematic

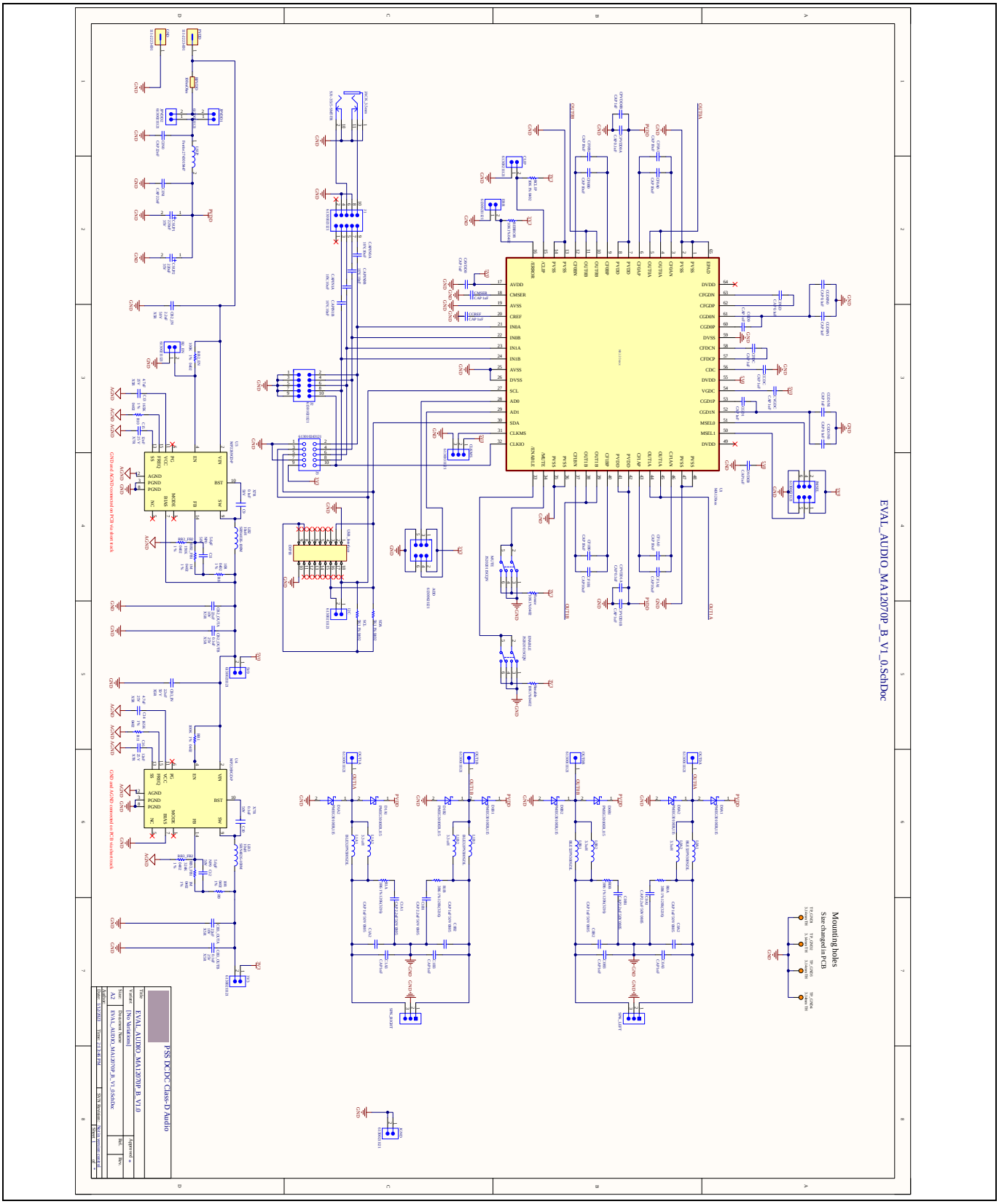

Figure 5 EVK schematic

6 EVK PCB layout

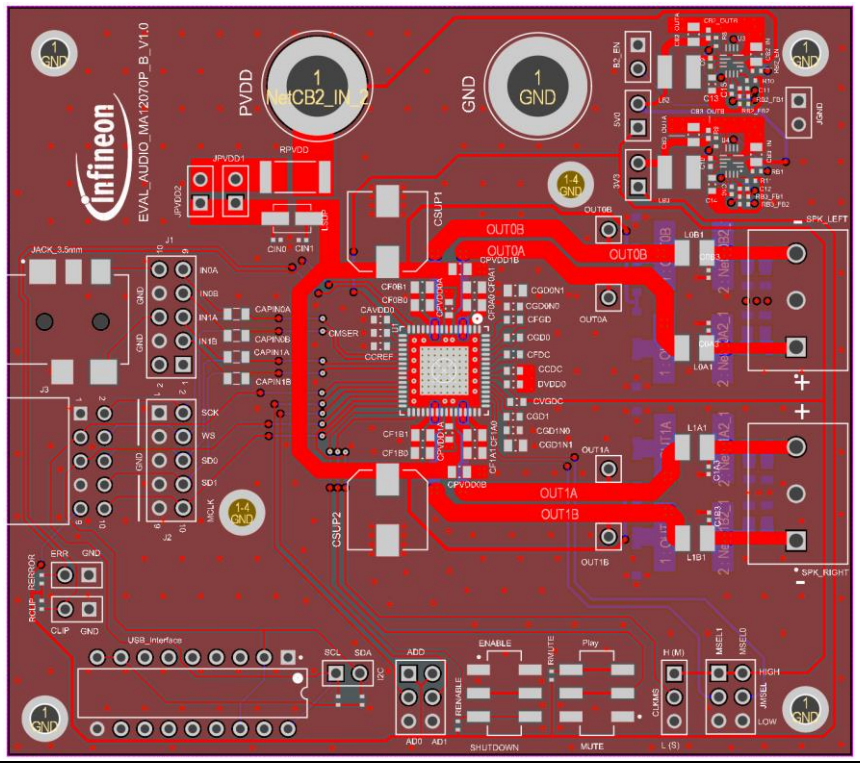

Figure 6 PCB layout (top x-ray view)

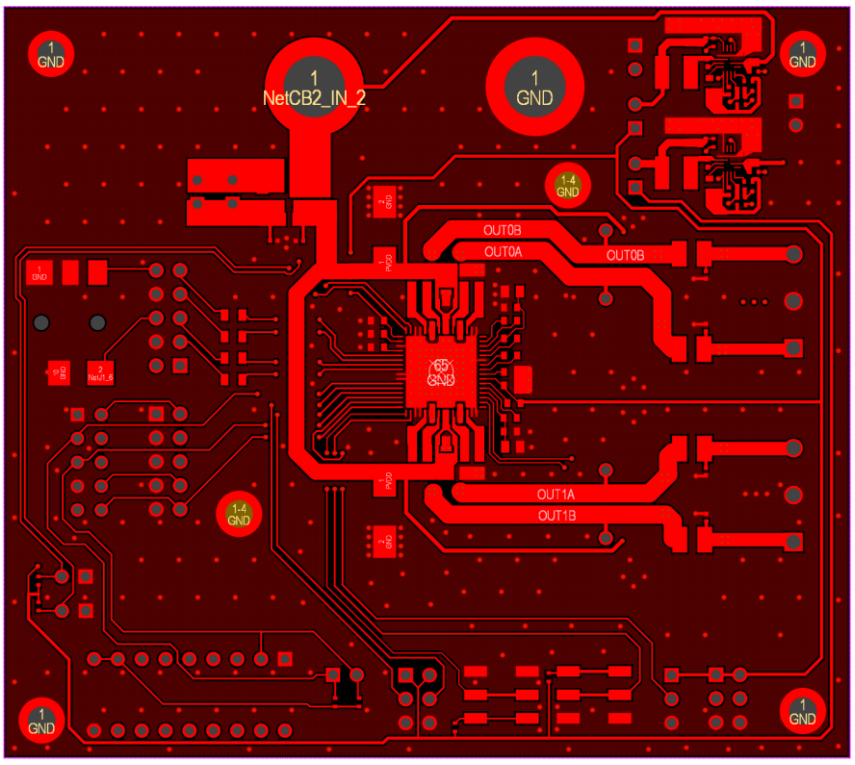

Figure 7 PCB layout (top layer)

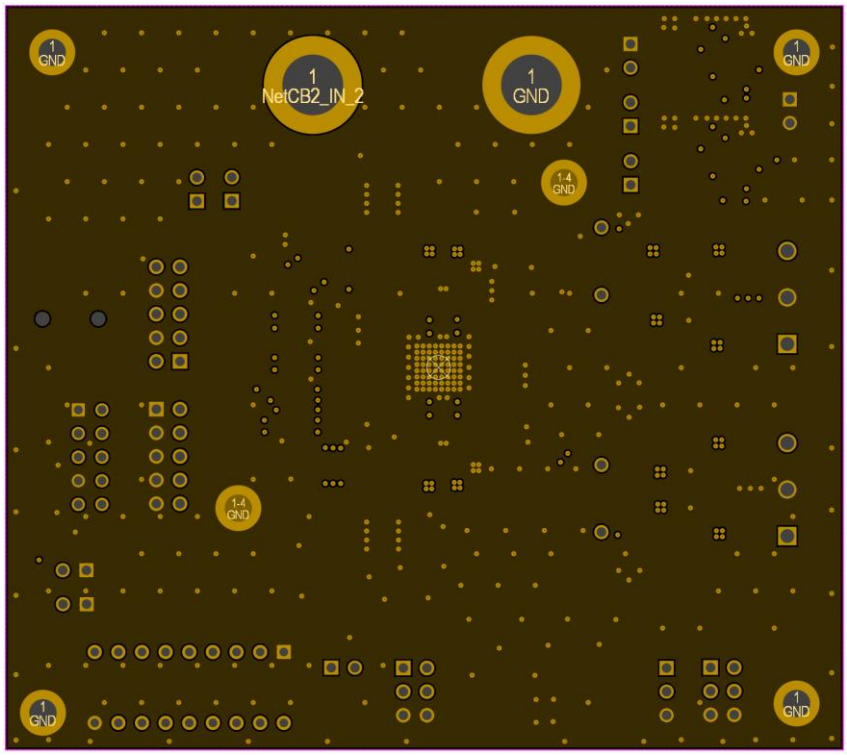

Figure 8 PCB layout (layer 1)

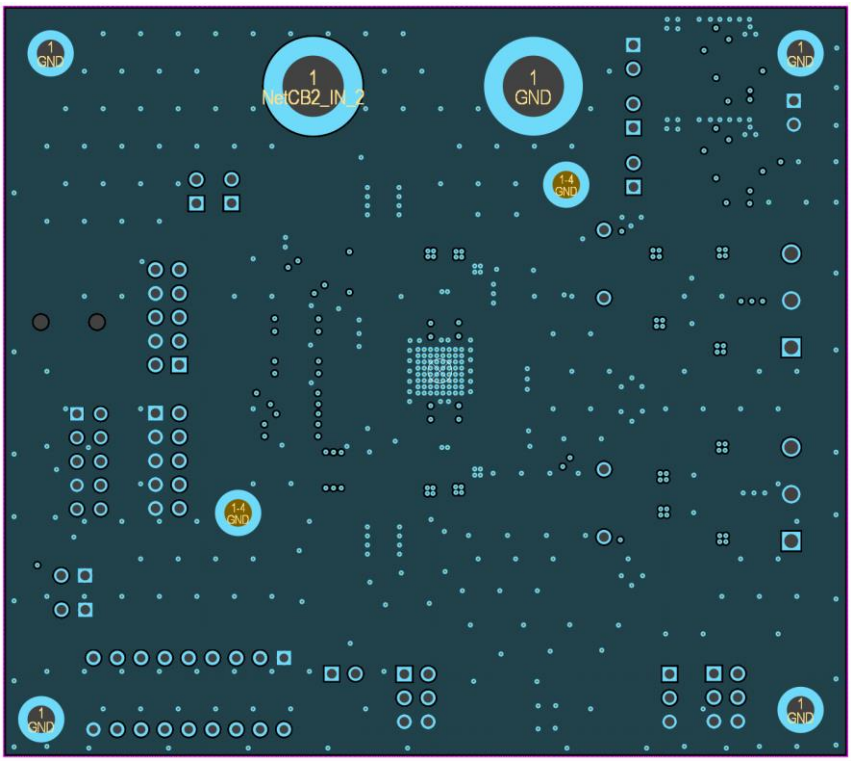

Figure 9 PCB layout (layer 2)

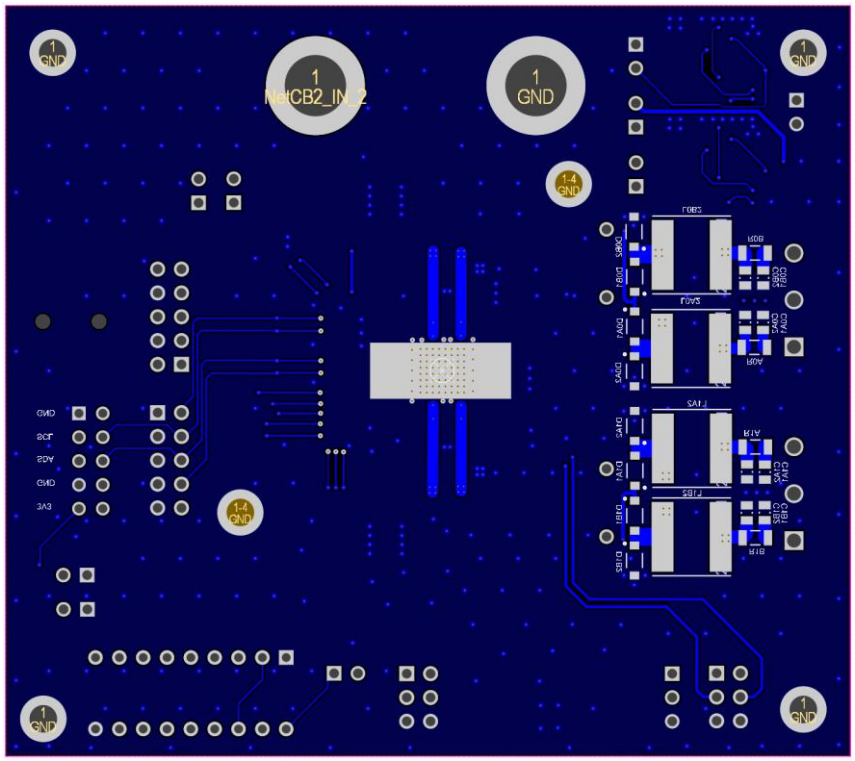

Figure 10 PCB layout (bottom layer)

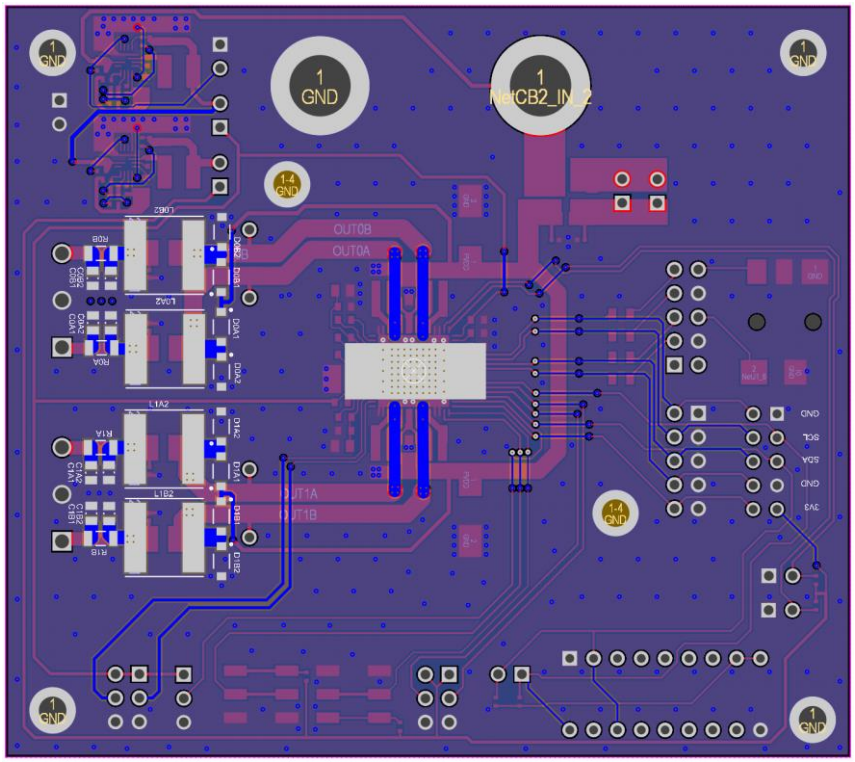

Figure 11 PCB layout (bottom x-ray view, mirrored)

7 Bill of materials (BOM)

Table 6 BOM

S. no.	Reference	Qty	Description	Manufacturer	Part number
1	3V3, 5V0, B2_EN, CLIP, ERR, I2C, JGND, JPVDD1, JPVDD2	9	THT vertical pin header WR-PHD, pitch 2.54 mm, single row, 2 pins	Würth Elektronik	61300211121
2	ADD, JMSEL	2	THT vertical pin header WR-PHD, pitch 2.54 mm, dual row, 6 pins	Würth Elektronik	61300621121
3	C0A3, C0B3, C1A3, C1B3	4	Capacitor, 1000 pF, ±10%, X7R, 50 V, 0402 [1005 metric]	TDK	C1005X7R1H102K050BA
4	C9, C10	2	Ceramic capacitor, 0.1 µF, 50 V, X7R, 0402	Murata Electronics	GRM155R71H104KE14D
5	C11, C12	2	Ceramic capacitor, 5.6 pF, 50 V, C0G/NP0, 0402	Samsung Electro-Mechanics	CL05C5R6DB5NNNC
6	C13, C14	2	Ceramic capacitor, 4.7 µF, 25 V, X5R, 0603	Samsung Electro-Mechanics	CL10A475KA8NQNC
7	C15, C16	2	Ceramic capacitor, 12 nF, 25 V, X7R, 0402	Murata Electronics	GCM155R71E123KA55J
8	CAPIN0A, CAPIN0B, CAPIN1A, CAPIN1B	4	WCAP-CSGP ceramic capacitors, 0805, X7R, 10 V, 10 µF	Würth Elektronik	885012207026
9	CAVDD0, CCDC, CCREF, CFDC, CGD0, CGD1, CMSER, CVGDC, DVDD0	9	Capacitor, 1 µF, ±10%, X7R, 25 V, 0603 [1608 metric]	Multicomp	MC0603X105K250CT
10	CB2_IN, CB3_IN	2	Ceramic capacitor, 2.2 µF, 50 V, X5R, 0805	Samsung Electro-Mechanics	CL21A225KBQNNNE
11	CB2_OUTA, CB3_OUTA	2	Ceramic capacitor, 22 µF, 10 V, X5R, 0805	Samsung Electro-Mechanics	CL21A226MPCLRNC
12	CB2_OUTB, CB3_OUTB	2	Ceramic capacitor, 0.1 µF, 25 V, X5R, 0402	Samsung Electro-Mechanics	CL05A104KA5NNND
13	CF0A0, CF0A1, CF0B0, CF0B1,	8	Capacitor, 10 µF, ±10%, X5R, 25 V,	TDK	TMK212BBJ106MG-T

S. no.	Reference	Qty	Description	Manufacturer	Part number
	CF1A0, CF1A1, CF1B0, CF1B1		0805 [2012 metric]		
14	CFGD, CGD0N0, CGD1N0, CPVDD0A, CPVDD1A	5	Capacitor, 0.1 µF, ±10%, X7R, 50 V, 0603 [1608 metric]	Multicomp	MC0603B104K500CT
15	CGD0N1, CGD1N1, CPVDD0B, CPVDD1B	4	Capacitor, 1 µF, 50 V, ±10%, X5R, 0805 [2012 metric]	Multicomp	MC0805X105K500CT
16	CIN0, CIN1	2	Capacitor, 0.022 µF, ±10%, X7R, 50 V, 0402 [1005 metric]	Murata	GRM155R71H223KA12D
17	CLKMS	1	THT vertical pin header WR-PHD, pitch 2.54 mm, single row, 3 pins	Würth Elektronik	61300311121
18	CSUP1, CSUP2	2	SMD aluminum electrolytic capacitor, 330 µF, 35 V, EEE-FN1V331UV	Multicomp Pro	MCESL35V227M8X10.5
19	ENABLE, MUTE	2	Switch slide DPDT, 0.3 A, 6 V	C&K Components	JS202011SCQN
20	GND, PVDD	2	Binding post uninsulated with knurled thumb-nut-grounded type	Cinch	111-2223-001
21	J1, J2	2	THT vertical pin header WR-PHD, pitch 2.54 mm, dual row, 10 pins	Würth Elektronik	61301021121
22	J3	1	THT angled socket header WR-PHD, pitch 2.54 mm, dual row, 10 pins	Würth Elektronik	613010243121
23	JACK_3.5mm	1	Audio jack, 5 pins	CUI	SJ1-3515-SMT-TR
24	L0A1, L0B1, L1A1, L1B1	4	Murata ferrite bead, size 1210, 30 Ω, 10 A	Murata Electronics	BLE32PN300SZ1L
25	LB2, LB3	2	SRN4026-150M	Bourns	SRN4026-100M
26	LSUP	1	SMD power bead ferrite, Z = 47 Ω	Fair-Rite	2743019447
27	OUT0A, OUT0B, OUT1A, OUT1B	4	THT vertical pin header WR-PHD, pitch 2.54 mm, single row, 1 pin	Würth Elektronik	61300111121
28	R8, R9	2	Resistor SMD, 10 Ω,	Vishay/Dale	CRCW040210R0FKEE

S. no.	Reference	Qty	Description	Manufacturer	Part number
			1%, 1/16 W, 0402		
29	R10, R11	2	Resistor 165 kΩ, 1%, 1/16 W, 0402	Yageo	RC0402FR-07165KL
30	RB1, RB2_EN	2	Resistor, 100 kΩ, 1%, 1/16 W, 0402	Yageo	RC0402FR-07100KL
31	RB2_FB1, RB3_FB1	2	Resistor 1M OHM 1% 1/16W 0402	Vishay/Dale	CRCW04021M00FKEDC
32	RB2_FB2	1	Resistor SMD, 191 kΩ, 1%, 1/16 W, 0402	Vishay/Dale	CRCW0402191KFKED
33	RB3_FB2	1	Resistor SMD, 324 kΩ, 1%, 1/16 W, 0402	Vishay/Dale	CRCW0402324KFKTD
34	RCLIP, R_{enable}, RERROR, R_{mute}	4	10k, 0.063 W, 1%, 0402 (1005 metric) SMD	Walsin	WR04X1002FTL
35	RPVDD	1	SMD low-value flat-chip resistor	Vishay/Dale	RCWE2512R100FKEA
36	SCL, SDA	2	5K1, 0.063 W, 1%, 0402 (1005 metric) SMD	Yageo	RC0402FR-075K1L
37	SPK_LEFT, SPK_RIGHT	2	Screw terminal block, 3 way, 5.0 mm pitch TH	TE Connectivity	796911-3
38	U1	1	Multilevel class D amplifier	Merus Audio	MA12070 or MA12070P
39	U3, U4	2	IC programmable buck regulator, 1 A	Monolithic Power Systems	MP2269GD-P
40	USB_Interface	1	DIP socket, 18 pins, 2.54 mm pin spacing, 7.62 mm row spacing	TE Connectivity	1-2199298-5

Revision history

Document version	Date of release	Description of changes
V 1.0	2023-03-02	Initial release

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