International
IOR Rectifier

February 18, 2009

IRS211(7,71,8)(S)

SINGLE CHANNEL DRIVER

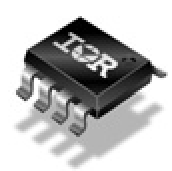
IC Features

- Floating channel designed for bootstrap operation
- Fully operational to +600V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20V
- Undervoltage lockout
- CMOS Schmitt-triggered inputs with pull-down
- Output in phase with input
- RoHS compliant
- IRS2117 and IRS2118 available in PDIP8

Product Summary

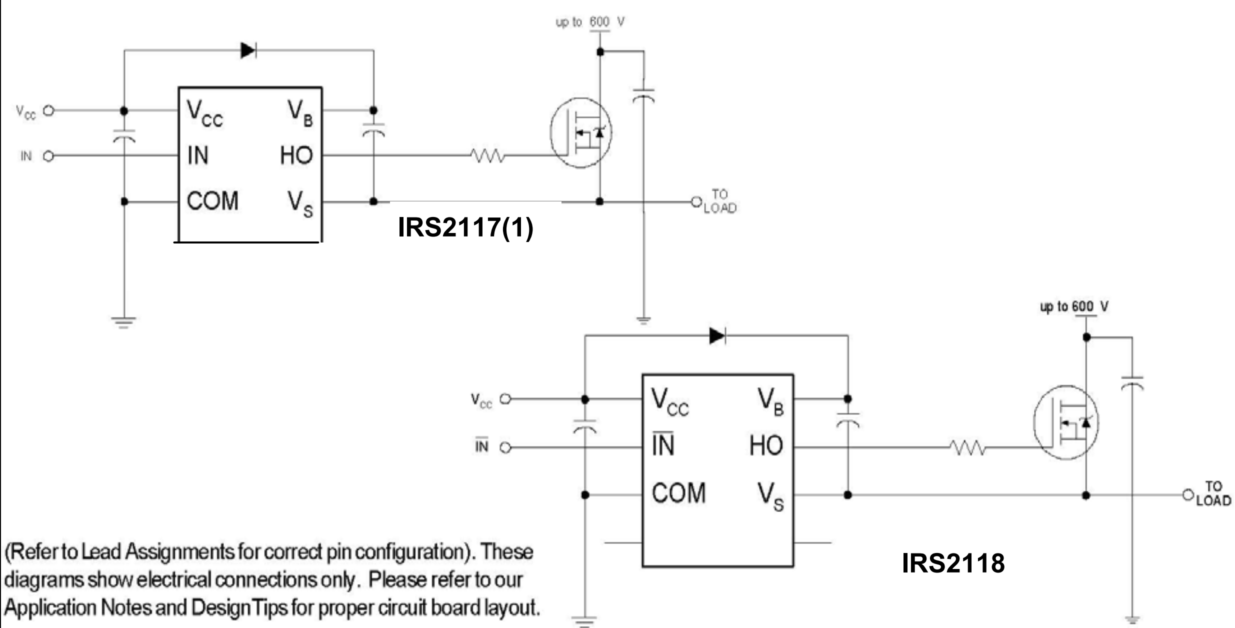
Topology		Single High Side
V_{OFFSET}		600 V
V_{OUT}		10V-20 V
I_{O+} & I_{O-} (typical)		290 mA & 600 mA
IN voltage threshold	IRS211(7,8)	9.5 V & 6 V
	IRS21171	2.5 V & 0.8 V

Package Type



SOIC8

PDIP8



(Refer to Lead Assignments for correct pin configuration). These diagrams show electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

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Description

The IRS2117, IRS21171, and IRS2118 are high voltage, high speed power MOSFET and IGBT driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized mono-lithic construction. The logic input is compatible with standard CMOS outputs. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side or low-side configuration which operates up to 600 V.

Qualification Information[†]

Qualification Level		Industrial[††] (per JEDEC JESD 47)	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOIC8	MSL2[†††] 260°C (per IPC/JEDEC J-STD-020C)
		PDIP8	Not applicable (non-surface mount package style)
ESD	Machine Model	Class B (per JEDEC standard EIA/JESD22-A115)	
	Human Body Model	Class 3A (per EIA/JEDEC standard JESD22-A114)	
IC Latch-Up Test		Class I, Level A (per JESD78)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating supply voltage		-0.3	625	V
V_S	High-side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High-side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Logic supply voltage		- 0.3	25	
V_{IN}	Logic input voltage		- 0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient (fig.2)		---	50	V/ns
P_D	Package power dissipation @ $T_A \le +25^{\circ}C$	8 lead SOIC	---	0.625	W
		8 lead PDIP		1.0	
$R_{\theta JA}$	Thermal Resistance, junction to Ambient	8 lead SOIC	---	200	ºC/W
		8 lead PDIP		125	
T_J	Junction temperature		---	150	ºC
T_S	Storage temperature		-55	150	
T_L	Lead Temperature (soldering, 10 seconds)		---	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The VS offset rating is tested with all supplies biased at 15 V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High-Side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High-side floating supply offset voltage	†	600	
V_{ST}	Transient High side floating supply offset voltage	-50 (††)	600	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Logic supply voltage	10	20	
V_{IN}	Logic input voltage	0	V_{CC}	
T_A	Ambient Temperature	-40	125	ºC

† Logic operational for V_S of -5 V to +600 V. Logic state held for V_S of -5 V to – V_{BS}.

†† Operational for transient negative VS of COM - 50 V with a 50 ns pulse width. Guaranteed by design. Refer to the Application Information section of this datasheet for more details.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, C_L = 1000 pF and T_A = 25 °C unless otherwise specified.

Symbol	Definition		Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	IRS21171	---	160	230	ns	V_S = 0V
		IRS211(7,8)	---	125	200		
t_{off}	Turn-off propagation delay	IRS21171	---	160	230		V_S = 600V
		IRS211(7,8)	---	105	180		
t_r	Turn-on rise time		---	75	130		
t_f	Turn-off fall time		---	35	65		

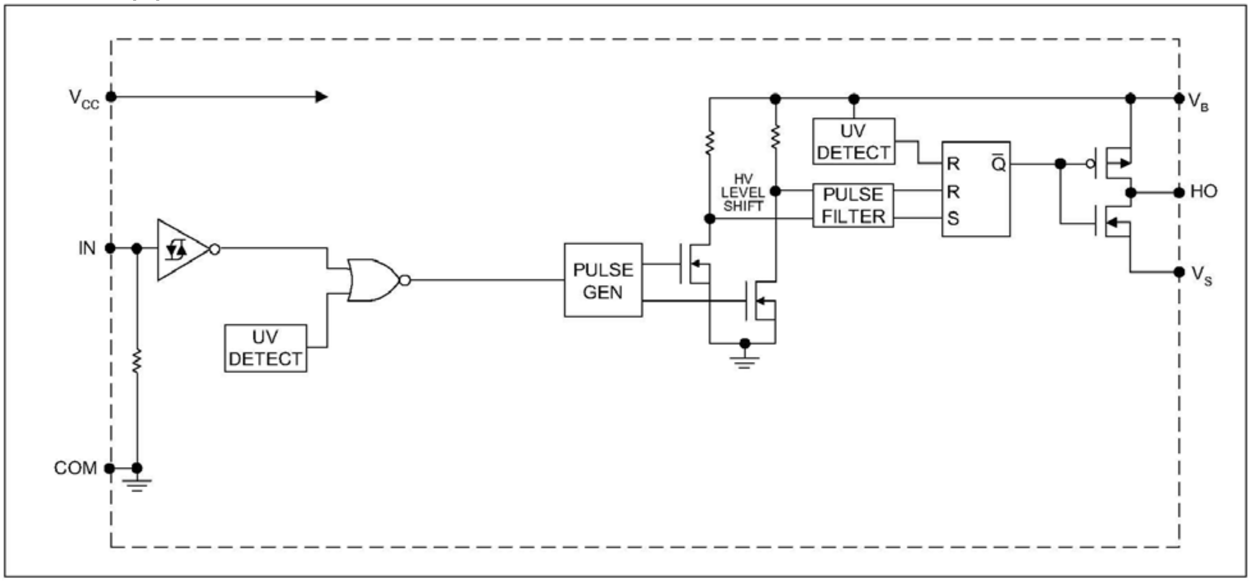
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V and T_A = 25 °C unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

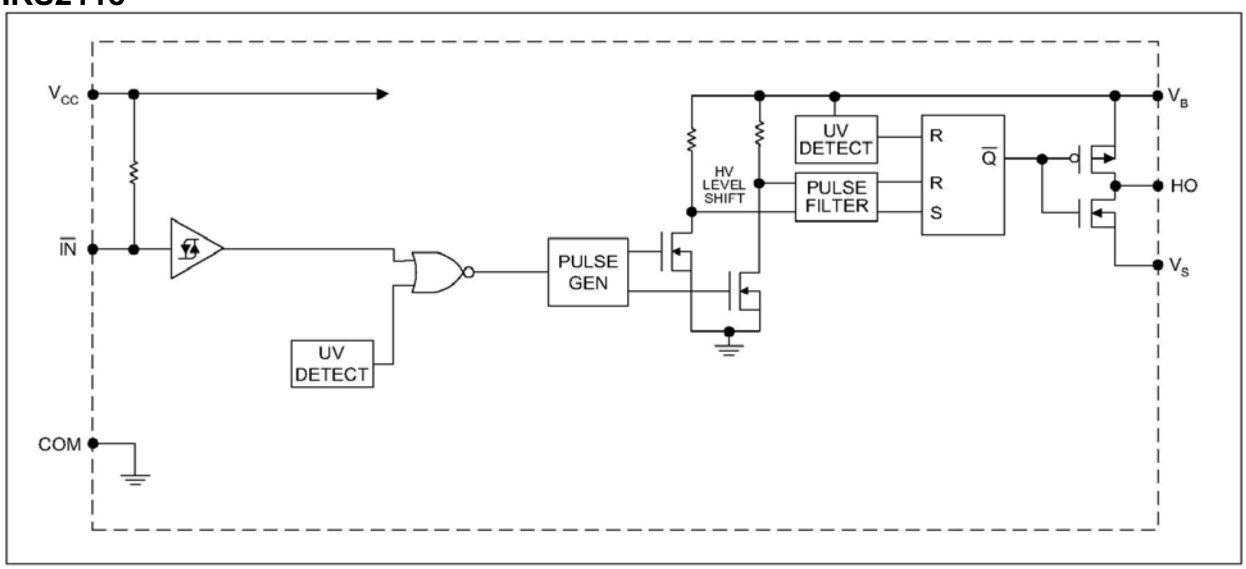
Symbol	Definition		Min	Typ	Max	Units	Test Conditions
V_{IH}	Input voltage –logic "1"	IRS21171	2.5	---	---	V	
		IRS211(7,8)	9.5	---	---		
V_{IL}	Input voltage – logic "0"	IRS21171	---	---	0.8		
		IRS211(7,8)			6.0		
V_{OH}	High level output voltage, $V_{BIAS} – V_O$		---	0.05	0.2		I_O = 2mA
V_{OL}	Low level output voltage, V_O		---	0.02	0.1		
I_{LK}	Offset supply leakage current		---	---	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} Supply Current	IRS211(7,8)	---	50	240		V_{IN} = 0V or V_{CC}
		IRS21171	---	80	150		
I_{QCC}	Quiescent V_{CC} Supply Current	IRS211(7,8)	---	70	340		
		IRS21171	---	120	240		
I_{IN+}	Logic "1" input bias current	IRS2117(1)	---	20	40		V_{IN} = V_{CC}
		IRS2118					V_{IN} = 0V
I_{IN-}	Logic "0" input bias current	IRS2117(1)	---	---	5.0		
		IRS2118					V_{IN} = V_{CC}
V_{BSUV+}	V_{BS} supply undervoltage positive going		7.6	8.6	9.6	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going		7.2	8.2	9.2		
V_{CCUV+}	V_{CC} supply undervoltage positive going		7.6	8.6	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going		7.2	8.2	9.2		
I_{O+}	Output high short circuit pulsed current		200	290	---	mA	V_O = 0V V_{IN} Logic "1" PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current		420	600	---		V_O = 15V V_{IN} Logic "0" PW ≤ 10 µs

Functional Block Diagram

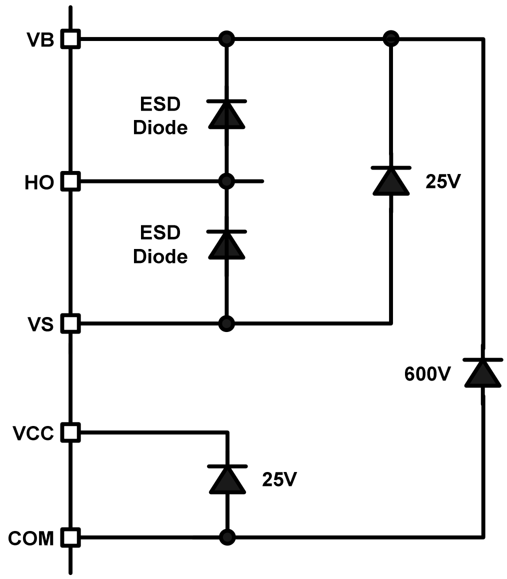
IRS2117(1)

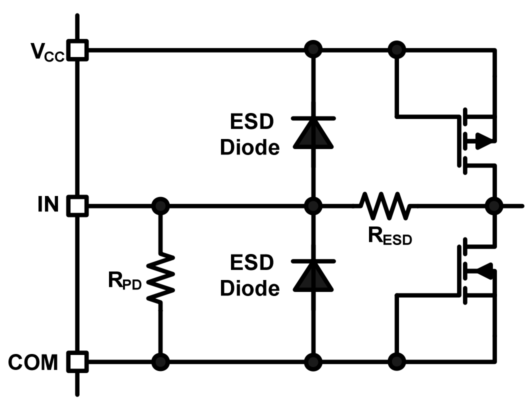


IRS2118

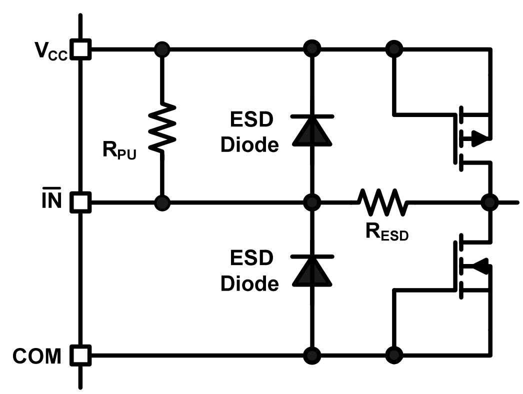


I/O Pin Equivalent Circuit Diagrams: IRS211(7,71,8)





IRS2117(1)

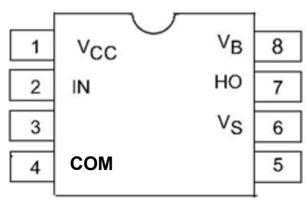


IRS2118

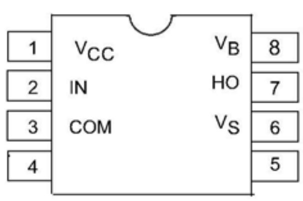
Lead Definitions

Pin #	Symbol	Description
1	VCC	Logic and gate drive supply
2	IN	IRS2117(1) Logic input for gate driver output (HO), in phase with HO
	$\overline{IN}$	IRS2118 Logic input for gate driver output (HO), out of phase with HO
3	NC	IRS21171 No Connect
	COM	IRS2117 / IRS2118 Logic ground
4	NC	IRS2117 / IRS2118 No Connect
	COM	IRS21171 Logic ground
5	NC	No Connect
6	V_S	High-side floating supply return
7	HO	High-side gate drive output
8	V_B	High-side floating supply

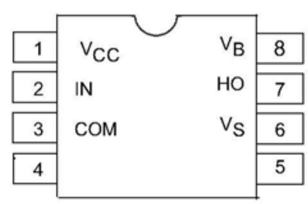
Lead Assignments



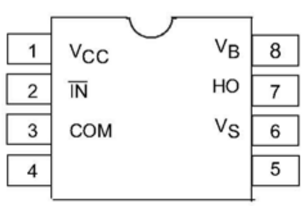
IRS21171 SOIC 8



IRS2117 PDIP 8



IRS2117 SOIC 8



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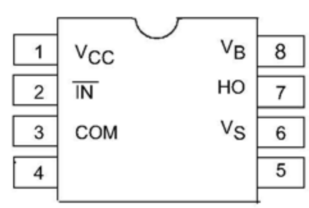


IRS2118 SOIC 8

Application Information and Additional Details

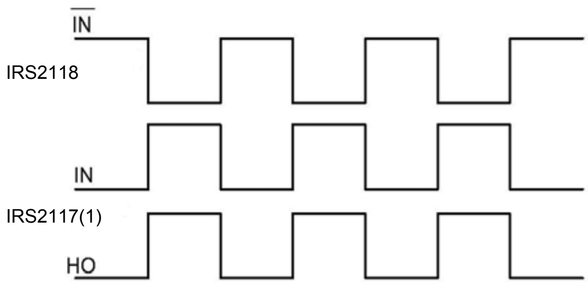


Figure 1 Input/Output Timing Diagram circuit

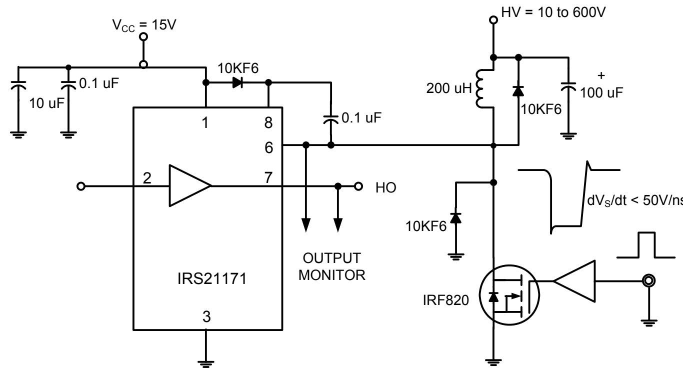


Figure 2 Floating Supply Voltage Transient Test

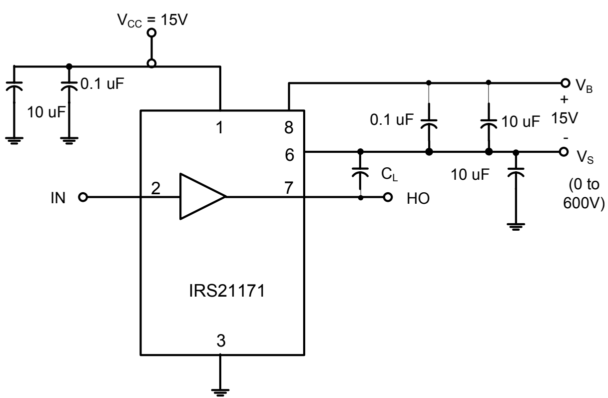


Figure 3 Switching Time Test Circuit

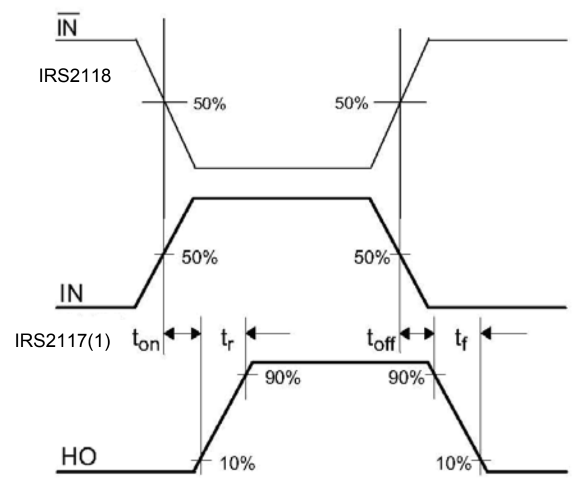


Figure 4 Switching Time Waveform Definition

Tolerant to Negative V_S Transients

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical half bridge circuit is shown in Figure 5; here we define the power switches and diodes of the inverter.

If the high-side switch (e.g., Q1 in Figures 6 and 7) switches off, while the current is flowing to a load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the inverter. At the same instance, the voltage node V_S swings from the positive DC bus voltage to the negative DC bus voltage.

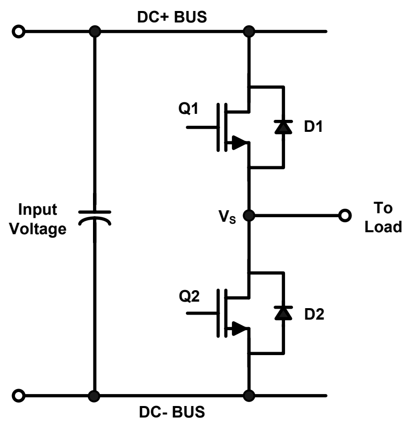


Figure 5: Half Bridge Circuit

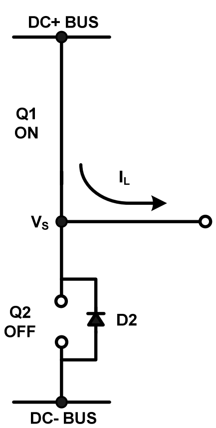


Figure 6: Q1 conducting

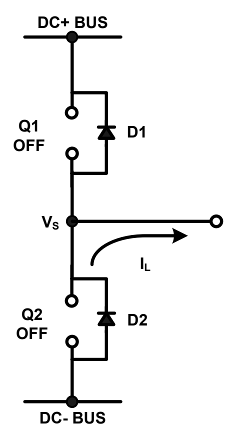


Figure 7: D2 conducting

Also when the current flows from the load back to the inverter (see Figures 8 and 9), and Q2 switches on, the current commutation occurs from D1 to Q2. At the same instance, the voltage node V_S swings from the positive DC bus voltage to the negative DC bus voltage.

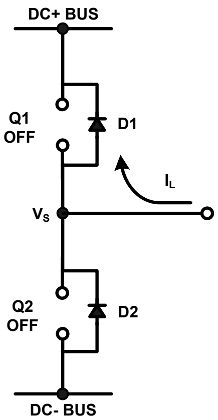


Figure 8: D1 conducting

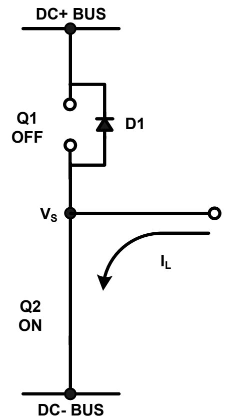


Figure 9: Q2 conducting

However, in a real inverter circuit, the V_S voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called “negative V_S transient”.

The circuit shown in Figure 10 depicts a half bridge circuit with parasitic elements shown; Figures 11 and 12 show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_D and L_S for each switch. When the high-side switch is on, V_S is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current can momentarily flow in the low-side freewheeling diode due to the inductive load connected to V_S (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_S and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the V_S pin).

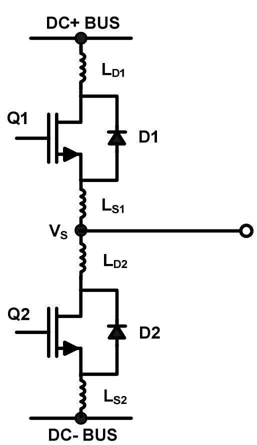


Figure 10: Parasitic Elements

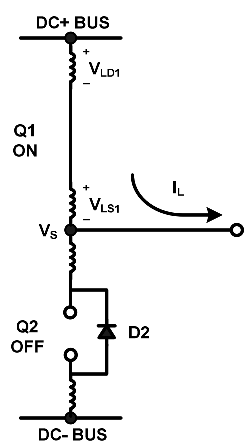


Figure 11: V_S positive

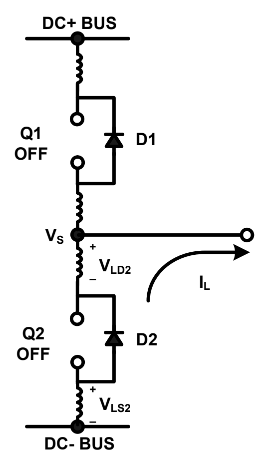


Figure 12: V_S negative

In a typical power circuit, dV/dt is typically designed to be in the range of 1-5 V/ns. The negative V_S transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

International Rectifier’s HVICs have been designed for the robustness required in many of today’s demanding applications. An indication of the IRS211(7,71,8)’s robustness can be seen in Figure 13, where there is represented the IRS211(7,71,8) Safe Operating Area at V_{BS}=15V based on repetitive negative V_S spikes. A negative V_S transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; viceversa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside SOA.

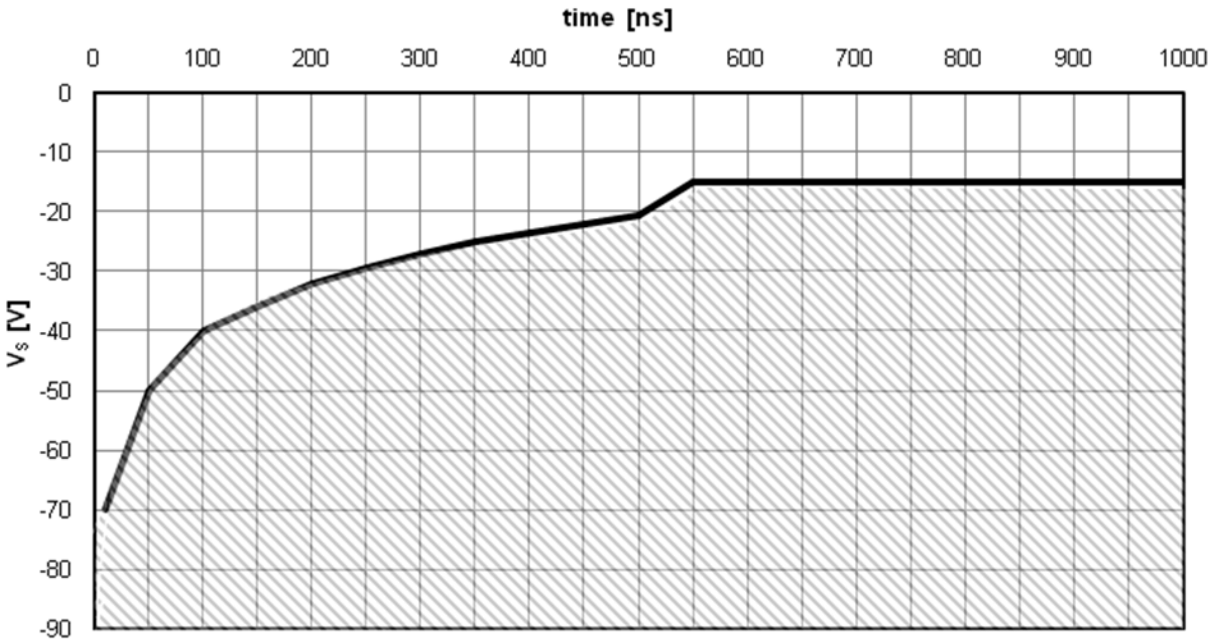


Figure 13: **Negative V_S transient SOA for IRS211(7,71,8) @ VBS=15V**

Even though the IRS211(7,71,8) has shown the ability to handle these large negative V_S transient conditions, it is highly recommended that the circuit designer always limit the negative V_S transients as much as possible by careful PCB layout and component use.

Parameter Temperature Trends - 211(7,71,8)

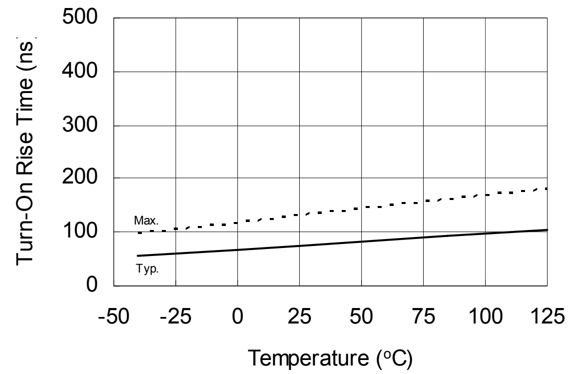


Figure 14A. Turn-On Rise Time vs.Temperature

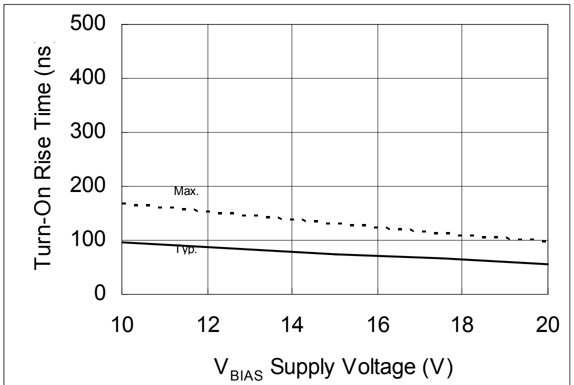


Figure 14B. Turn-On Rise Time vs. Supply Voltage

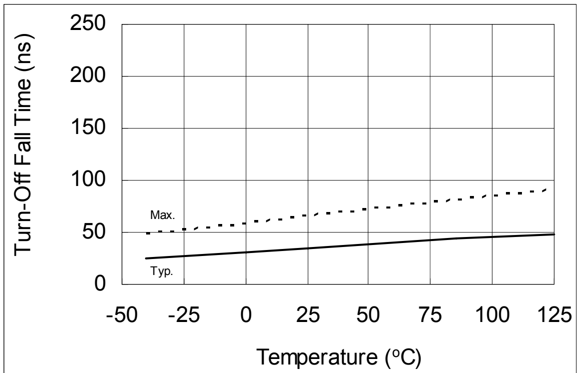


Figure 15A. Turn-Off Fall Time vs. Temperature

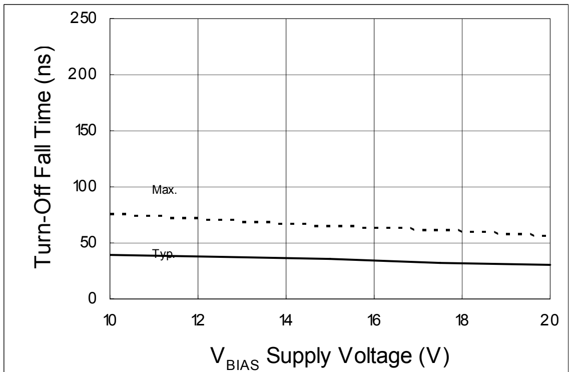


Figure 15B. Turn-Off Fall Time vs. Supply Voltage

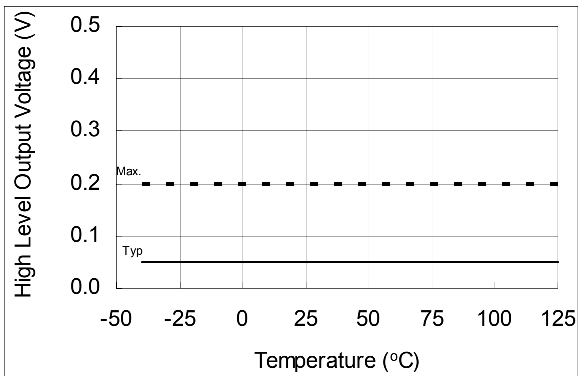


Figure 16A. High Level Output vs. Temperature (Io = 2mA)

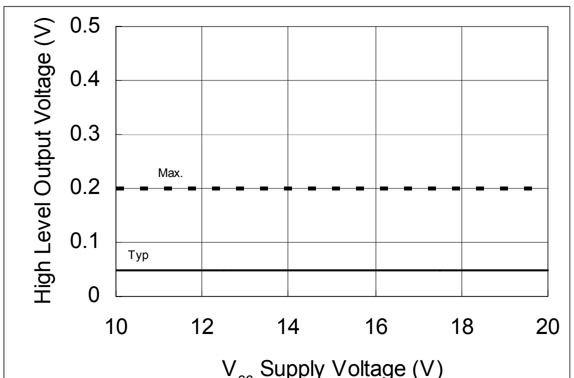


Figure 16B. High Level Output vs. Supply Voltage (Io = 2mA)

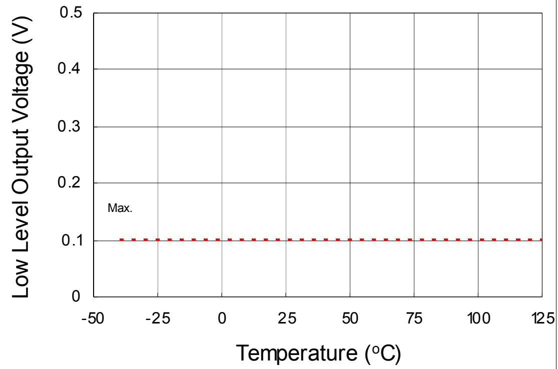


Figure 17A. Low Level Output vs.Temperature

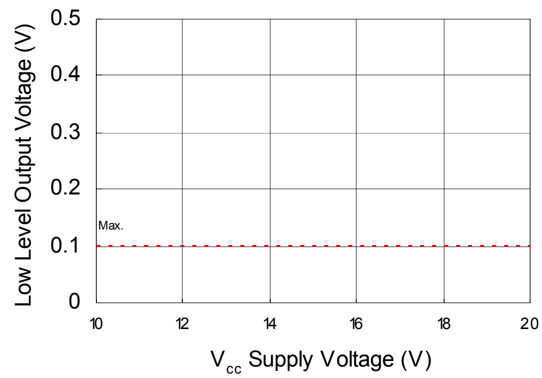


Figure 17B. Low Level Output vs. Supply Voltage

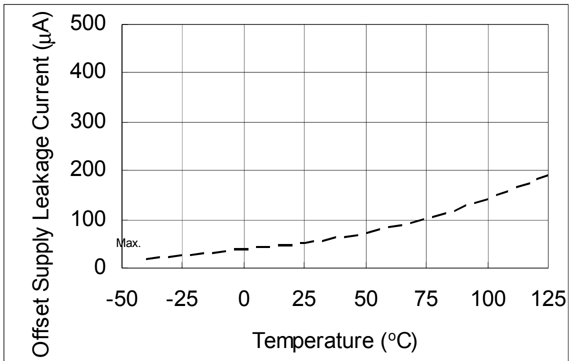


Figure 18A. Offset Supply Leakage Current vs. Temperature

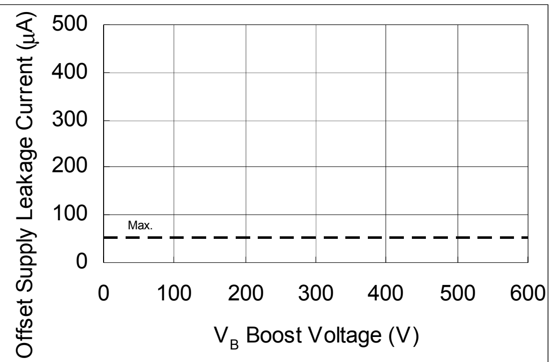


Figure 18B.Offset Supply Leakage Current vs. VB Boost Voltage

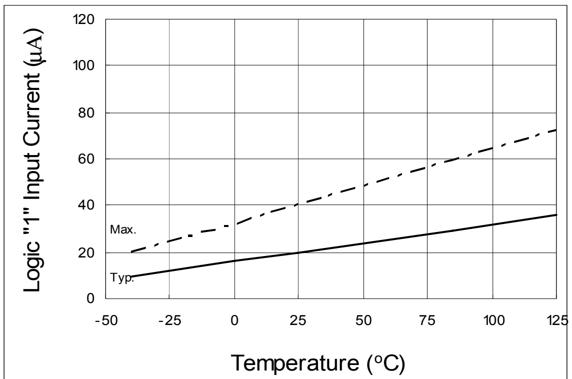


Figure 19A. Logic "1" (2118 "0") Inp Current vs. Temperature

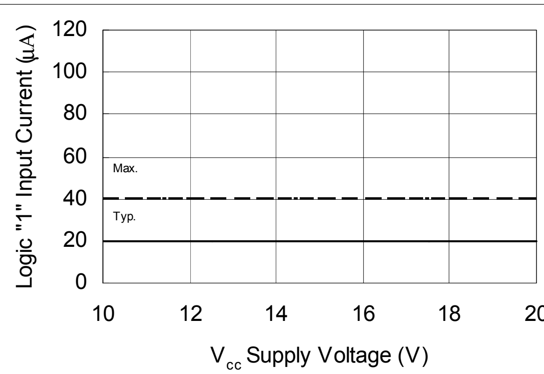


Figure 19B. Logic "1" (2118 "0") Input Current vs. Supply Voltage

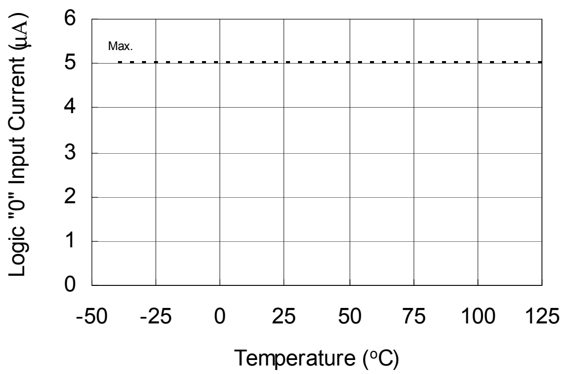


Figure 20A. Logic "0" (2118 "1") Input Current vs. Temperature

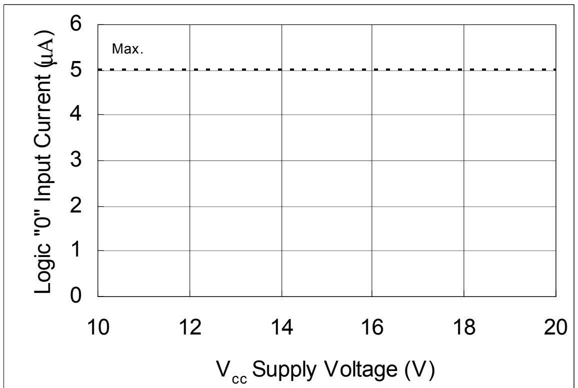


Figure 20B. Logic "0" (2118"1") Input Current vs. Supply Voltage

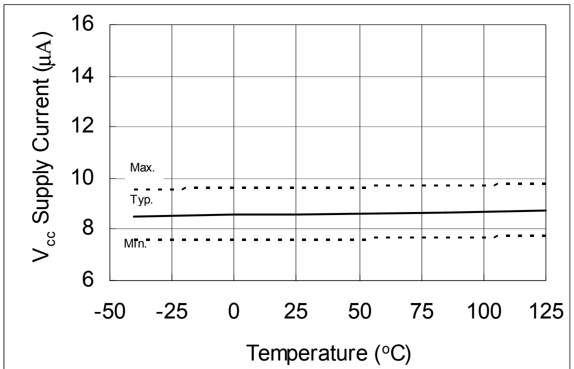


Figure 21. V_{cc} Undervoltage Threshold (+) vs. Temperature

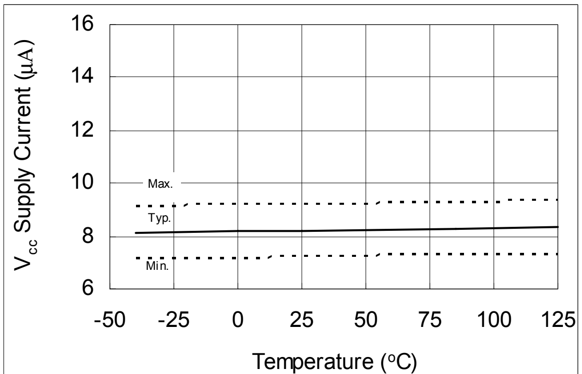


Figure 22. V_{cc} Undervoltage Threshold (-) vs. Temperature

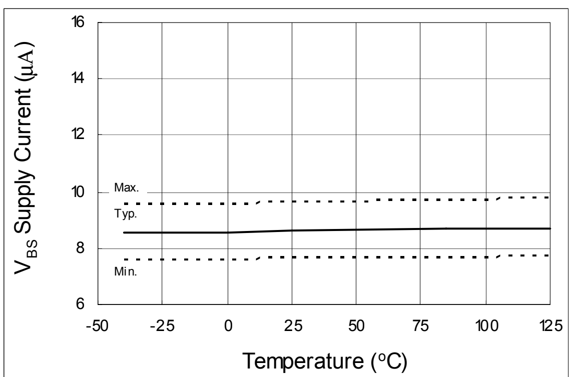


Figure 23. V_{BS} Undervoltage Threshold (+) vs. Temperature

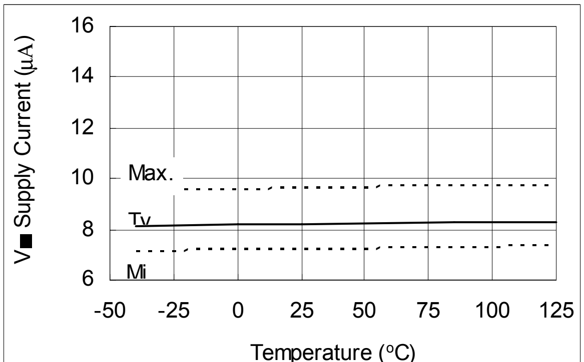


Figure 24. VBS Undervoltage Threshold (-) vs. Temperature

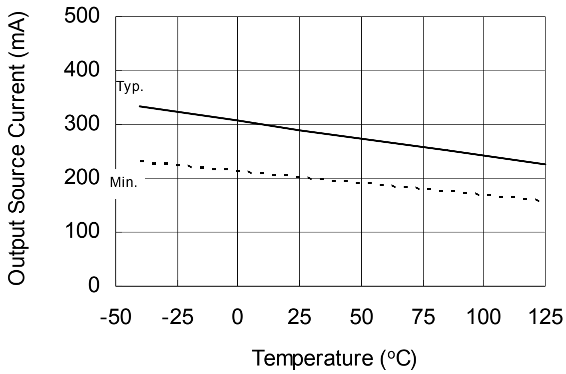


Figure 25A. Output Source Current vs. Temperature

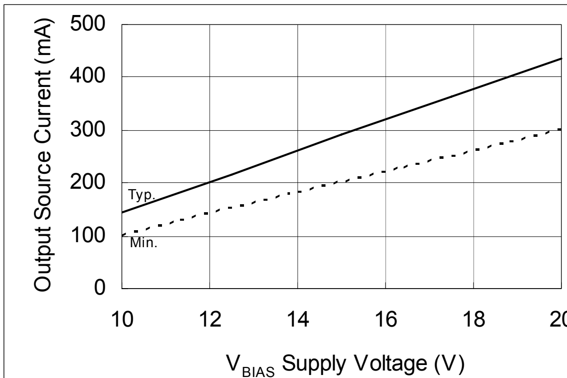


Figure 25B. Output Source Current vs. Supply Voltage

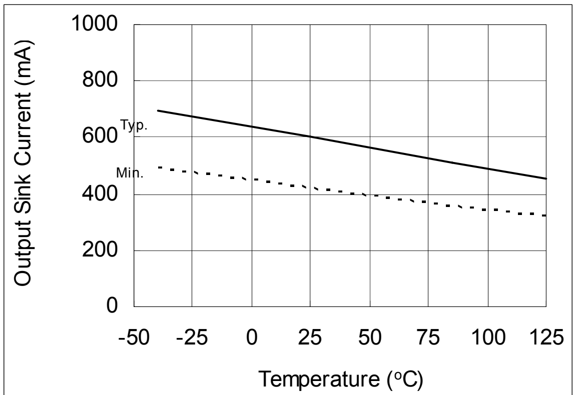


Figure 26A. Output Sink Current vs.Temperature

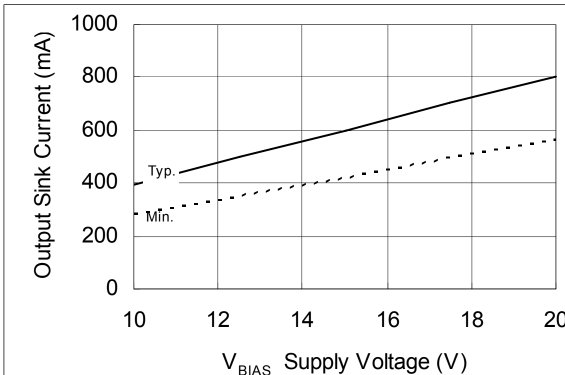


Figure 26B. Output Sink Current vs. Supply Voltage

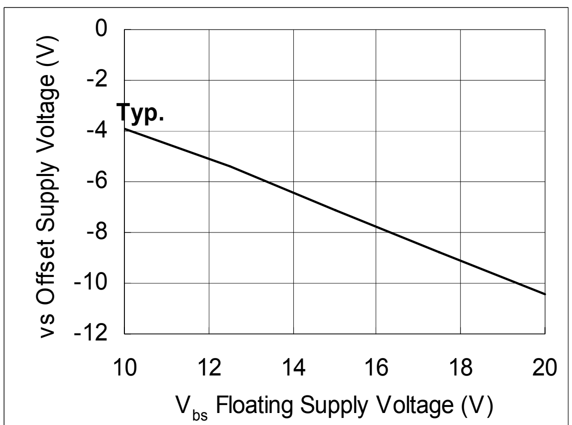


Figure 27. Maximum VS Negative Offset vs. Supply Voltage

Parameter Temperature Trends - 211(7,8)

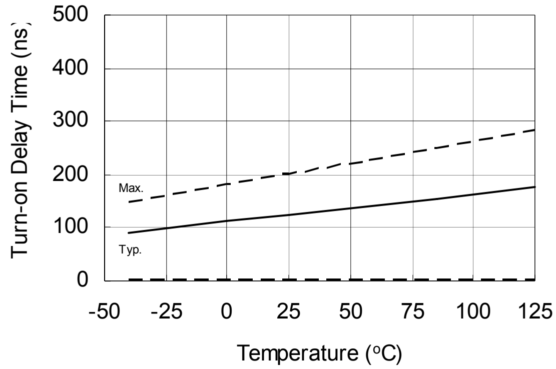


Figure 28A. IRS211(7,8) Turn-On Time vs. Temperature

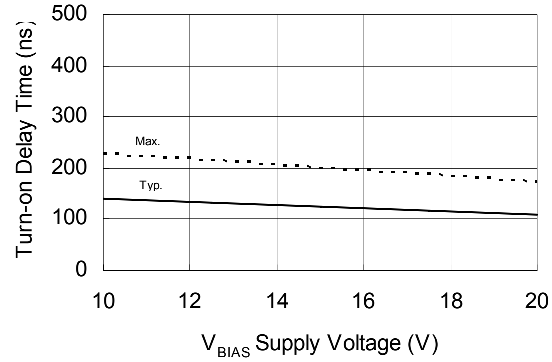


Figure 28B. IRS211(7,8) Turn-On Time vs. Supply Voltage

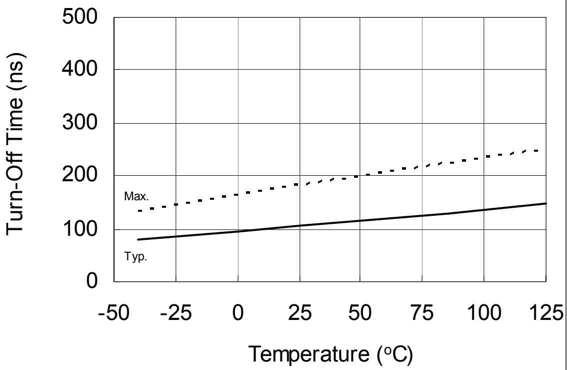


Figure 29A. IRS211(7,8) Turn-Off Time vs. Temperature

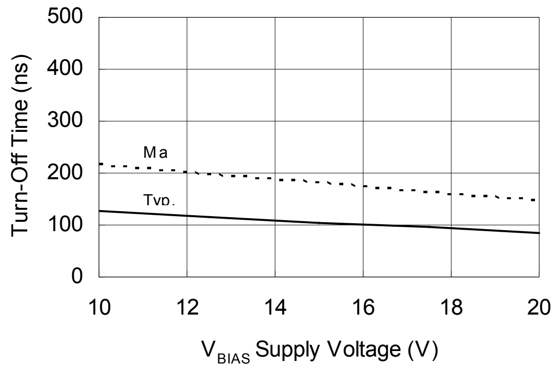


Figure 29B. IRS211(7,8) Turn-Off Time vs. Supply Voltage

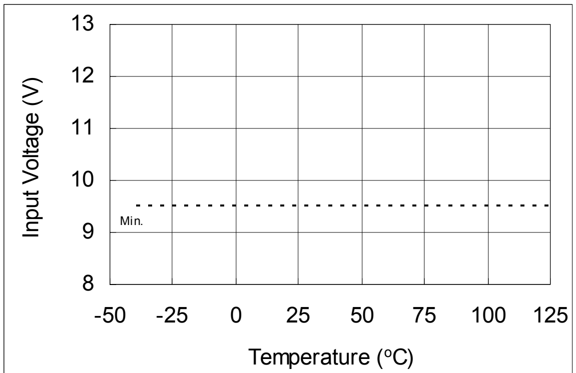


Figure 30A. IRS2117 Logic "1" (2118 "0") Input Voltage vs. Temperature

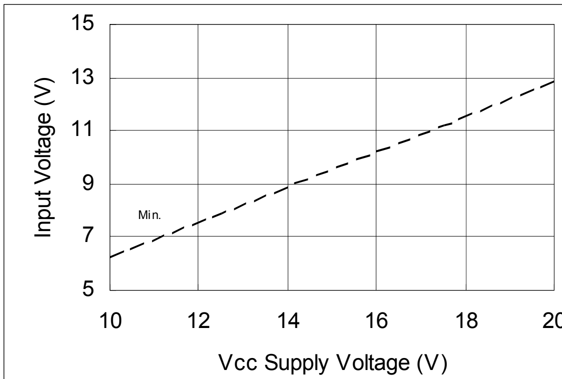


Figure 30B. IRS2117 Logic "1" (2118 "0") Input Voltage vs. Supply Voltage

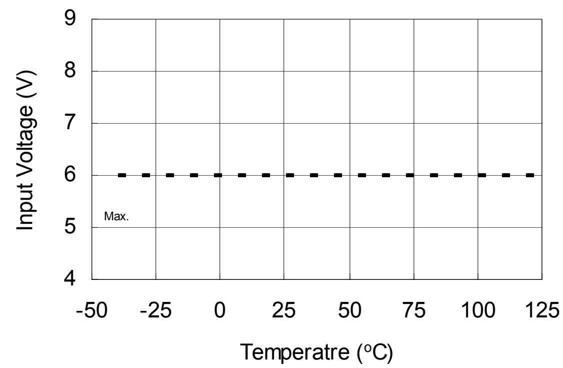


Figure 31A. IRS2117 Logic "0" (2118 "1") Input Voltage vs. Temperature

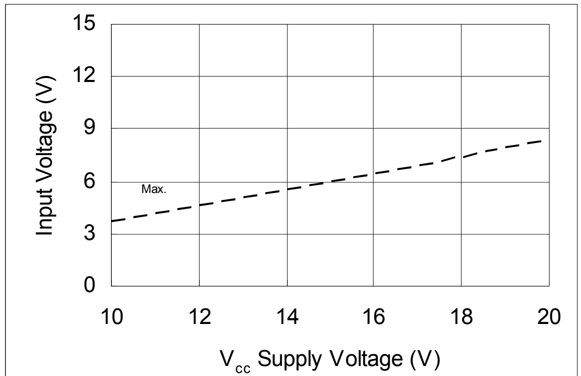


Figure 31B. IRS2117 Logic "0" (2118 "1") Input Voltage vs. Supply Voltage

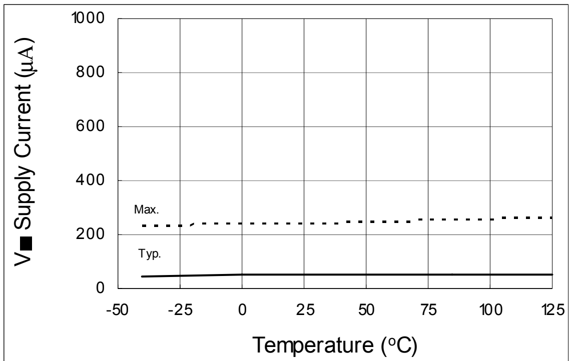


Figure 32A. 211(7,8) V_{BS} Supply Current vs. Temperature

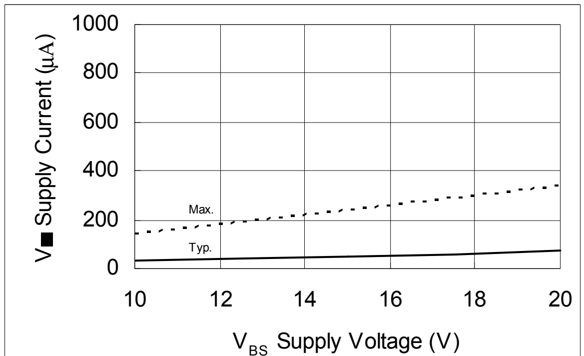


Figure 32B. 211(7,8) V_{BS} Supply Current

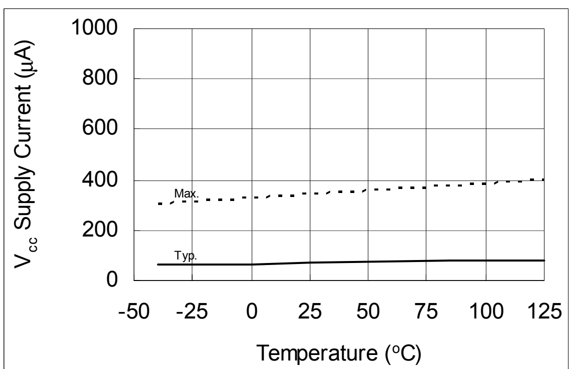


Figure 33A. 211(7,8) V_{cc} Supply Current vs. Temperature

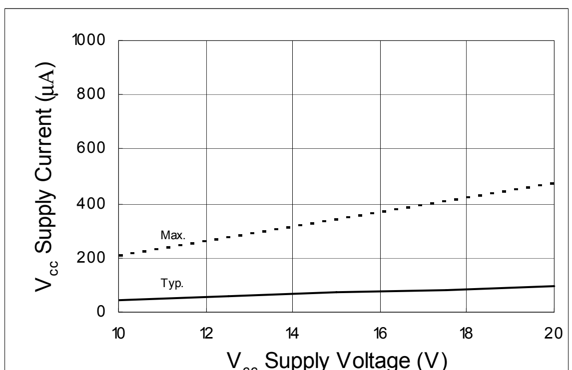


Figure 33B. 211(7,8) V_{cc} Supply Current vs. Supply Voltage

Parameter Temperature Trends - 21171

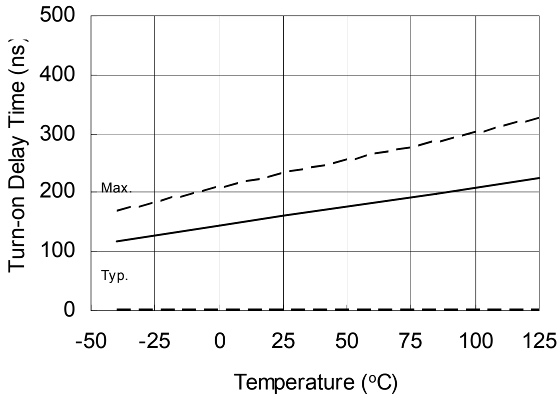


Figure 34A. IRS21171 Turn-On Time vs. Temperature

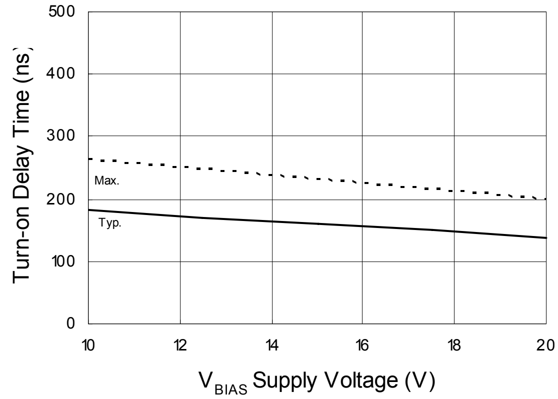


Figure 34B. IRS21171 Turn-On Time vs. Supply Voltage

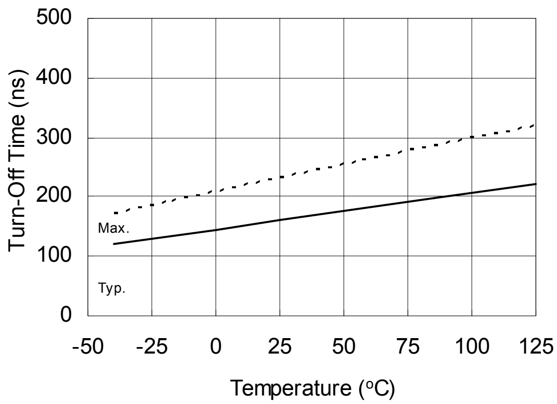


Figure 35A. IRS21171 Turn-Off Time vs. Temperature

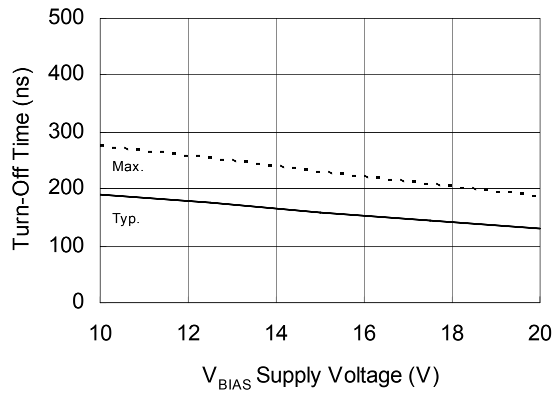


Figure 35B. IRS21171 Turn-Off Time vs. Supply Voltage

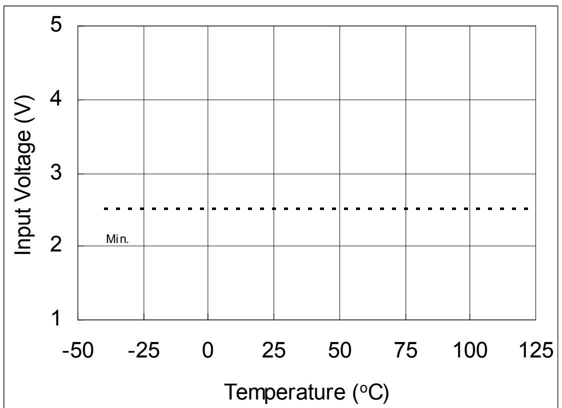


Figure 36A. IRS21171 Logic "1" Input Voltage vs. Temperature

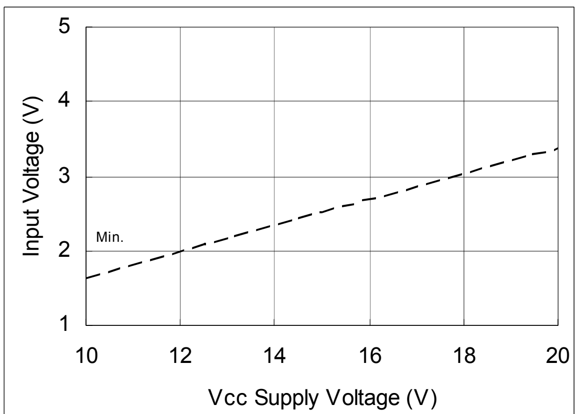


Figure 36B. IRS21171 Logic "1" Input Voltage vs. Supply Voltage

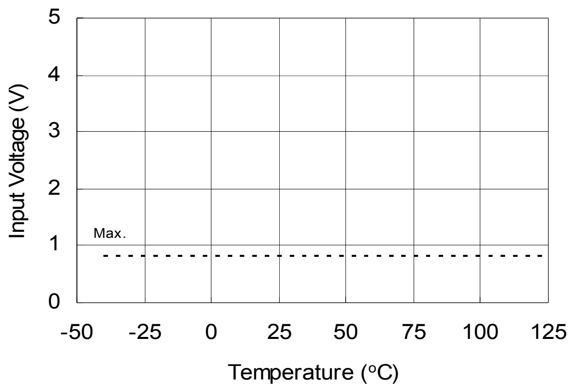


Figure 37A. IRS21171 Logic "0" Input Voltage vs. Temperature

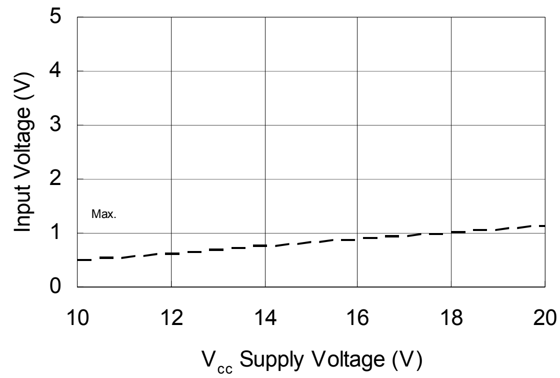


Figure 37B. IRS21171 Logic "0" Input Voltage vs. Supply Voltage

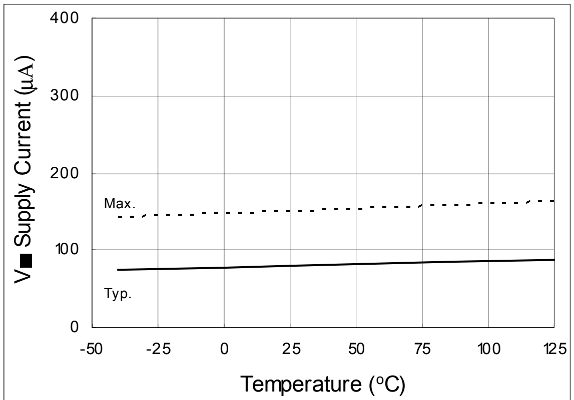


Figure 38A. IRS21171 V_{BS} Supply Current vs. Temperature

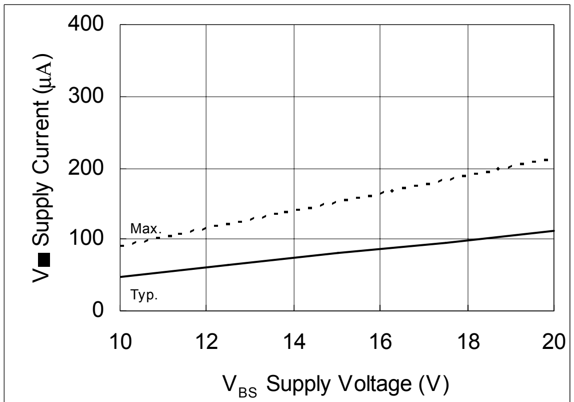


Figure 38B. IRS21171 V_{BS} Supply Current vs. Supply Voltage

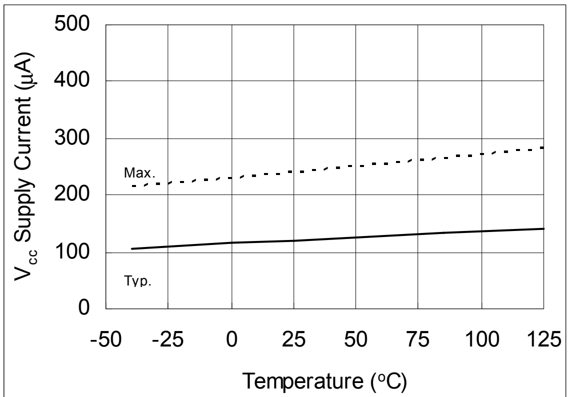


Figure 39A. IRS21171 V_{cc} Supply Current vs. Temperature

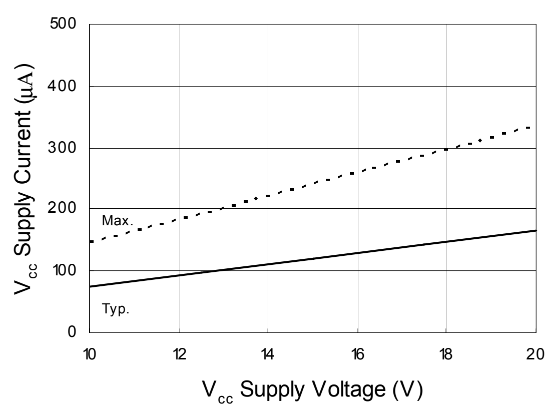


Figure 39B. IRS21171 V_{cc} Supply Current vs. Supply Voltage

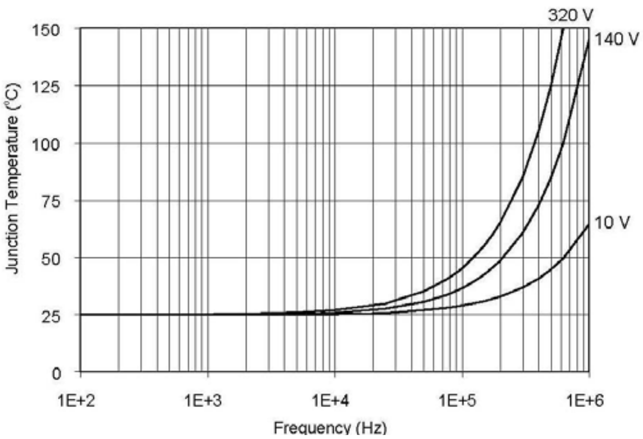


Figure 40. IRS2117/IRS2118 T_J vs. Frequency (IRFBC20) R_{GATE}=33Ω, V_{CC}=15V

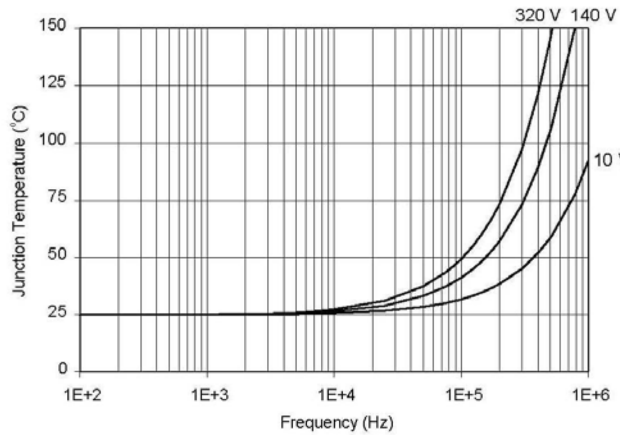


Figure 41. IRS2117/IRS2118 T_J vs. Frequency (IRFBC30) R_{GATE}=22Ω, V_{CC}=15V

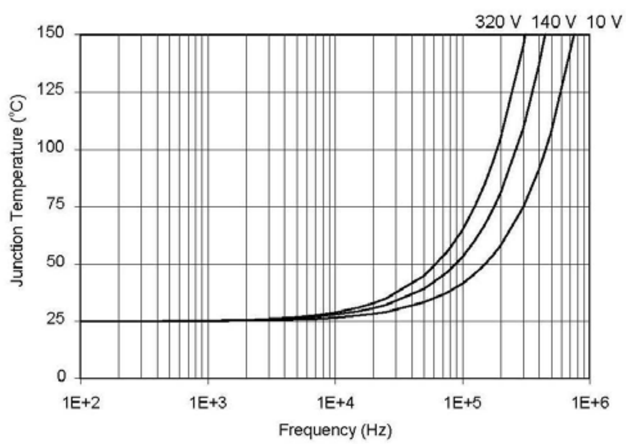


Figure 42. IRS2117/IRS2118 T_J vs. Frequency (IRFBC40) R_{GATE}=15Ω, V_{CC}=15V

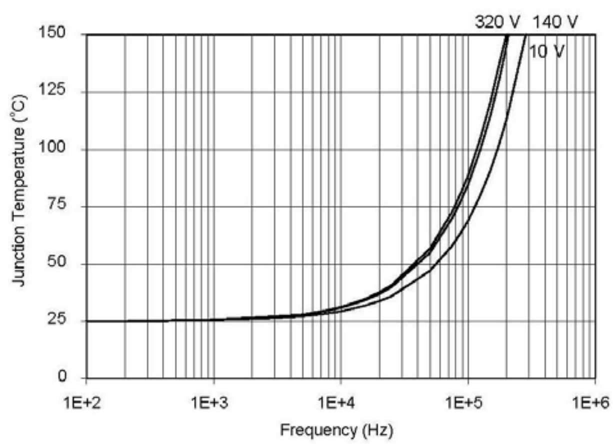
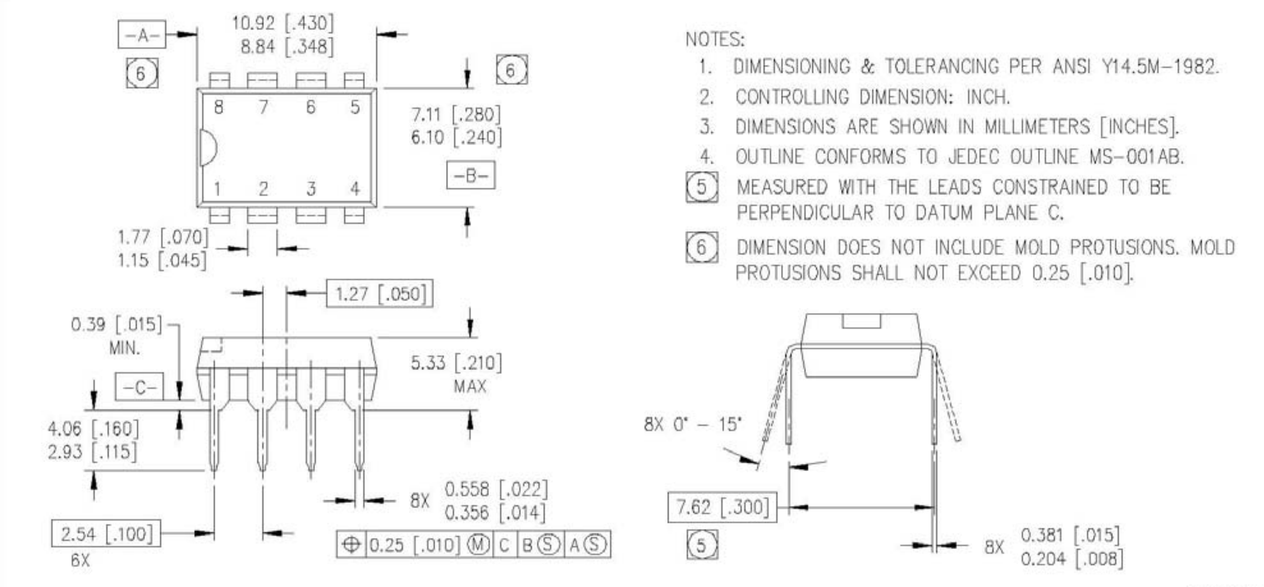


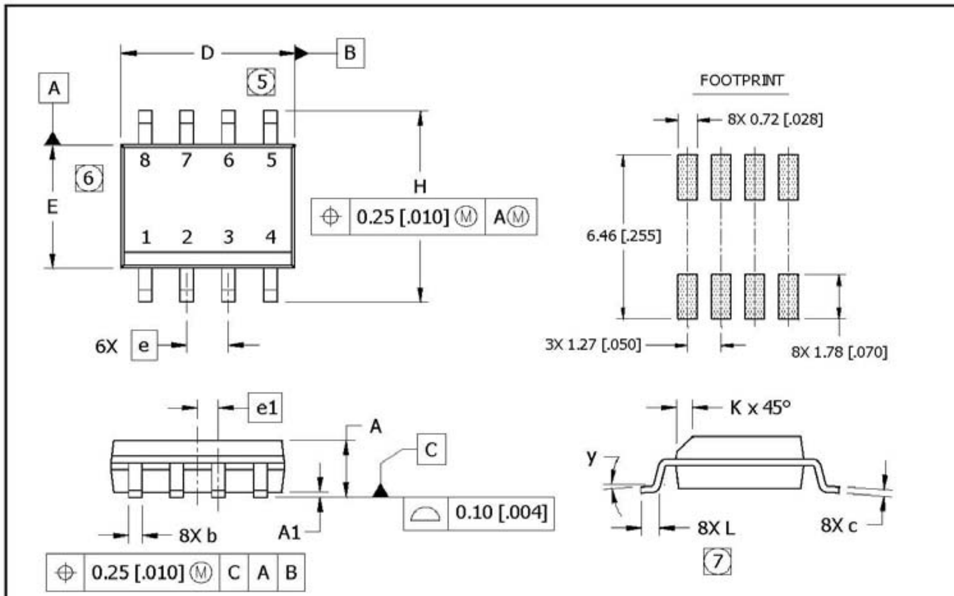
Figure 43. IRS2117/IRS2118 T_J vs. Frequency (IRFPE50) R_{GATE}=10Ω, V_{CC}=15V

Package Details



8 Lead PDIP

01-6014
01-3003 01 (MS-001AB)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

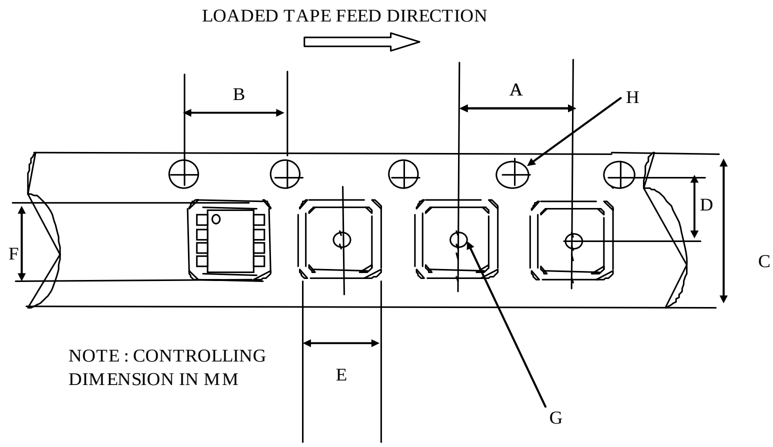
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8 Lead SOIC

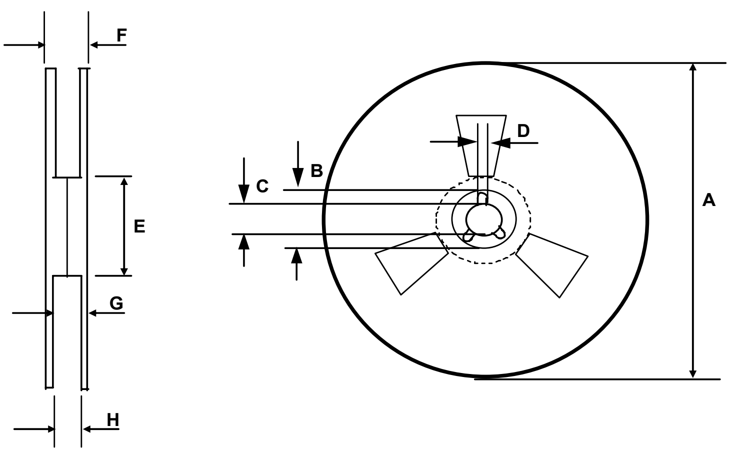
01-6027
01-0021 11 (MS-012AA)

Package Details: SOIC8N, Tape and Reel



CARRIER TAPE DIMENSION FOR 8SOICN

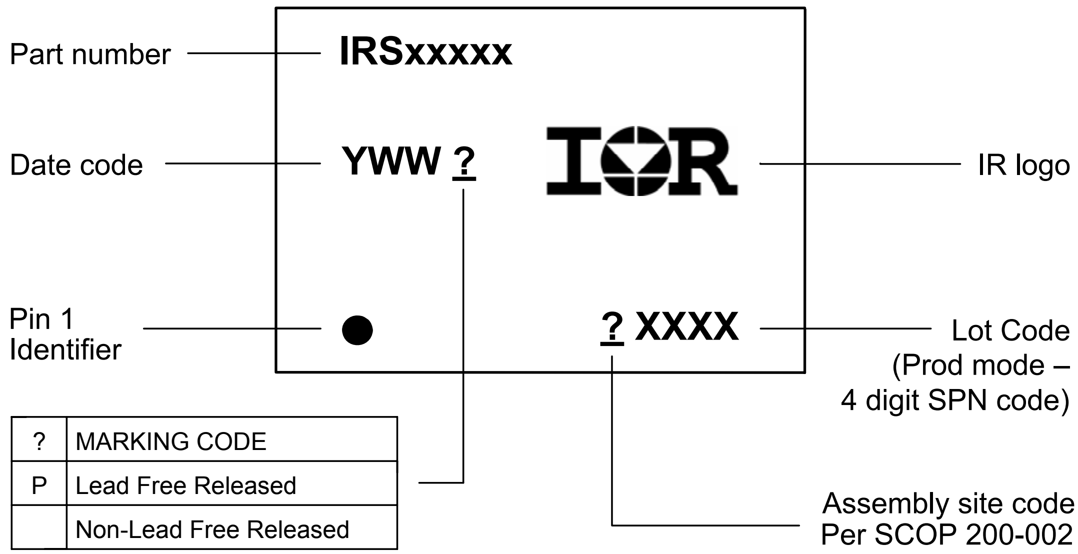
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS2117	SOIC8N	Tube/Bulk	95	IRS2117SPBF
		Tape and Reel	2500	IRS2117STRPBF
	PDIP8	Tube/Bulk	50	IRS2117PBF
IRS21171	SOIC8N	Tube/Bulk	95	IRS21171SPBF
		Tape and Reel	2500	IRS21171STRPBF
IRS2118	SOIC8N	Tube/Bulk	95	IRS2118SPBF
		Tape and Reel	2500	IRS2118STRPBF
	PDIP8	Tube/Bulk	50	IRS2118PBF

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

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