

# LF2101N

## High-Side / Low-Side Gate Driver

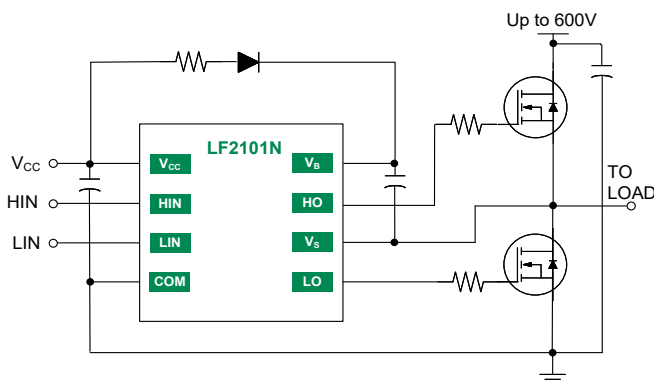
### Features

- Floating high-side driver in bootstrap operation to 600V
- Drives two N-channel MOSFETs or IGBTs in high-side/low-side configuration
- Outputs tolerant to negative transients
- Wide low-side gate driver and logic supply: 10V to 20V
- Logic inputs CMOS and TTL compatible (down to 3.3V)
- Schmitt triggered logic inputs with internal pull down
- Under Voltage Lockout (UVLO) for  $V_{CC}$  (low-side driver)
- Space-saving SOIC(N)-8 package available
- Extended temperature range:-40°C to +125°C

### Applications

- DC-DC Converters
- AC-DC Inverters
- Motor Controls
- Class D Power Amplifiers

### Typical Application



### Description

The LF2101N is a high voltage, high speed gate driver capable of driving N-channel MOSFETs and IGBTs in a high-side/low-side configuration. The high voltage process enables the LF2101N's high-side to switch to 600V in a bootstrap operation. The 50ns (max) propagation delay matching between the high and the low side drivers allows high frequency switching.

LF2101N logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) for easy interfacing with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction. The low-side gate driver and logic share a common ground

LF2101N is offered in a space-saving 8-pin SOIC package operating over the extended temperature range of -40°C to +125°C.



SOIC(N)-8

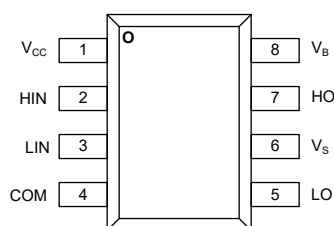
### Ordering Information

| YearYear WeekWeek |           |            |                           |
|-------------------|-----------|------------|---------------------------|
| Part#             | Package   | Pack / Qty | Mark                      |
| LF2101NTR         | SOIC(N)-8 | T&R / 2500 | YYWW<br>LF2101N<br>LOT ID |



## 1 Specifications

### 1.1 Pin Diagrams



**Top View:** SOIC(N)-8

**LF2101N**

### 1.2 Pin Descriptions

| Pin# | Pin Name        | Pin Type | Pin Description                                             |
|------|-----------------|----------|-------------------------------------------------------------|
| 1    | V <sub>CC</sub> | Power    | Low-side and logic fixed supply                             |
| 2    | HIN             | Input    | Logic input for high-side gate driver output (HO), in phase |
| 3    | LIN             | Input    | Logic input for low-side gate driver output (LO), in phase  |
| 4    | COM             | Power    | Low-side return                                             |
| 5    | LO              | Output   | Low-side gate drive output                                  |
| 6    | V <sub>S</sub>  | Power    | High-side floating supply return                            |
| 7    | HO              | Output   | High-side gate drive output                                 |
| 8    | V <sub>B</sub>  | Power    | High-side floating supply                                   |

### 1.3 Absolute Maximum Ratings

| Parameter                                | Symbol    | Min         | Max            | Unit |
|------------------------------------------|-----------|-------------|----------------|------|
| High side floating supply voltage        | $V_B$     | -0.3        | +624           | V    |
| High side floating supply offset voltage | $V_S$     | $V_B - 24$  | $V_B + 0.3$    | V    |
| High side floating output voltage        | $V_{HO}$  | $V_S - 0.3$ | $V_B + 0.3$    | V    |
| Offset supply voltage transient          | $dV_S/dt$ | --          | 50             | V/ns |
| Low side fixed supply voltage            | $V_{CC}$  | -0.3        | +24            | V    |
| Low side output voltage                  | $V_{LO}$  | -0.3        | $V_{CC} + 0.3$ | V    |
| Logic input voltage (HIN and LIN)        | $V_{IN}$  | -0.3        | $V_{CC} + 0.3$ | V    |
| Package power dissipation                | $P_D$     | --          | 0.625          | W    |
| Junction Operating Temperature           | $T_J$     | --          | +150           | °C   |
| Storage Temperature                      | $T_{STG}$ | -55         | +150           | °C   |

Unless otherwise specified all voltages are referenced to COM. All electrical ratings are at  $T_A = 25^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### 1.4 Thermal Characteristics

| Parameter           | Symbol        | Rating | Unit |
|---------------------|---------------|--------|------|
| Junction to ambient | $\theta_{JA}$ | 200    | °C/W |

When mounted on a standard JEDEC 2-layer FR-4 board - JESD51-3

### 1.5 Recommended Operating Conditions

| Parameter                                  | Symbol   | Min          | Max        | Unit |
|--------------------------------------------|----------|--------------|------------|------|
| High side floating supply absolute voltage | $V_B$    | $V_S + 10$   | $V_S + 20$ | V    |
| High side floating supply offset voltage   | $V_S$    | <b>NOTE1</b> | 600        | V    |
| High side floating output voltage          | $V_{HO}$ | $V_S$        | $V_B$      | V    |
| Low side and logic fixed supply voltage    | $V_{CC}$ | 10           | 20         | V    |
| Low side output voltage                    | $V_{LO}$ | 0            | $V_{CC}$   | V    |
| Logic input voltage (HIN and LIN)          | $V_{IN}$ | 0            | 5          | V    |
| Ambient temperature                        | $T_A$    | -40          | 125        | °C   |

Unless otherwise specified all voltages are referenced to COM

**NOTE1** High-side driver remains operational for  $V_S$  transients down to -5V

### 1.6 DC Electrical Characteristics

$V_{CC} = V_{BS} = 15V$ ,  $T_A = 25^\circ C$  and  $V_{COM} = 0V$ , unless otherwise specified.

The  $V_{IN}$  and  $I_{IN}$  parameters are applicable to both logic input pins: HIN and LIN. The  $V_O$  and  $I_O$  parameters are applicable to the respective output pins: HO and LO and are referenced to COM

| Parameter                                     | Symbol          | Conditions                                                       | Min | Typ  | Max | Unit    |
|-----------------------------------------------|-----------------|------------------------------------------------------------------|-----|------|-----|---------|
| Logic "1" input voltage                       | $V_{IH}$        | $V_{CC} = 10V \text{ to } 20V$ ,<br><b>NOTE2</b>                 | 2.5 | --   | --  | V       |
| Logic "0" input voltage                       | $V_{IL}$        |                                                                  | --  | --   | 0.8 |         |
| Logic input voltage hysteresis                | $V_{IN(HYS)}$   |                                                                  | --  | 0.3  | --  |         |
| High level output voltage, $V_{BIAS} - V_O$   | $V_{OH}$        | $I_O = 2mA$                                                      | --  | 0.05 | 0.2 | V       |
| Low level output voltage, $V_O$               | $V_{OL}$        | $I_O = 2mA$                                                      | --  | 0.02 | 0.1 | V       |
| Offset supply leakage current                 | $I_{LK}$        | $V_B = V_S = 600V$                                               | --  | --   | 50  | $\mu A$ |
| Quiescent $V_{BS}$ supply current             | $I_{BSQ}$       | $V_{IN} = 0V \text{ or } 5V$                                     | --  | 30   | 55  | $\mu A$ |
| Quiescent $V_{CC}$ supply current             | $I_{CCQ}$       | $V_{IN} = 0V \text{ or } 5V$                                     | --  | 150  | 270 | $\mu A$ |
| Logic "1" input bias current                  | $I_{IN+}$       | $V_{IN} = 5V$                                                    | --  | 3    | 10  | $\mu A$ |
| Logic "0" input bias current                  | $I_{IN-}$       | $V_{IN} = 0V$                                                    | --  | --   | 5   | $\mu A$ |
| $V_{CC}$ UVLO off positive going threshold    | $V_{CCUV+}$     | --                                                               | 8   | 8.9  | 9.8 | V       |
| $V_{CC}$ UVLO enable negative going threshold | $V_{CCUV-}$     | --                                                               | 7.4 | 8.2  | 9   |         |
| $V_{CC}$ UVLO hysteresis                      | $V_{CCUV(HYS)}$ | --                                                               | --  | 0.7  | --  |         |
| Output high short circuit pulsed current      | $I_{O+}$        | $V_O = 0V$ , $V_{IN} = \text{Logic "1"}$ ,<br>$t \leq 10 \mu s$  | 130 | 290  | --  | mA      |
| Output low short circuit pulsed current       | $I_{O-}$        | $V_O = 15V$ , $V_{IN} = \text{Logic "0"}$ ,<br>$t \leq 10 \mu s$ | 270 | 600  | --  | mA      |

**NOTE2** For optimal operation, it is recommended the input pulse (to HIN and LIN) should have a minimum amplitude of 2.5V a minimum pulse width of 300ns.

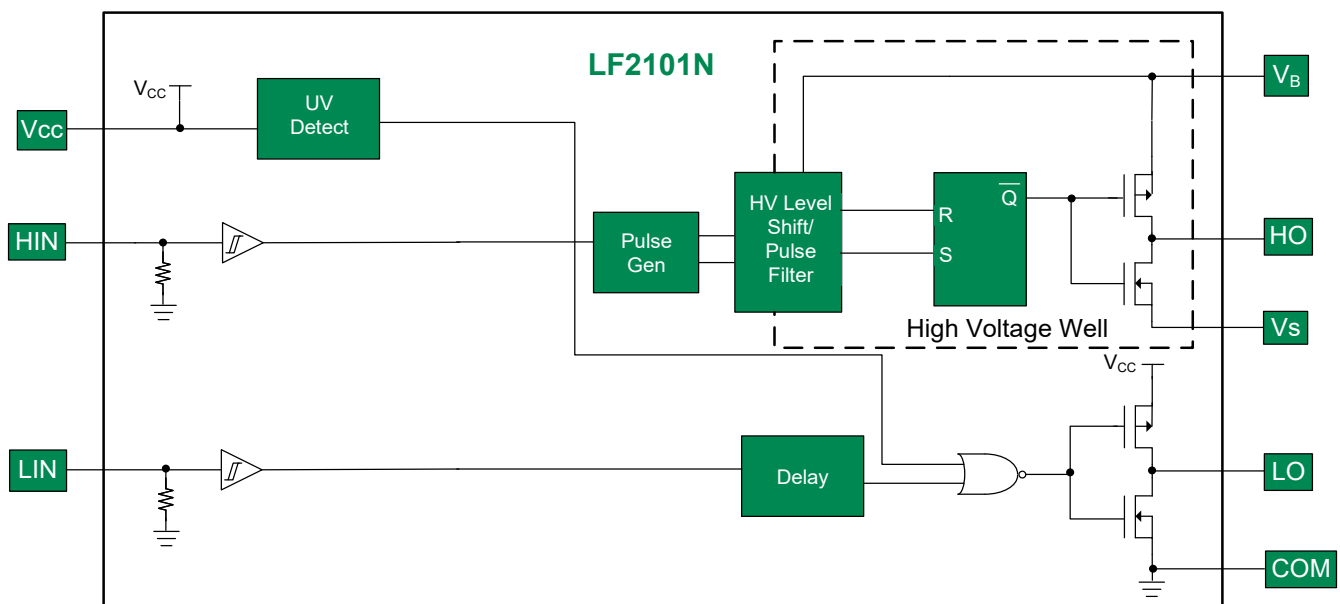
### 1.7 AC Electrical Characteristics

$V_{CC} = V_{BS} = 15V$ ,  $C_L = 1000pF$ , and  $T_A = 25^\circ C$ , unless otherwise specified.

| Parameter                  | Symbol    | Conditions   | Min | Typ | Max | Unit |
|----------------------------|-----------|--------------|-----|-----|-----|------|
| Turn-on propagation delay  | $t_{ON}$  | $V_S = 0V$   | --  | 160 | 220 | ns   |
| Turn-off propagation delay | $t_{OFF}$ | $V_S = 600V$ | --  | 150 | 220 | ns   |
| Turn-on rise time          | $t_r$     | --           | --  | 70  | 170 | ns   |
| Turn-off fall time         | $t_f$     | --           | --  | 35  | 90  | ns   |
| Propagation delay matching | $t_{DM}$  | --           | --  | --  | 50  | ns   |

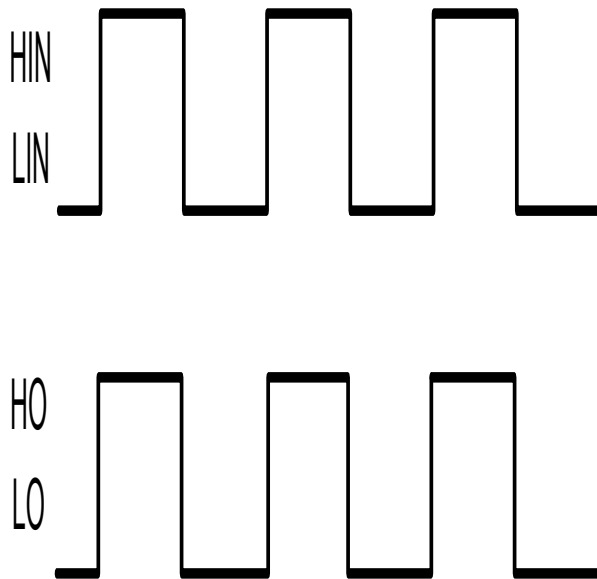
## 2 Functional Description

### 2.1 Functional Block Diagram

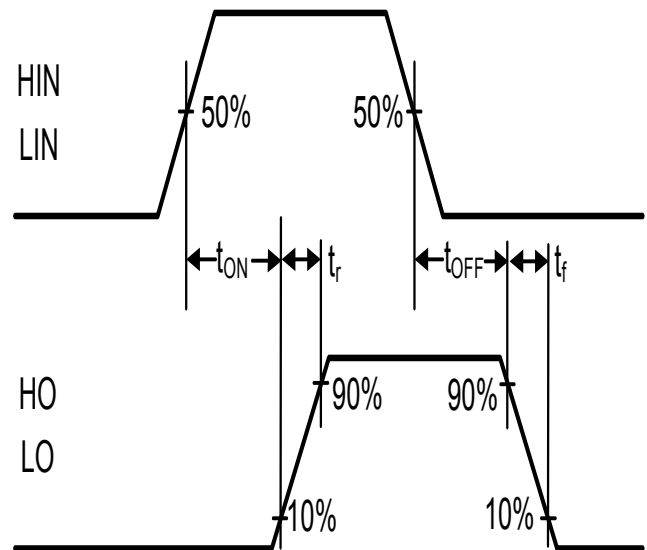


### 2.2 Timing Waveforms

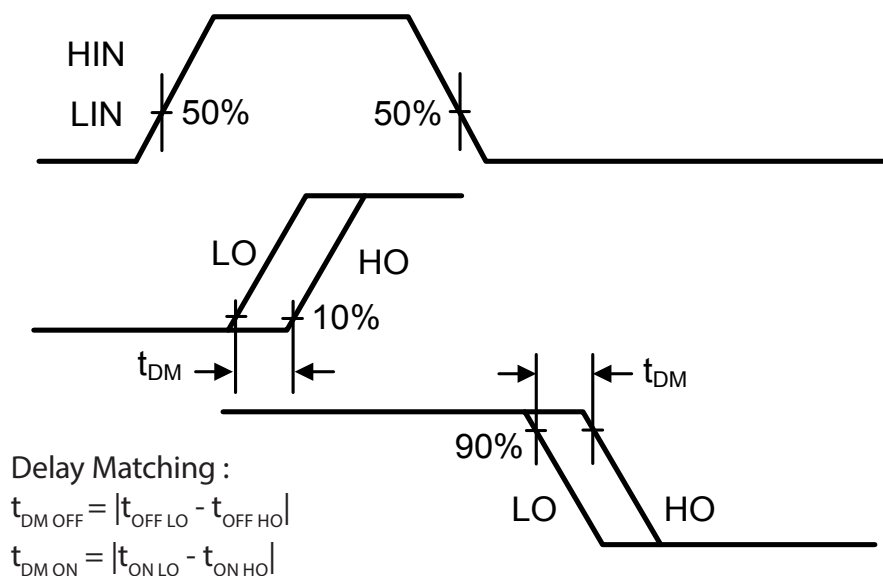
**Figure 1.** Input / Output Logic Diagram



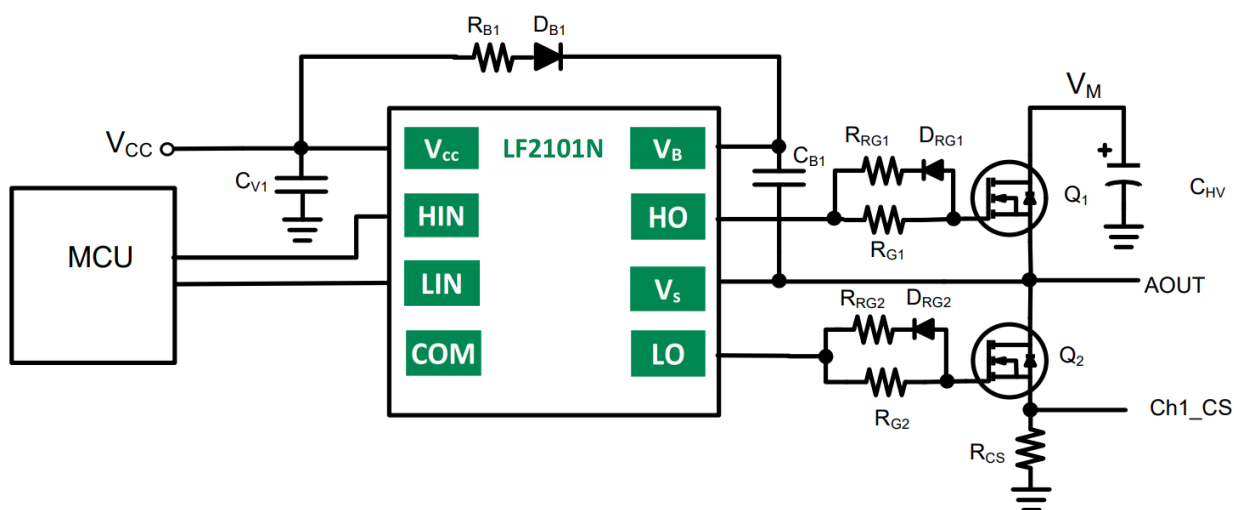
**Figure 2.** Input-to-Output Delay Timing Diagram



**Figure 3.** Delay Matching Waveform



### 2.3 Application Information



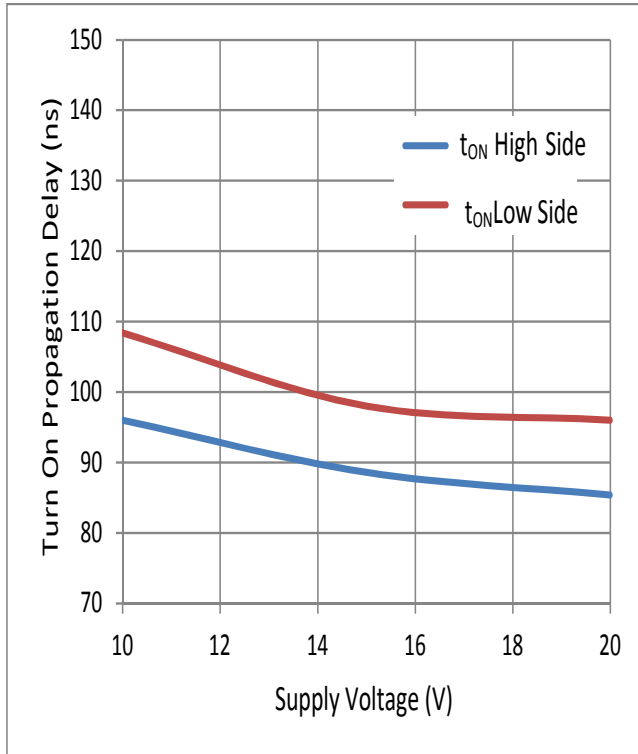
**Figure 4.** Single phase (of four) for Stepper motor driver application using the LF2101N

- RRG1 and RRG2 values are typically between  $0\Omega$  and  $10\Omega$ , exact value decided by MOSFET junction capacitance and drive current of gate driver;  $10\Omega$  is used in this example.
- It is **highly recommended** that the input pulse (to HIN and LIN) should have an amplitude of 2.5V minimum (for  $V_{cc}=15V$ ) with a minimum pulse width of 300ns.
- RG1 and RG2 values are typically between  $10\Omega$  and  $100\Omega$ , exact value decided by MOSFET junction capacitance and drive current of gate driver;  $50\Omega$  is used in this example.
- RB1 value is typically between  $3\Omega$  and  $20\Omega$ , exact value depending on bootstrap capacitor value and amount of current limiting required for bootstrap capacitor charging;  $10\Omega$  is used in this example. Also DB should be an ultra fast diode of 1A rating minimum and voltage rating greater than system operating voltage.

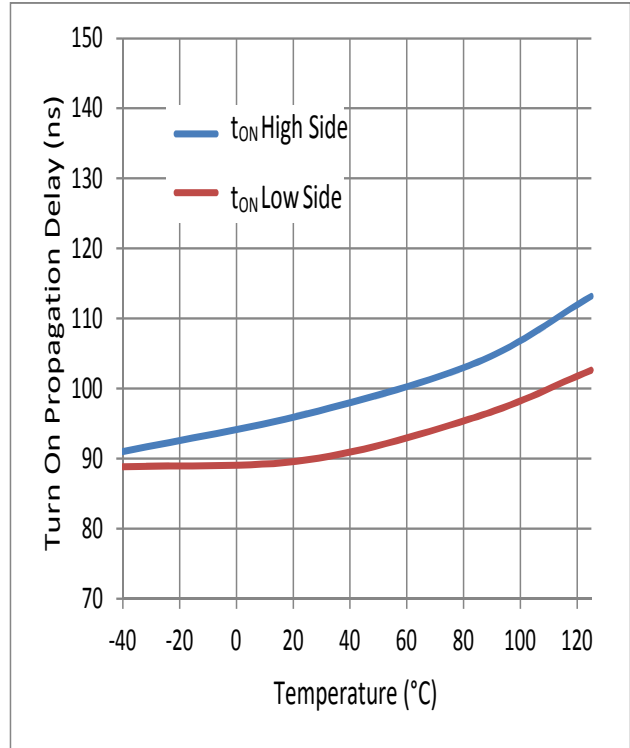
### 3 Performance Data

Unless otherwise noted  $V_{CC} = V_{BS} = 15V$ ,  $T_A = 25^\circ C$ ,  $V_{COM} = 0V$  and values are typical.

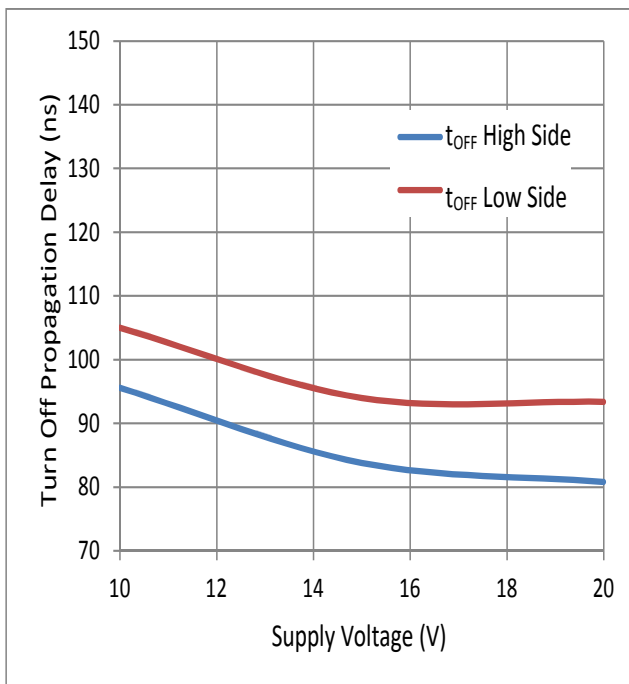
**Figure 5.** Turn-on Propagation Delay vs. Supply Voltage



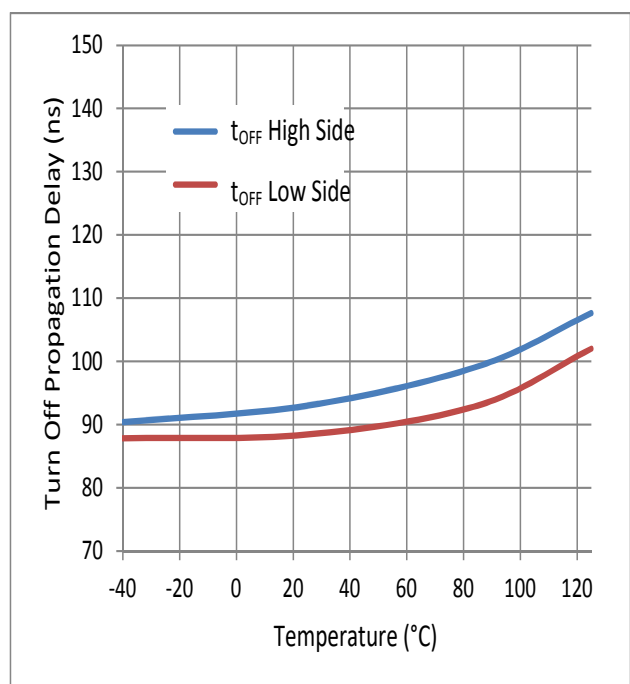
**Figure 6.** Turn-on Propagation Delay vs. Temperature



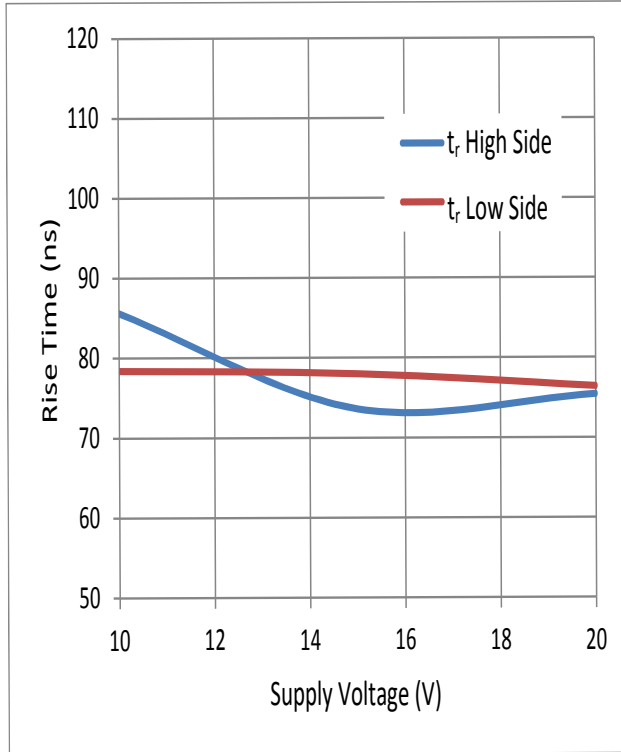
**Figure 7.** Turn-off Propagation Delay vs. Supply Voltage



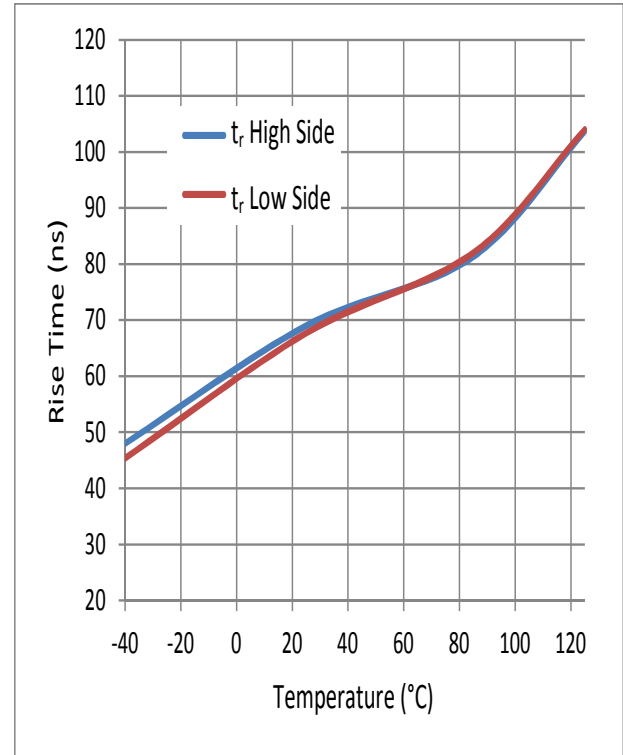
**Figure 8.** Turn-off Propagation Delay vs. Temperature



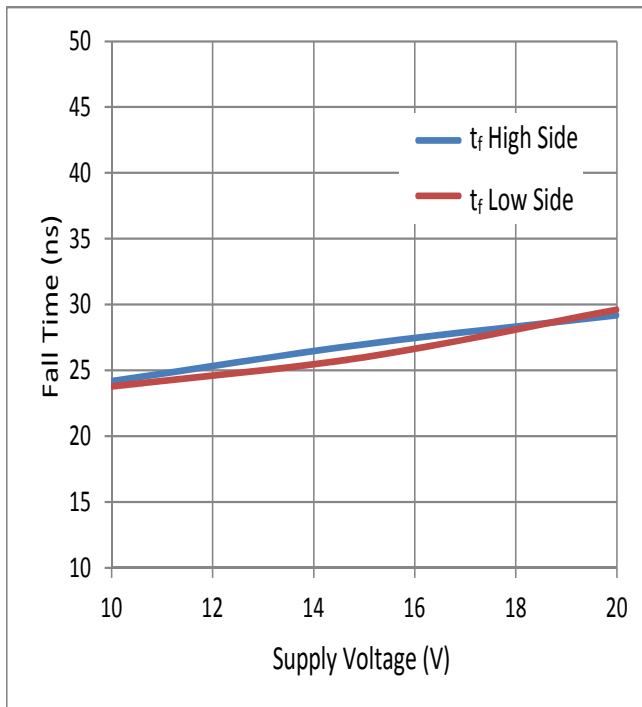
**Figure 9.** Rise Time vs. Supply Voltage



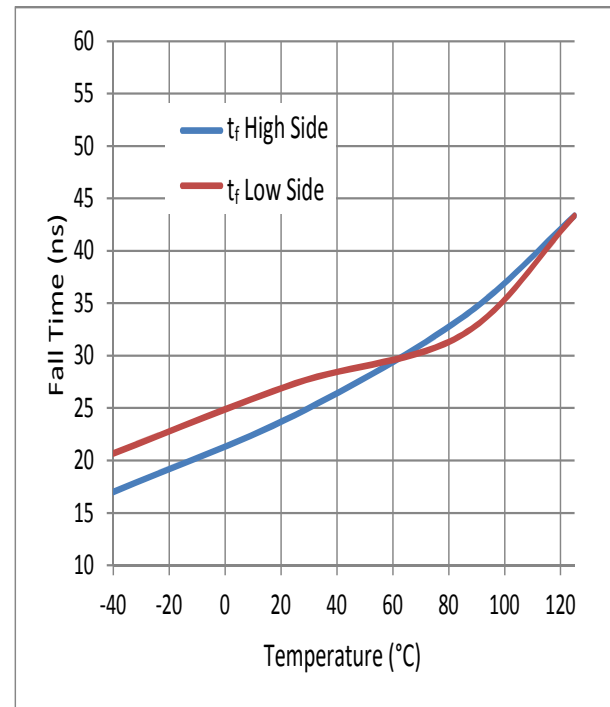
**Figure 10.** Rise Time vs. Temperature



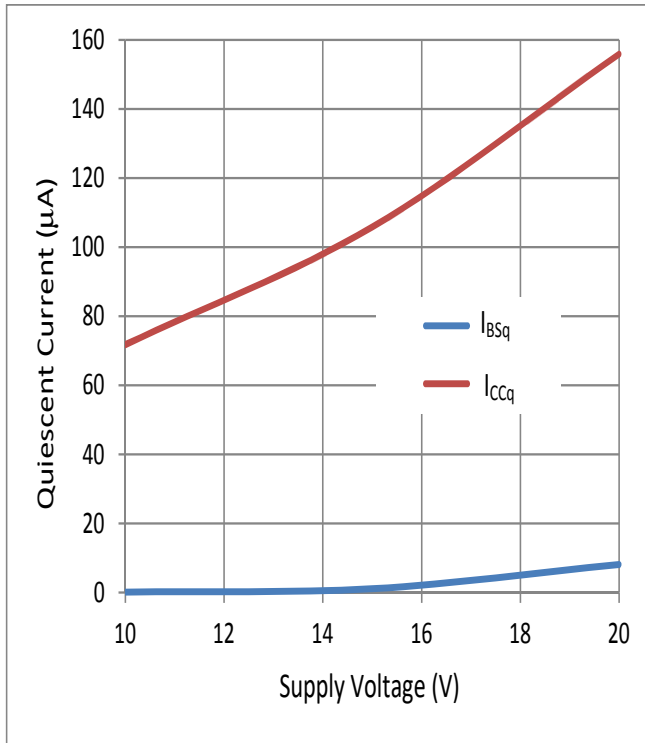
**Figure 11.** Fall Time vs. Supply Voltage



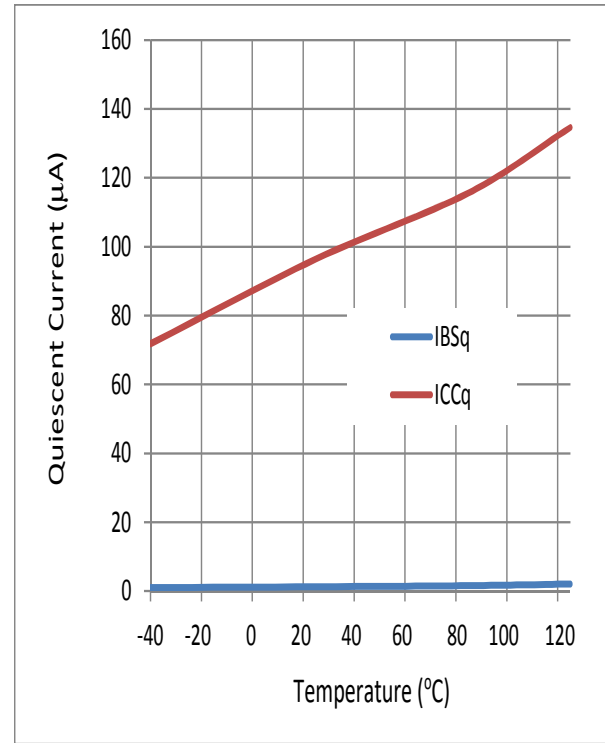
**Figure 12.** Fall Time vs. Temperature



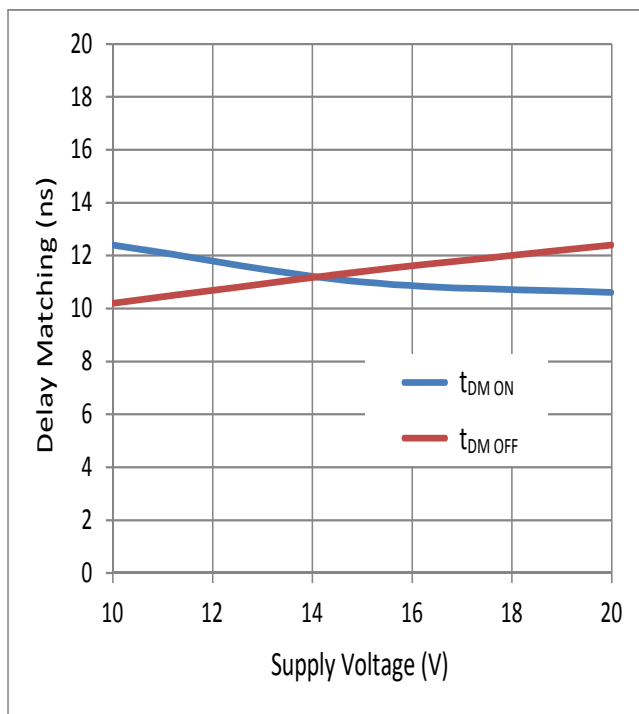
**Figure 13.** Quiescent Current vs. Supply Voltage



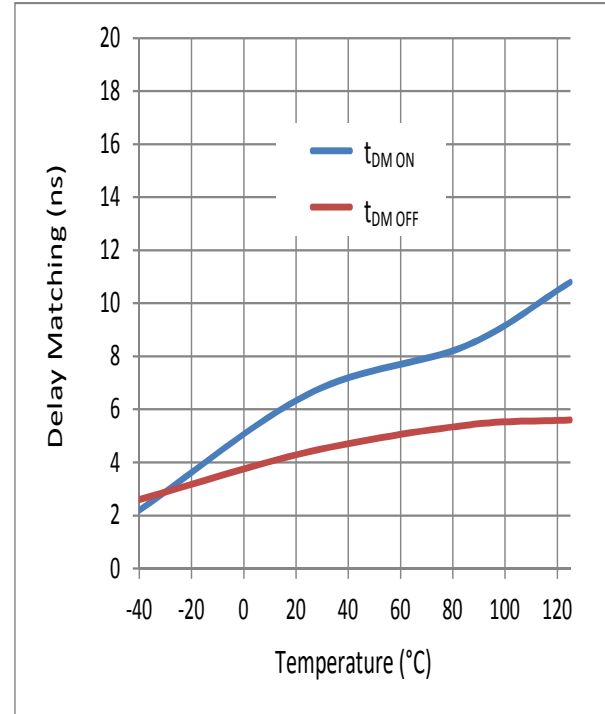
**Figure 14.** Quiescent Current vs. Temperature



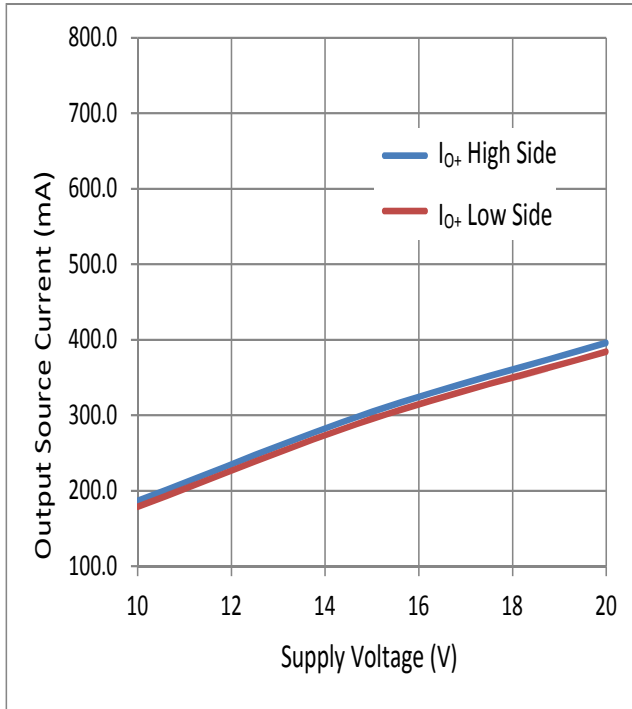
**Figure 15.** Delay Matching vs. Supply Voltage



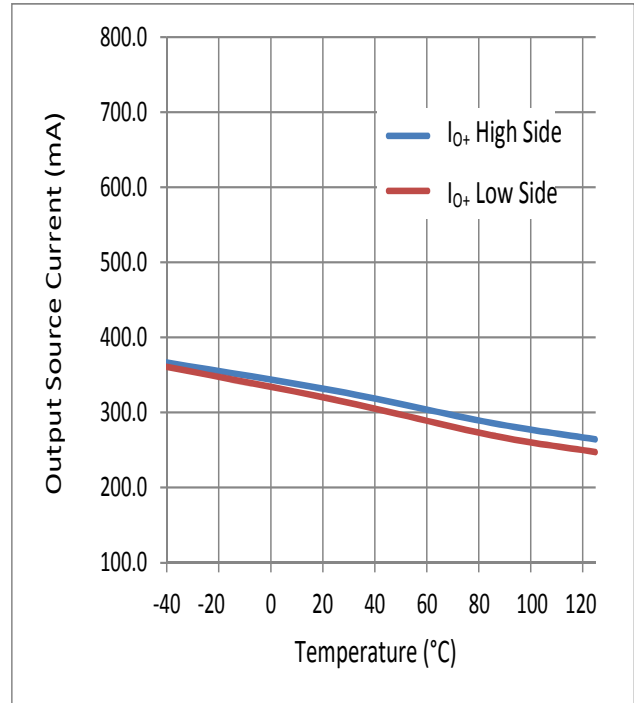
**Figure 16.** Delay Matching vs. Temperature



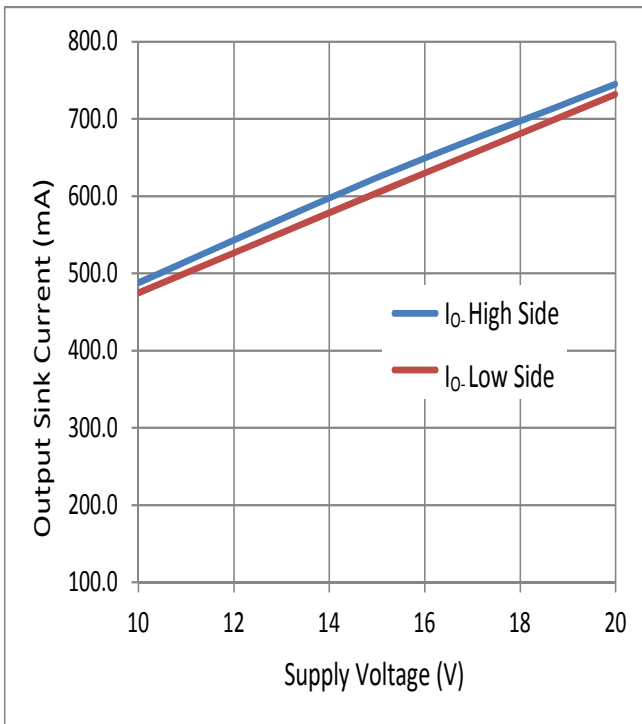
**Figure 17.** Output Source Current vs. Supply Voltage



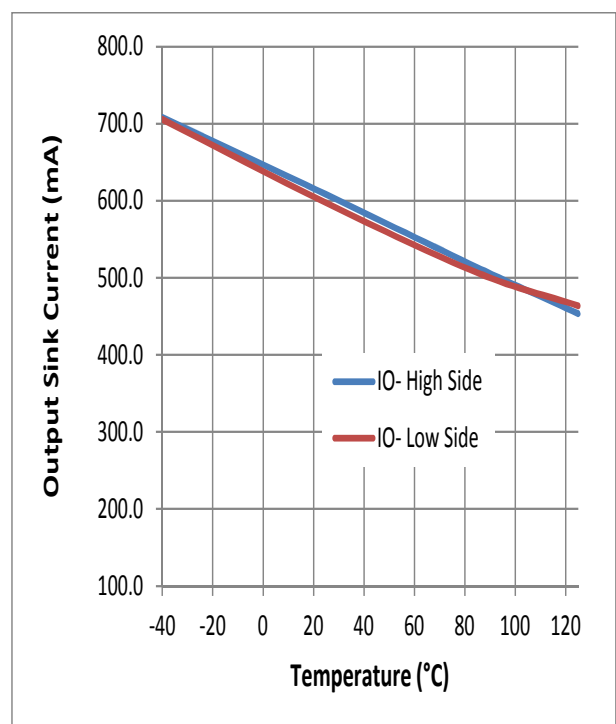
**Figure 18.** Output Source Current vs. Temperature



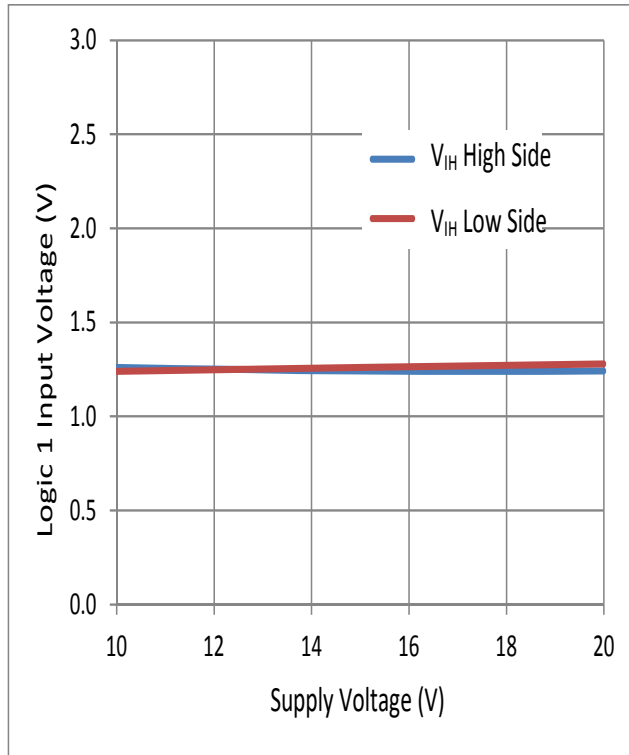
**Figure 19.** Output Sink Current vs. Supply Voltage



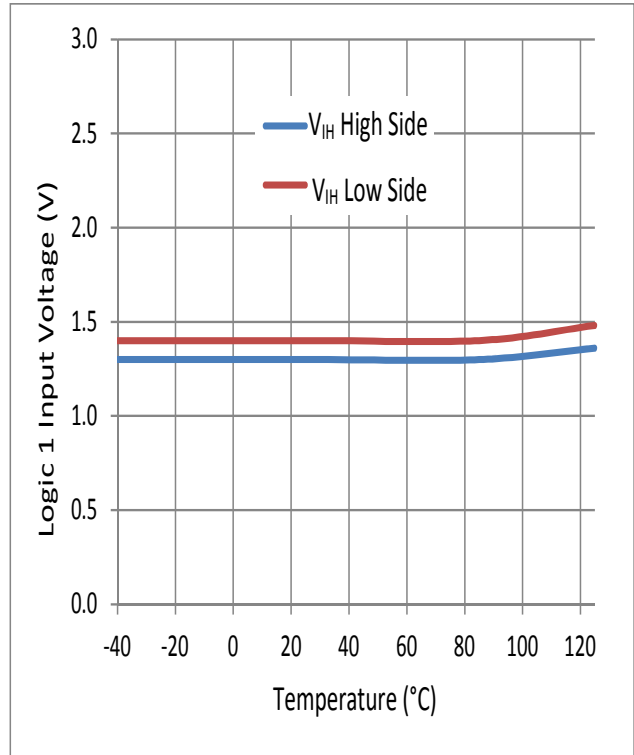
**Figure 20.** Output Sink Current vs. Temperature



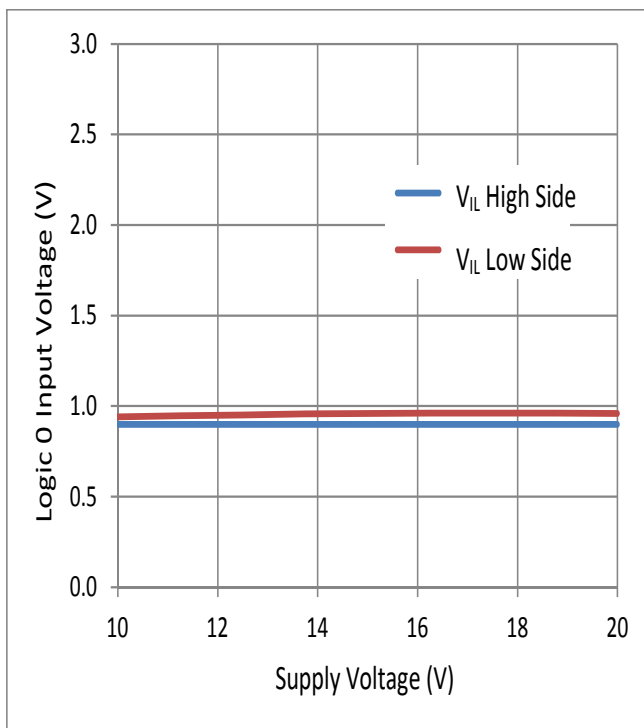
**Figure 21.** Logic 1 Input Voltage vs. Supply Voltage



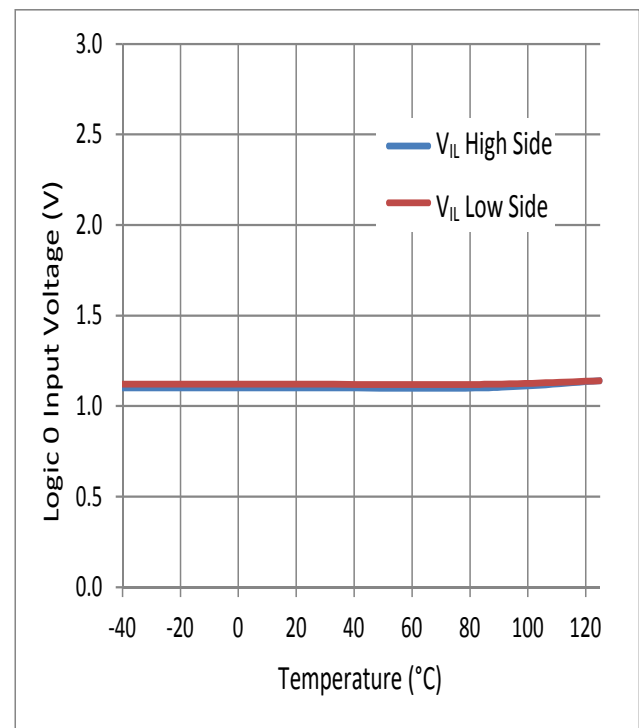
**Figure 22.** Logic 1 Input Voltage vs. Temperature



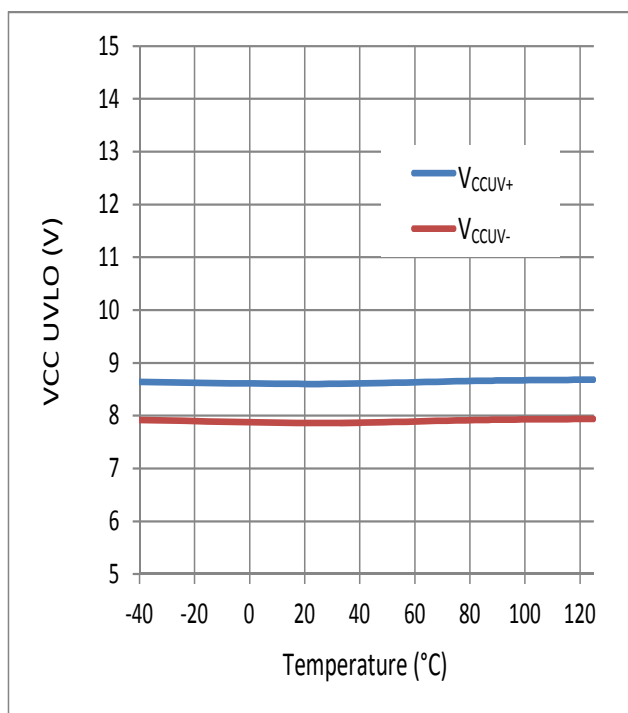
**Figure 23.** Logic 0 Input Voltage vs. Supply Voltage



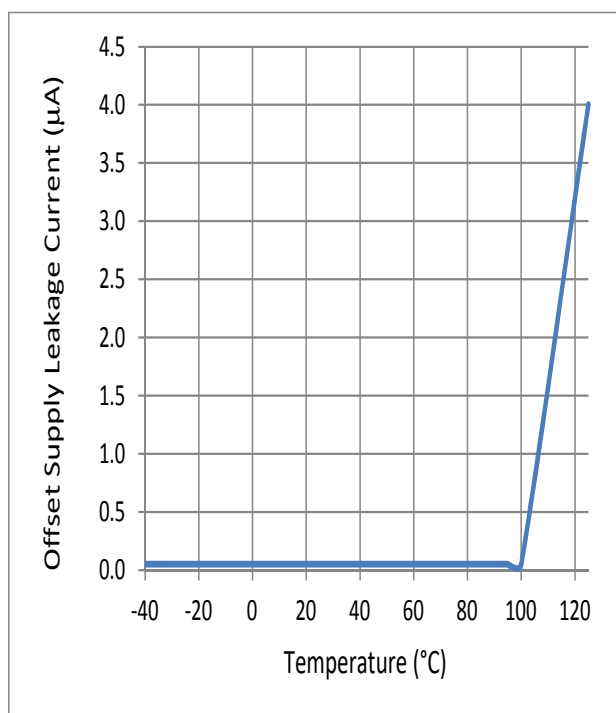
**Figure 24.** Logic 0 Input Voltage vs. Temperature



**Figure 25.**  $V_{CC}$  UVLO vs. Temperature



**Figure 26.** Offset Supply Leakage Current Temperature



## 4 Manufacturing Information

### 4.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. Littelfuse Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** rating as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

| Device  | Moisture Sensitivity Level (MSL) Classification |
|---------|-------------------------------------------------|
| LF2101N | MSL3                                            |

### 4.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

### 4.3 Reflow Profile

Provided in the table below is the IPC/JEDEC J-STD-020 Classification Temperature ( $T_c$ ) and the maximum dwell time the body temperature of these surface mount devices may be ( $T_c - 5$ )°C or greater. The Classification Temperature sets the Maximum Body Temperature allowed for these devices during reflow soldering processes.

| Device  | Classification Temperature( $T_c$ ) | Dwell Time ( $t_p$ ) | Max Reflow Cycles |
|---------|-------------------------------------|----------------------|-------------------|
| LF2101N | 260°C                               | 30 seconds           | 3                 |



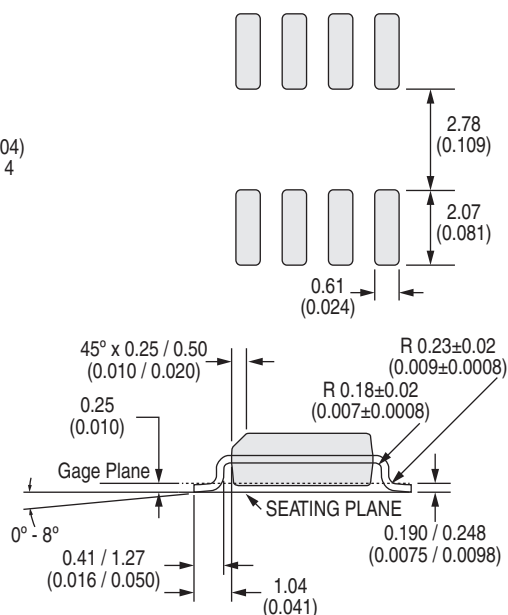
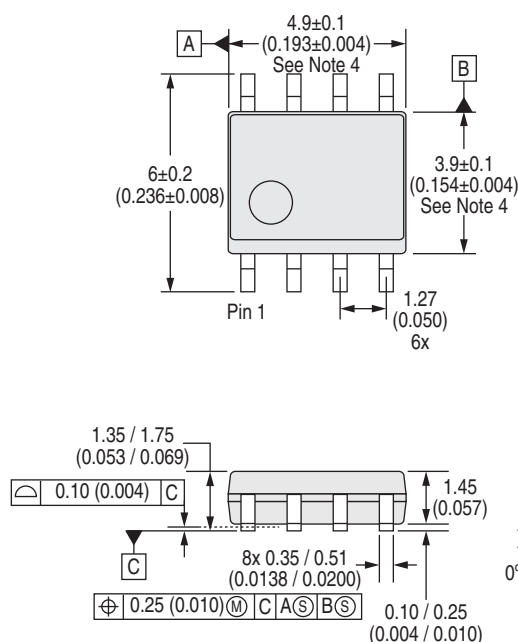
#### 4.4 Board Wash

Littelfuse recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.





## High-Side / Low-Side Gate Driver



1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. Reference JEDEC registration MS-012, variation AA.
4. Not including mold flash, protrusion, or gate burrs  
0.15 (0.006) maximum per end.

Dimensions:  
Minimum / Maximum

Specification: DS-LF2101N-R01  
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