Features

- **maXTouch™ Touchscreen**
  - Two touchscreens with true 12-bit multiple touch reporting and real-time XY tracking for up to 16 concurrent touches per touchscreen
  - Up to 10.1 inch diagonal screen size supported
- **Number of Channels**
  - Electrode grid configurations of up to 24 X and 32 Y lines supported
  - Touchscreens up to 768 channels (subject to other configurations)
  - Up to 64 channels can be allocated as fixed keys (subject to other configurations)
  - Two separate self-capacitance channels for use as touch keys or proximity sensors.
- **Signal Processing**
  - Advanced digital filtering using both hardware engine and firmware
  - Self-calibration
  - Auto drift compensation
  - Adjacent Key Suppression® (AKS®) technology
  - Noise cancellation algorithms for display noise suppression
  - Grip suppression
  - Suppression of unintentional touches
  - Reports one-touch and two-touch gestures
  - Down-scaling and clipping support to match LCD resolution
  - Ultra-fast start-up and calibration for best user experience
  - Supports axis flipping and axis switch-over for portrait and landscape modes
  - Fast and powerful 32-bit processor core
- **Scan Speed**
  - Maximum single touch >120 Hz, subject to configuration
  - Maximum 10 touches >100 Hz, subject to configuration
  - Configurable to allow power/speed optimization
  - Programmable timeout for automatic transition from active to idle states
- **Response Times**
  - Initial latency <25 ms for first touch from idle, subject to configuration
- **Sensors**
  - Shieldless sensor compatible, including fully laminated sensors, touch-on-lens stack-ups and on-cell designs
  - Works with PET or glass sensors, including curved profiles
  - Works with all proprietary sensor patterns recommended by Atmel®
  - Supports gloved touch with different materials up to 2.5 mm thickness, subject to configuration
- **Panel Thickness**
  - Supports different panel thickness
- **Interfaces**
  - I²C slave mode, 400 kHz
- **Dual-rail Power**
  - Digital 2.7V to 3.3V nominal
  - Analog 2.7V to 3.3V nominal
- **Package**
  - 100-pin TQFP 14 × 14 × 1 mm, 0.5 mm lead pitch

Atmel

maXTouch™ 768-channel Touchscreen Controller

mXT768E-AT Automotive Version

maXTouch™

Atmel®

1. Overview of the mXT768E-AT

1.1 Introduction

The Atmel® maXTouch family of touch controllers has set a new industry benchmark for capacitive touchscreens with their low current consumption, fast response time and high levels of accuracy. The mXT768E-AT's single-chip solution offers the benefits of the maXTouch enhanced architecture on devices with touchscreens up to 10.1 in. diagonal:

- **Patented capacitive sensing method** – The mXT768E-AT uses a unique charge-transfer acquisition engine to implement the Atmel-patented QMatrix® capacitive sensing method. This allows the measurement of up to 768 mutual capacitance nodes. Coupled with a state-of-the-art CPU, the entire touchscreen sensing solution can measure, classify and track individual finger touches with a high degree of accuracy.

- **Capacitive Touch Engine (CTE)** – The mXT768E-AT features the E-series acquisition engine, which uses an optimal measurement approach to ensure almost complete immunity from parasitic capacitance on the receiver inputs (Y lines). The engine includes sufficient dynamic range to cope with touchscreen mutual capacitances spanning 0.63 pF to 5 pF. This allows great flexibility for use with the Atmel-proprietary ITO pattern designs. One and two layer ITO sensors are possible using glass or PET substrates.

- **Noise filtering** – Hardware noise processing in the capacitive touch engine provides enhanced autonomous filtering and allows a broad range of noise profiles to be handled. The result is good performance in the presence of charger and LCD noise.

- **Processing power** – The main CPU has two powerful, yet low power, microsequencer coprocessors under its control. These combine to allow the signal acquisition, preprocessing, postprocessing and housekeeping to be partitioned in an efficient and flexible way. This gives ample scope for sensing algorithms, touch tracking or advanced shape-based filtering. An in-circuit reflash can be performed over the chip's hardware-driven interface.

- **Interpreting user intention** – Atmel's mutual capacitance method provides unambiguous multitouch performance. Algorithms in the mXT768E-AT provide optimized touchscreen position filtering for the smooth tracking of touches. Stylus support allows stylus touches to be detected and distinguished from other touches, such as finger touches. The suppression of unintentional touches from the user's gripping fingers, resting palm or touching cheek or ear also help ensure that the user's intentions are correctly interpreted.

- **Self-capacitance channels** – Two sets of self-capacitance channels allow for the implementation of additional touch keys or proximity sensors using Atmel's patented QTouch® technology.

1.2 Understanding Unfamiliar Concepts

If some of the concepts mentioned in this datasheet are unfamiliar, see the following sections for more information:

1.3   Resources

The following datasheet provides essential information on configuring the device:

- *mXT768E-AT 2.1 Protocol Guide*

The following documents may also be useful (available by contacting the Atmel Touch Technology division):

- **Configuring the device:**
  - Application Note: QTAN0058 – *Rejecting Unintentional Touches with the maXTouch Touchscreen Controllers*
  - Application Note: QTAN0078 – *maXTouch Stylus Tuning*

- **Miscellaneous:**
  - Application Note: QTAN0050 – *Using the maXTouch Debug Port*
  - Application Note: QTAN0061 – *maXTouch™ Sensitivity Effects for Mobile Devices*
  - Application Note: QTAN0086 – *Touchscreen Design for Gloved Operation*

- **Touchscreen design and PCB/FPCB layout guidelines:**
  - Application Note: QTAN0054 – *Getting Started with maXTouch Touchscreen Designs*
  - Application Note: QTAN0048 – *maXTouch PCB/FPCB Layout Guidelines*
  - Application Note: QTAN0080 – *Touchscreens Sensor Design Guide*

- **Other documents –** The device uses the same core technology as the mXT224E, so the following documents may also be useful (available by contacting Atmel's Touch Technology division):
  - Application Note: QTAN0083 – *mXT224E Power and Speed Considerations*
  - Application Note: QTAN0052 – *mXT224 Passive Stylus Support*

2. Pinout and Schematic

2.1 Pinout Configuration

mXT768E-AT
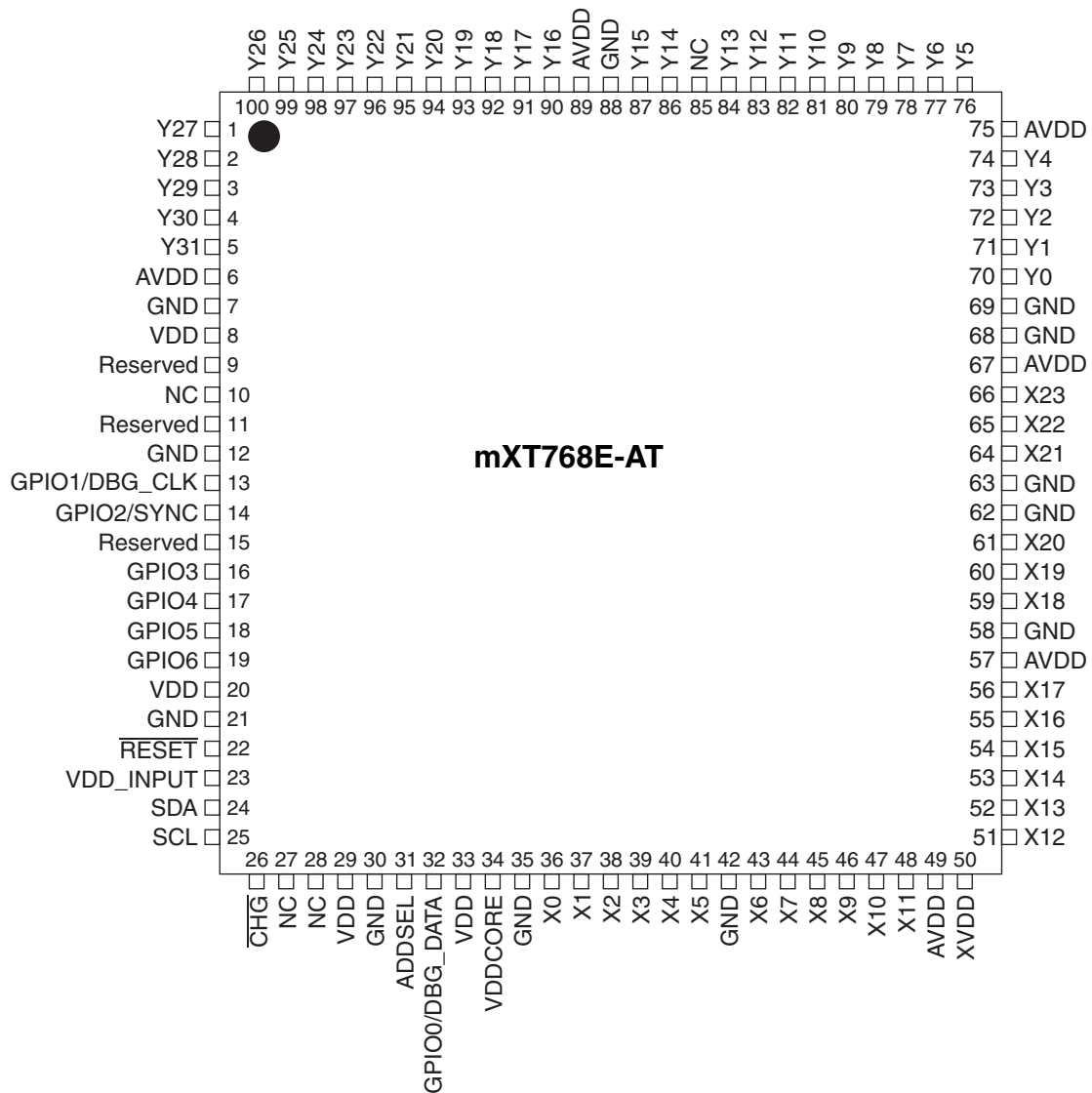
2.2   Pinout Descriptions

Table 2-1.   Pin Listing

Pin	Name	Type	Comments	If Unused, Connect To...
1	Y27	I	Y line connection	Leave open
2	Y28	I	Y line connection	Leave open
3	Y29	I	Y line connection	Leave open
4	Y30	I	Y line connection	Leave open
5	Y31	I	Y line connection	Leave open
6	AVDD	P	Analog power	–
7	GND	P	Ground	–
8	VDD	P	Digital Power	–
9	Reserved	–	Always connect to GND	–
10	NC	–	No connection	Leave open
11	Reserved	–	Always connect to GND	–
12	GND	P	Ground	–
13	GPIO1 DBG_CLK SNS0	I/O	General purpose I/O – Input: GND, Output: leave open Debug clock Self-capacitance sense pin	Make it available as a test pin
14	GPIO2/ SYNC SNSK0	I/O	General purpose I/O External synchronization Self-capacitance sense pin	Input: GND Output: leave open
15	Reserved	–	Always connect to GND	–
16	GPIO3	I/O	General purpose I/O	Input: GND Output: leave open
17	GPIO4 SNS1	I/O	General purpose I/O Self-capacitance sense pin	Input: GND Output: leave open
18	GPIO5 CHRG_IN SNSK1	I/O	General purpose I/O Charger present input Self-capacitance sense pin	Input: GND Output: leave open
19	GPIO6	I/O	General purpose I/O	Input: GND Output: leave open
20	VDD	P	Digital power	–
21	GND	P	Ground	–
22	$\overline{\text{RESET}}$	I	Reset low; has internal 20 kΩ to 60 kΩ pull-up resistor	Vdd [1]
23	VDD_INPUT	–	For factory use only – connect to VDD	VDD
24	SDA [1]	OD	Serial Interface Data	VDD
25	SCL [1]	OD	Serial Interface Clock	VDD
26	$\overline{\text{CHG}}$ [2]	OD	State change interrupt	Leave open
27	NC	–	No connection	–
28	NC	–	No connection	–

Table 2-1. Pin Listing (Continued)

Pin	Name	Type	Comments	If Unused, Connect To...
29	VDD	P	Digital power	–
30	GND	P	Ground	–
31	ADDSEL	I	I^2C address select	–
32	GPIO0 DBG_DATA	I/O	General purpose I/O – Input: GND, Output: leave open Debug data	Make it available as a test pin
33	VDD	P	Digital power	–
34	VDDCORE	P	Digital core power. Must be connected as in schematics (see Section 2.3 on page 9)	–
35	GND	P	Ground	–
36	X0	O	X matrix drive line	Leave open
37	X1	O	X matrix drive line	Leave open
38	X2	O	X matrix drive line	Leave open
39	X3	O	X matrix drive line	Leave open
40	X4	O	X matrix drive line	Leave open
41	X5	O	X matrix drive line	Leave open
42	GND	P	Ground	–
43	X6	O	X matrix drive line	Leave open
44	X7	O	X matrix drive line	Leave open
45	X8	O	X matrix drive line	Leave open
46	X9	O	X matrix drive line	Leave open
47	X10	O	X matrix drive line	Leave open
48	X11	O	X matrix drive line	Leave open
49	AVDD	P	Analog power	–
50	XVDD	P	X line regulator bypass – see schematics in Section 2.3 on page 9	–
51	X12	O	X matrix drive line	Leave open
52	X13	O	X matrix drive line	Leave open
53	X14	O	X matrix drive line	Leave open
54	X15	O	X matrix drive line	Leave open
55	X16	O	X matrix drive line	Leave open
56	X17	O	X matrix drive line	Leave open
57	AVDD	P	Analog power	–
58	GND	P	Ground	–
59	X18	O	X matrix drive line	Leave open
60	X19	O	X matrix drive line	Leave open
61	X20	O	X matrix drive line	Leave open
62	GND	P	Ground	–

Table 2-1. Pin Listing (Continued)

Pin	Name	Type	Comments	If Unused, Connect To...
63	GND	P	Ground	–
64	X21	O	X matrix drive line	Leave open
65	X22	O	X matrix drive line	Leave open
66	X23	O	X matrix drive line	Leave open
67	AVDD	P	Analog power	–
68	GND	P	Ground	–
69	GND	P	Ground	–
70	Y0	I	Y line connection	Leave open
71	Y1	I	Y line connection	Leave open
72	Y2	I	Y line connection	Leave open
73	Y3	I	Y line connection	Leave open
74	Y4	I	Y line connection	Leave open
75	AVDD	P	Analog power	–
76	Y5	I	Y line connection	Leave open
77	Y6	I	Y line connection	Leave open
78	Y7	I	Y line connection	Leave open
79	Y8	I	Y line connection	Leave open
80	Y9	I	Y line connection	Leave open
81	Y10	I	Y line connection	Leave open
82	Y11	I	Y line connection	Leave open
83	Y12	I	Y line connection	Leave open
84	Y13	I	Y line connection	Leave open
85	NC	–	No connection	Leave open
86	Y14	I	Y line connection	Leave open
87	Y15	I	Y line connection	Leave open
88	GND	P	Ground	–
89	AVDD	P	Analog power	–
90	Y16	I	Y line connection	Leave open
91	Y17	I	Y line connection	Leave open
92	Y18	I	Y line connection	Leave open
93	Y19	I	Y line connection	Leave open
94	Y20	I	Y line connection	Leave open
95	Y21	I	Y line connection	Leave open
96	Y22	I	Y line connection	Leave open
97	Y23	I	Y line connection	Leave open

Table 2-1. Pin Listing (Continued)

Pin	Name	Type	Comments	If Unused, Connect To...
98	Y24	I	Y line connection	Leave open
99	Y25	I	Y line connection	Leave open
100	Y26	I	Y line connection	Leave open

1. It is recommend that $\overline{\text{RESET}}$ is connected to the host system.

2. $\overline{\text{CHG}}$ is momentarily set (approximately 100 ms) as an input after power-up or reset for diagnostic purposes.

I	Input only	OD	Open drain output	O	Output only, push-pull
P	Ground or power				

2.3   Schematics

2.3.1   I²C Mode – Digital Supply 2.5 – 3.3 V
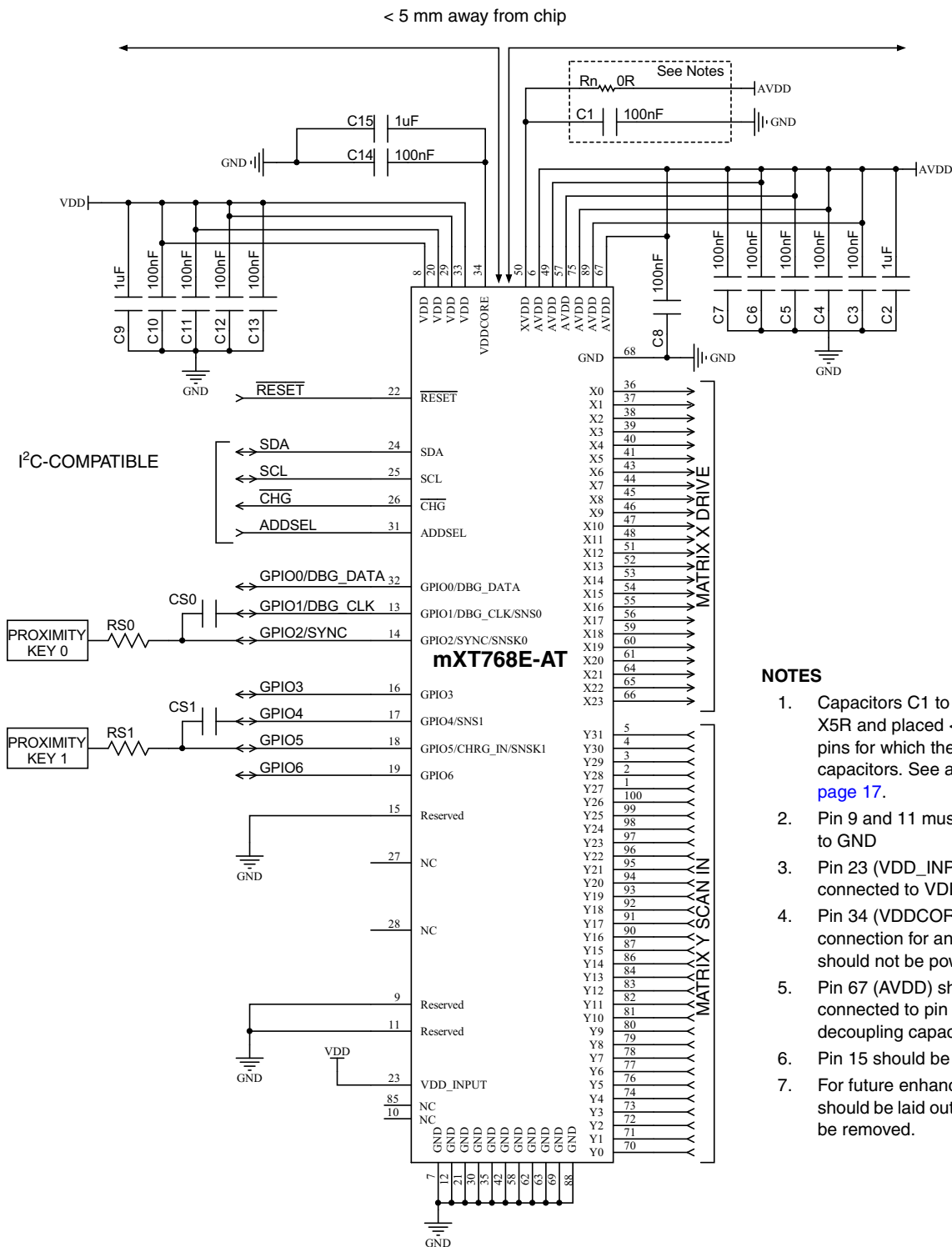
NOTES

1. Capacitors C1 to C14 must be X7R or X5R and placed <5 mm away from the pins for which they act as bypass capacitors. See also Section 4.8.1 on page 17.

2. Pin 9 and 11 must always be connected to GND

3. Pin 23 (VDD_INPUT) should be connected to VDD.

4. Pin 34 (VDDCORE) is a decoupling connection for an internal circuit and should not be powered.

5. Pin 67 (AVDD) should be closely connected to pin 68 (GND) by a decoupling capacitor.

6. Pin 15 should be connected to GND.

7. For future enhancements, boards should be laid out so that Rn and C1 can be removed.

3. Touchscreen Basics

3.1 Sensor Construction

A touchscreen is usually constructed from a number of transparent electrodes. These are typically on a glass or plastic substrate. They can also be made using non-transparent electrodes, such as copper or carbon. Electrodes are normally formed by etching a material called Indium Tin Oxide (ITO). This is a brittle ceramic material, of high optical clarity and varying sheet resistance. Thicker ITO yields lower levels of resistance (perhaps tens to hundreds of Ω/square) at the expense of reduced optical clarity. Lower levels of resistance are generally more compatible with capacitive sensing. Thinner ITO leads to higher levels of resistance (perhaps hundreds to thousands of Ω/square) with some of the best optical characteristics.

Interconnecting tracks formed in ITO can cause problems. The excessive RC time constants formed between the resistance of the track and the capacitance of the electrode to ground can inhibit the capacitive sensing function. In such cases, ITO tracks should be replaced by screen printed conductive inks (non-transparent) outside the touchscreen's viewing area.

A range of trade-offs also exist with regard to the number of layers used for construction. Atmel has pioneered single-layer ITO capacitive touchscreens. For many applications these offer a near optimum cost/performance balance. With a single layer screen, the electrodes are all connected using ITO out to the edges of the sensor. From there the connection is picked up with printed silver tracks. Sometimes two overprinted silver tracking layers are used to reduce the margins between the edge of the substrate and the active area of the sensor.

Two-layer designs can have a strong technical appeal where ultra-narrow edge margins are required. They are also an advantage where the capacitive sensing function needs to have a very precise cut-off as a touch is moved to just off the active sensor area. With a two-layer design the QMatrix transmitter electrodes are normally placed nearest the bottom and the receiver electrodes nearest the top. The separation between layers can range from hundreds of nanometers to hundreds of microns, with the right electrode design and considerations of the sensing environment.

3.2 Electrode Configuration

The specific electrode designs used in Atmel's touchscreens are the subject of various patents and patent applications. Further information is available on request.

The device supports various configurations of electrodes as summarized below:

Touchscreens: 2 Touchscreens allowed
3 X × 3 Y minimum (depends on screen resolution)
24 X × 32 Y maximum (subject to other configurations)

Keys: 2 Key Arrays allowed
Each up to 32 keys (subject to other configurations)

3.3 Scanning Sequence

All channels are scanned in sequence by the device. The channels are scanned by measuring capacitive changes at the intersections formed between the first X line and all the odd Y lines, followed by the intersections between the first X line and all the even Y lines. Then the intersections between the next X line and the odd and even Y lines are scanned, and so on, until all X and Y combinations have been measured.

The device can be configured in various ways. It is possible to disable some channels so that they are not scanned at all. This can be used to improve overall scanning time.

3.4 Touchscreen Sensitivity

3.4.1 Adjustment

Sensitivity of touchscreens can vary across the extents of the electrode pattern due to natural differences in the parasitics of the interconnections, control chip, and so on. An important factor in the uniformity of sensitivity is the electrode design itself. It is a natural consequence of a touchscreen pattern that the edges form a discontinuity and hence tend to have a different sensitivity. The electrodes at the far edges do not have a neighboring electrode on one side and this affects the electric field distribution in that region.

A sensitivity adjustment is available for the whole touchscreen. This adjustment is a basic algorithmic threshold that defines when a channel is considered to have enough signal change to qualify as being in detect.

The device supports mixed configurations of different touch objects, each having independent threshold controls to allow fine tuning with mixed configurations.

3.4.2 Mechanical Stackup

The mechanical stackup refers to the arrangement of material layers that exist above and below a touchscreen. The arrangement of the touchscreen in relation to other parts of the mechanical stackup has an effect on the overall sensitivity of the screen. QMatrix technology has an excellent ability to operate in the presence of ground planes close to the sensor. QMatrix sensitivity is attributed more to the interaction of the electric fields between the transmitting (X) and receiving (Y) electrodes than to the surface area of these electrodes. For this reason, stray capacitance on the X or Y electrodes does not strongly reduce sensitivity.

Front panel dielectric material has a direct bearing on sensitivity. Plastic front panels are usually suitable up to about 1.2 mm, and glass up to about 2.5 mm (dependent upon the screen size and layout). The thicker the front panel, the lower the signal-to-noise ratio of the measured capacitive changes and hence the lower the resolution of the touchscreen. In general, glass front panels are near optimal because they conduct electric fields almost twice as easily as plastic panels.

4. Detailed Operation

4.1 Power-up/Reset

There is an internal Power-on Reset (POR) in the device.

The device must be held in $\overline{\text{RESET}}$ (active low) while both the digital and analog power supplies (Vdd and AVdd) are powering up. If a slope or slew is applied to the digital or analog supplies, Vdd and AVdd must reach their nominal values before the $\overline{\text{RESET}}$ signal is deasserted (that is, goes high). This is shown in Figure 4-1. See Section 7.2 on page 29 for nominal values for Vdd and AVdd.

Figure 4-1.   Power Sequencing on the mXT768E-AT
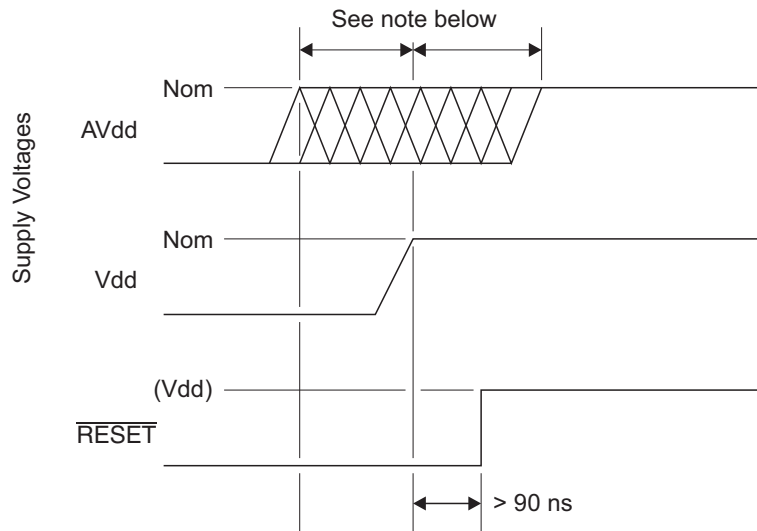
Note: Vdd and AVdd can be powered up in either order.
There is no prerequisite for the length of time between Vdd and AVdd powering up.

Note that there are no specific power-up, or power-down sequences required for the mXT768E-AT. This means that the digital or analog supplies can be applied independently and in any order during power-up.

After power-up, the device takes ~46.5 ms before it is ready to start communications. Vdd must drop to below 1.45V in order to effect a proper POR. See Section 7 for further specifications.

If the $\overline{\text{RESET}}$ line is released before the AVDD supplies have reached their nominal voltage (see Figure 4-2), then some additional operations need to be carried out by the host. There are two options open to the host controller:

- Start the part in deep sleep mode and then send the command sequence to set the cycle time to wake the part and allow it to run normally. Note that in this case a calibration command is also needed.
- Send a reset command.

Figure 4-2. Power Sequencing on the mXT768E-AT – Late rise on AVDD
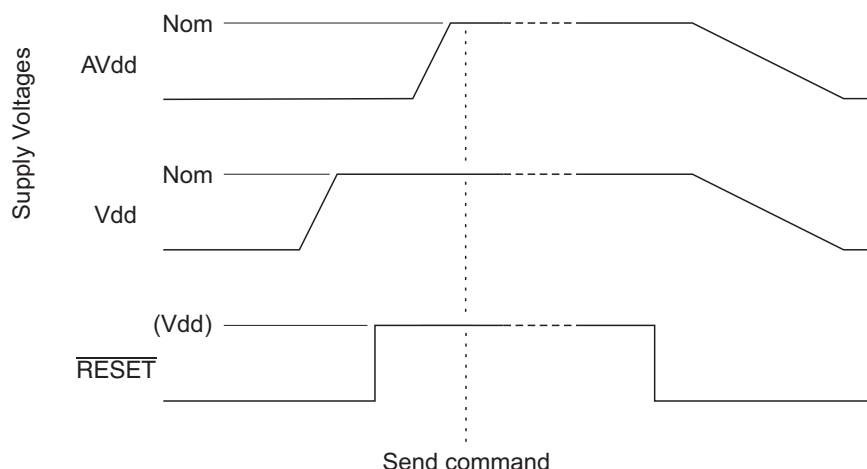
The $\overline{\text{RESET}}$ pin can be used to reset the device whenever necessary. The $\overline{\text{RESET}}$ pin must be asserted low for at least 90 ns to cause a reset. After releasing the $\overline{\text{RESET}}$ pin the device takes ~46.5 ms before it is ready to start communications. It is recommended to connect the $\overline{\text{RESET}}$ pin to a host controller to allow it to initiate a full hardware reset without requiring a power-down.

Note that the voltage level on the RESET pin of the device must never exceed Vdd (digital supply voltage).

A software reset command can be used to reset the chip (refer to the Command Processor object in the *mXT768E-AT 2.1 Protocol Guide*). A software reset takes ~194 ms. After the chip has finished it asserts the $\overline{\text{CHG}}$ line to signal to the host that a message is available. The reset flag is set in the Message Processor object to indicate to the host that it has just completed a reset cycle. This bit can be used by the host to detect any unexpected brownout events. This allows the host to take any necessary corrective actions, such as reconfiguration.

A checksum check is performed on the configuration settings held in the nonvolatile memory. If the checksum does not match a stored copy of the last checksum, then this indicates that the settings have become corrupted. This is signaled to the host by setting the configuration error bit in the message data for the Command Processor object (refer to the *mXT768E-AT 2.1 Protocol Guide* for more information).

Note that the $\overline{\text{CHG}}$ line is momentarily set (approximately 100 ms) as an input after power-up or reset for diagnostic purposes. It is therefore particularly important that the line should be allowed to float high via the $\overline{\text{CHG}}$ line pull-up resistors during this period. It should not be driven by the host.

4.2 Calibration

Calibration is the process by which a sensor chip assesses the background capacitance on each channel. Channels are only calibrated on power-up and when:

- The channel is enabled (that is, activated).

OR

- The channel is already enabled and one of the following applies:
    - The channel is held in detect for longer than the Touch Automatic Calibration setting (refer to the *mXT768E-AT 2.1 Protocol Guide* for more information on TCHAUTOCAL setting in the Acquisition Configuration object).
    - The signal delta on a channel is at least the touch threshold (TCHTHR) in the anti-touch direction, while no other touches are present on the channel matrix (refer to the *mXT768E-AT 2.1 Protocol Guide* for more information on the TCHTHR field in the Multiple Touch Touchscreen and Key Array objects).
    - The host issues a recalibrate command.
    - Certain configuration settings are changed.

A status message is generated on the start and completion of a calibration.

Note that the device performs a global calibration; that is, all the channels are calibrated together.

4.3 Operational Modes

The device operates in two modes: active (touch detected) and idle (no touches detected). Both modes operate as a series of burst cycles. Each cycle consists of a short burst (during which measurements are taken) followed by an inactive sleep period. The difference between these modes is the length of the cycles. Those in idle mode typically have longer sleep periods. The cycle length is configured using the IDLEACQINT and ACTVACQINT settings in the Power Configuration object. In addition, an Active to Idle timeout (ACTV2IDLETO) setting is provided.

Refer to the *mXT768E-AT 2.1 Protocol Guide* for full information on how these modes operate, and how to use the settings provided.

4.4 Touchscreen Layout

The physical matrix can be configured to have one or more touch objects. These are configured using the appropriate touch objects (Multiple Touch Touchscreen,Key Array, Proximity Sensor). It is not mandatory to have all the allowable touch objects present. The objects are disabled by default so only those that you wish to use need to be enabled. Refer to the *mXT768E-AT 2.1 Protocol Guide* for more information on configuring the touch objects.

When designing the physical layout of the touch panel, obey the following rules:

- Each touch object should be a regular rectangular shape in terms of the lines it uses.
- Touch objects can share X and Y lines, as necessary. Note, however, that the first instance (instance 0) of the Multiple Touch Touchscreen T9 object cannot share Ylines if the Shieldless T56 object is enabled.
- The design of the touch objects does not physically need to be on a strict XY grid pattern.

4.5 Signal Processing

4.5.1 Adjacent Key Suppression Technology

Adjacent Key Suppression (AKS) technology is a patented method used to detect which touch object is touched when objects are located close together. A touch in a group of AKS objects is only indicated on the object in that group that is touched first. This is assumed to be the intended object. Once an object in an AKS group is in detect, there can be no further detections within that group until the object is released. Objects can be in more than one AKS group.

Note that AKS technology works best when it operates in conjunction with a detect integration setting of several acquisition cycles.

The device has two levels of AKS. The first level works between the touch objects (Multiple Touch Touchscreen T9, Key Array T15, Proximity Key T52). The touch objects are assigned to AKS groups. If a touch occurs within one of the touch objects in a group, then touches within other objects inside that group are suppressed. For example, if a Touchscreen and Key Array are placed in the same AKS group, then a touch in the Touchscreen will suppress touches in the Key Array, and vice versa.

The second level of AKS is internal AKS within an individual Key Array object (note that internal AKS is not present on other types of touch objects, only a Key Array). If internal AKS is enabled, then when one key is touched, touches on all the other keys within the Key Array are suppressed.

AKS is configured using the touch objects (Multiple Touch Touchscreen T9,or Key Array T15, Proximity Key T52). Refer to the *mXT768E-AT 2.1 Protocol Guide* for more information.

Note: If a touch is in detect and then AKS is enabled, that touch will not be forced out of detect. It will not go out of detect until the touch is released. AKS will then operate normally. This applies to both levels of AKS.

4.5.2 Detection Integrator

The device features a touch detection integration mechanism. This acts to confirm a detection in a robust fashion. A counter is incremented each time a touch has exceeded its threshold and has remained above the threshold for the current acquisition. When this counter reaches a preset limit the sensor is finally declared to be touched. If, on any acquisition, the signal is not seen to exceed the threshold level, the counter is cleared and the process has to start from the beginning.

The detection integrator is configured using the appropriate touch objects (Multiple Touch Touchscreen T9, Key Array T15). Refer to the *mXT768E-AT 2.1 Protocol Guide* for more information.

4.5.3 Digital Filtering and Noise Suppression

The mXT768E-AT supports the on-chip filtering of the acquisition data received from the sensor. Specifically, the Noise Suppression T48 object provides an algorithm to suppress the effects of noise (for example, from a noisy charger plugged into the user's product). This algorithm can automatically adjust some of the acquisition parameters on-the-fly to filter the analog-to-digital conversions (ADCs) received from the sensor. The algorithm can make use of a Grass Cutter (which rejects any samples outside a predetermined limit) and a Median Filter (which rejects the highest and lowest sets of accumulated ADCs, leaving the center set).

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Noise suppression is triggered when a noise source is detected (typically when a charger is turned on). A hardware trigger can be implemented using the CHRG_IN pin. Alternatively, the host's driver code can indicate when a noise source is present.

A Mean Acquisition Mode can be used for acquisition when the noise suppression algorithm is in its off state. This aids stylus operation, as the quieter reported position gives better linearity.

An alternative burst mode on the X lines, known as Dual X Drive, is provided. This improves the signal-to-noise ratio (SNR) on a closely spaced X sensor matrix (when finger touches are likely to cover more than one X line).

Refer to the *mXT768E-AT 2.1 Protocol Guide* for more information on the Noise Suppression T48 object.

4.5.4   Stylus Support

The mXT768E-AT allows for the particular characteristics of stylus touches, whilst still allowing conventional finger touches to be detected. Stylus touches are configured by the Stylus T47 object. There is one instance of the Stylus T47 object for each Multiple Touch Touchscreen T9 object present on the device.

For example, stylus support ensures that the small touch area of a stylus registers as a touch, as this would otherwise by considered too small for the touchscreen. Additionally, there are controls to distinguish a stylus touch from an unwanted approaching finger (such as on the hand holding the stylus).

The touch sensitivity and threshold controls for stylus touches are configured separately from those for conventional finger touches so that both types of touches can be accommodated.

4.5.5   Grip Suppression

The mXT768E-AT has a grip suppression mechanism to suppress false detections when the user grips a handheld device.

Grip suppression works by specifying a boundary around a touchscreen, within which touches can be suppressed whilst still allowing touches in the center of the touchscreen. This ensures that a "rolling" hand touch (such as when a user grips a mobile device) is suppressed. A "real" (finger) touch towards the center of the screen is allowed.

Grip suppression is configured using the Grip Suppression T40 object. There is one instance of the Grip Suppression T40 object for each Multiple Touch Touchscreen T9 object present on the device. Refer to the *mXT768E-AT 2.1 Protocol Guide* for more information.

4.5.6   Unintentional Touch Suppression

The Touch Suppression T42 object provides a mechanism to suppress false detections from unintentional touches from a large body area, such as from a face, ear or palm. This mechanism is enhanced by another mechanism (known as distance touch suppression) that operates in conjunction with large object suppression to suppress false touches only if they are less than a specified distance from a suppressed touch, whilst any touches greater than this distance remain unsuppressed. The Touch Suppression T42 object also provides Maximum Touch Suppression to suppress all touches if more than a specified number of touches has been detected. There is one instance of the Touch Suppression T42 object for each Multiple Touch Touchscreen T9 object present on the device. Refer to the *mXT768E-AT 2.1 Protocol Guide* for more information.

4.5.7 Gestures

The device supports the on-chip processing of touches so that specific gestures can be detected. These may be a one-touch gesture (such as a tap or a drag) or they may be a two-touch gesture (such as a pinch or a rotate).

Gestures are configured using the One-touch Gesture Processor T24 and the Two-touch Gesture Processor T27 objects. There is one instance of the One-touch Gesture Processor T24 and the Two-touch Gesture Processor T27 objects for each Multiple Touch Touchscreen T9 object present on the device. Refer to the *mXT768E-AT 2.1 Protocol Guide* for more information on gestures and their configuration.

4.6 GPIO Pins

The mXT768E-AT has seven GPIO pins, which can be set as either input or output pins, as required. Four of the GPIO pins can be set as PWM pins. The GPIO pins are configured using the GPIO/PWM Configuration T19 object.

4.7 Self-capacitance Channels

The mXT768E-AT has two self-capacitance channels for the implementation of individual touch keys or proximity sensors. These are separate from the touchscreen matrix and instead use Atmel's QTouch technology specifically designed for touch-key applications.

By increasing the sensitivity, these channels can be used as effective proximity sensors, allowing the presence of a nearby object (typically a hand) to be detected. In this scenario a large electrode size can be used, which is extremely effective in increasing the sensitivity of the detector. The value of the Cs sampling capacitor (see Section 4.8.6 on page 18) will also need to be increased to ensure improved sensitivity.

With the proper electrode and circuit design, the mXT768E-AT will project a touch or proximity field to several centimeters through any dielectric.

4.8 Circuit Components

4.8.1 Bypass Capacitors

Each power supply (Vdd and AVdd) requires a 1 µF bypass capacitor. In addition, there should be a 100 nF bypass capacitor on each power trace. The capacitors should be ceramic X7R or X5R. See the schematics in Section 2.3 on page 9 for more details.

The PCB traces connecting the bypass capacitors to the pins of the device must not exceed 5 mm in length. This limits any stray inductance that would reduce filtering effectiveness. See also Section 7.9 on page 33.

4.8.2 Supply Quality

While the device has good Power Supply Rejection Ratio properties, poorly regulated and/or noisy power can significantly reduce performance. See Section 7.9 on page 33.

Always operate the device with a well-regulated and clean AVdd supply. It supplies the sensitive analog stages in the device.

4.8.3 Supply Sequencing

Vdd and AVdd can be powered independently of each other without damage to the device. Vdd and AVdd should be supplied with the same voltage unless specified by Atmel.

Make sure that any lines connected to the device are below or equal to Vdd during power-up. For example, if $\overline{\text{RESET}}$ is supplied from a different power domain to the mXT768E-AT's Vdd pin, make sure that it is held low when Vdd is off. If this is not done, the $\overline{\text{RESET}}$ signal could parasitically couple power via the mXT768E-AT's $\overline{\text{RESET}}$ pin into the Vdd supply.

4.8.4 Oscillator

An oscillator is not required.

4.8.5 Decoupling Requirements

Certain pins have specific decoupling requirements:

- VDD_INPUT (Pin 23) should be connected to VDD.
- VDDCORE (Pin 34) is a decoupling connection for an internal circuit and should not be powered.
- AVDD (Pin 67) should be closely connected to pin 68 (GND) by a decoupling capacitor.
- For future enhancements, boards should be laid out so that Rn and C1 can be removed.

See also the schematics in Section 2.3 on page 9.

4.8.6 Cs Sample Capacitors

The Cs capacitors are the charge sensing sample capacitors for the two self-capacitance channels. The optimal Cs values depend on the corresponding key electrode design, the thickness of the panel and its dielectric constant, and the purpose of the design (touch key or proximity sensor). Thicker panels require larger values of Cs. Larger values of Cs demand higher stability and better dielectric to ensure reliable sensing. Values can be in the range 4.7 nF for a key to 100 nF for a proximity sensor.

The value of the Cs capacitors should be chosen such that a light touch on a key mounted in a production unit or a prototype panel causes a reliable detection. The chosen Cs value should never be so large that the key signals exceed ~1750, as reported by the chip in the debug data.

The Cs capacitors should be a stable type, such as X7R ceramic or PPS film. For more consistent sensing from unit to unit, 5 percent tolerance capacitors are recommended.

4.8.7 Rs Series Resistors

The Rs series resistors in the self-capacitance circuit are inline with the electrode connections (close to the mXT768E-AT chip) and are used to limit electrostatic discharge (ESD) currents and to suppress radio frequency (RF) interference. The value should be chosen so that the sensor is fully charged. This can be measured using a coin. Refer to QTAN0079, *Buttons, Sliders and Wheels Sensor Design Guide*, (downloadable from the Touch Technology area of Atmel's website) for details.

Although these resistors may be omitted, the device may become susceptible to external noise or radio frequency interference (RFI). For details on how to select these resistors refer to QTAN0079, *Buttons, Sliders and Wheels Sensor Design Guide*.

4.8.8 PCB Cleanliness

Modern no-clean-flux is generally compatible with capacitive sensing circuits.

> **CAUTION:** If a PCB is reworked to correct soldering faults relating to any of the device, or to any associated traces or components, be sure that you fully understand the nature of the flux used during the rework process. Leakage currents from hygroscopic ionic residues can stop capacitive sensors from functioning. If you have any doubts, a thorough cleaning after rework may be the only safe option.

4.9 PCB Layout

See for general advice on PCB layout.

4.10 Debugging

The device provides a mechanism for obtaining raw data for development and testing purposes by reading data from the Diagnostic Debug T37 object. Refer to the *mXT768E-AT 2.1 Protocol Guide* for more information on this object.

A second mechanism is provided that allows the host to read the real-time raw data using the low-level debug port. This can be accessed via the SPI interface. Refer to QTAN0050, *Using the maXTouch Debug Port*, for more information on the debug port.

There is also a Self Test T25 object that runs self-test routines in the mXT768E-AT to find hardware faults on the sense lines and the electrodes. Refer to the *mXT768E-AT 2.1 Protocol Guide* and QTAN0059, *Using the maXTouch Self Test Feature*, for more information.

4.11 Communications

Communication with the host is achieved using the I^2C interface (see). Connect the COMMSEL pin to GND to select the I^2C interface.

4.12 Configuring the Device

The device has an object-based protocol that organizes the features of the device into objects that can be controlled individually. This is configured using the Object Protocol common to many of Atmel's touch sensor devices. For more information on the Object Protocol and its implementation on the device, refer to the *mXT768E-AT 2.1 Protocol Guide*.

5. I²C Communications

5.1 Communications Protocol

The device can use an I²C interface for communication. See Appendix E on page 48 for details of the I²C protocol.

The I²C interface is used in conjunction with the $\overline{\text{CHG}}$ line. The $\overline{\text{CHG}}$ line going active signifies that a new data packet is available. This provides an interrupt-style interface and allows the device to present data packets when internal changes have occurred.

5.2 I²C Addresses

The mXT768E-AT supports two I²C device addresses that are selected using the ADDSEL line at start-up. The two internal I²C device addresses are 0x4C (ADDSEL low) and 0x4D (ADDSEL high). These are shifted left to form the SLA+W or SLA+R address when transmitted over the I²C interface, as shown in Table 5-1.

Table 5-1.　Format of SLA+W and SLA+R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0x4C or 0x4D							Read/write

5.3 Writing To the Device

A WRITE cycle to the device consists of a START condition followed by the I²C-compatible address of the device (SLA+W). The next two bytes are the address of the location into which the writing starts. The first byte is the Least Significant Byte (LSByte) of the address, and the second byte is the Most Significant Byte (MSByte). This address is then stored as the address pointer.

Subsequent bytes in a multibyte transfer form the actual data. These are written to the location of the address pointer, location of the address pointer + 1, location of the address pointer + 2, and so on. The address pointer returns to its starting value when the WRITE cycle's STOP condition is detected.

Figure 5-1 shows an example of writing four bytes of data to contiguous addresses starting at 0x1234.

Figure 5-1.　Example of a Four-byte Write Starting at Address 0x1234

| START | SLA+W | 0x34 | 0x12 | 0x96 | 0x9B | 0xA0 | 0xA5 | STOP |

Write Address (LSB, MSB)　　　Write Data
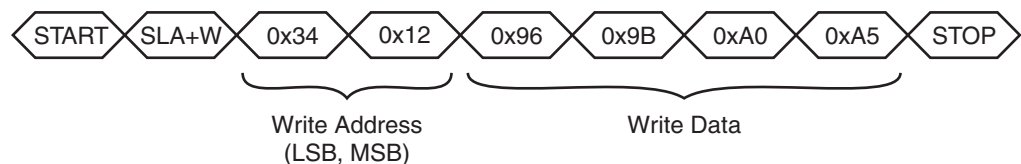
5.4 I²C Writes in Checksum Mode

In I²C checksum mode an 8-bit CRC is added to all I²C writes. The CRC is sent at the end of the data write as the last byte before the STOP condition. All the bytes sent are included in the CRC, including the two address bytes. Any command or data sent to the device is processed even if the CRC fails.

To indicate that a checksum is to be sent in the write, the most significant bit of the MSByte of the address is set to 1. For example, the I²C command shown in Figure 5-2 writes a value of 150 (0x96) to address 0x1234 with a checksum. The address is changed to 0x9234 to indicate checksum mode.

Figure 5-2. Example of a Write To Address 0x1234 With a Checksum
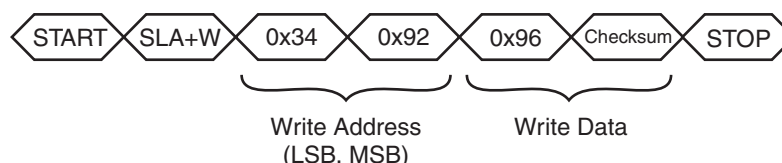
5.5 Reading From the Device

Two I²C bus activities must take place to read from the device. The first activity is an I²C write to set the address pointer (LSByte then MSByte). The second activity is the actual I²C-compatible read to receive the data. The address pointer returns to its starting value when the read cycle's NACK is detected.

It is not necessary to set the address pointer before every read. The address pointer is updated automatically after every read operation. The address pointer will be correct if the reads occur in order. In particular, when reading multiple messages from the Message Processor T5 object, the address pointer is automatically reset to allow continuous reads (see Section 5.6 on page 22).

The WRITE and READ cycles consist of a START condition followed by the I²C address of the device (SLA+W or SLA+R respectively).

Figure 5-3 shows the I²C commands to read four bytes starting at address 0x1234.

Figure 5-3. Example of a Four-byte Read Starting at Address 0x1234
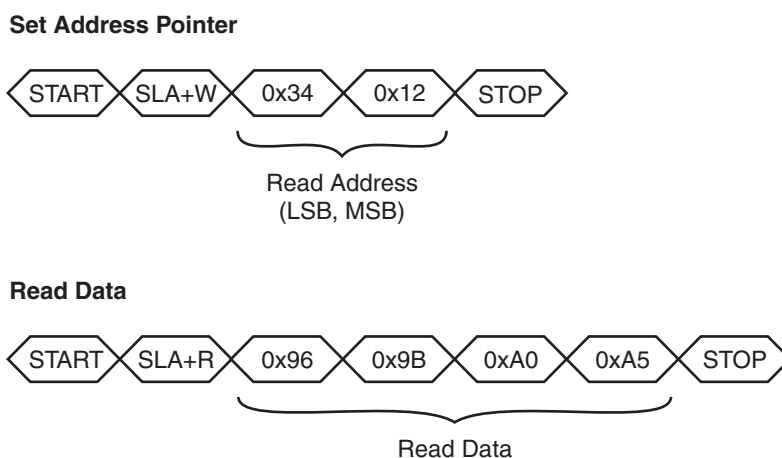
5.6   Reading Status Messages with DMA

The device facilitates the easy reading of multiple messages using a single continuous read operation. This allows the host hardware to use a direct memory access (DMA) controller for the fast reading of messages, as follows:

1. The host uses a write operation to set the address pointer to the start of the Message Count T44 object, if necessary [1] .If a checksum is required on each message, the most significant bit of the MSByte of the read address must be set to 1.

2. The host starts the read operation of the message by sending a START condition.

3. The host reads the Message Count T44 object (one byte) to retrieve a count of the pending messages (refer to the *mXT768E-AT 2.1 Protocol Guide* for details).

4. The host calculates the number of bytes to read by multiplying the message count by the size of the Message Processor T5 object. [2]

    Note that the size of the Message Processor T5 object as recorded in the Object Table includes a checksum byte. If a checksum has not been requested, one byte should be deducted from the size of the object. That is: number of bytes = count x (size-1).

5. The host reads the calculated number of message bytes. It is important that the host does *not* send a STOP condition during the message reads, as this will terminate the continuous read operation and reset the address pointer. No START and STOP conditions must be sent between the messages.

6. The host sends a STOP condition at the end of the read operation after the last message has been read. The NACK condition immediately before the STOP condition resets the address pointer to the start of Message Count T44 object.

Figure 5-4 shows an example of using a continuous read operation to read three messages from the device without a checksum. shows the same example with a checksum.

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1. The STOP condition at the end of the read resets the address pointer to its initial location, so it may already be pointing at the Message Count T44 object following a previous message read.

2. The host should have already read the size of the Message Processor T5 object in its initialization code.

Figure 5-4. Continuous Message Read Example – No Checksum

Set Address Pointer

$$\langle START \rangle\!\!\times\!\!\langle SLA+W \rangle\!\!\times\!\! LSB \times MSB \times\langle STOP \rangle$$

Start Address of
Message Count Object

Continuous
Read

Read Message Count

$$\langle START \rangle\!\!\times\!\!\langle SLA+R \rangle\!\!\times\!\!\langle Count = 3 \rangle$$

Message Count Object

Read Message Data

($size$ – 1) bytes

$\langle Report\ ID \rangle\!\!\times Data \rangle\quad \bullet\ \bullet\ \bullet\quad \langle Data \rangle$

Message Processor Object – Message # 1

$\langle Report\ ID \rangle\!\!\times Data \rangle\quad \bullet\ \bullet\ \bullet\quad \langle Data \rangle$

Message Processor Object – Message # 2

$\langle Report\ ID \rangle\!\!\times Data \rangle\quad \bullet\ \bullet\ \bullet\quad \langle Data \rangle\!\!\times\langle STOP \rangle$

Message Processor Object – Message # 3
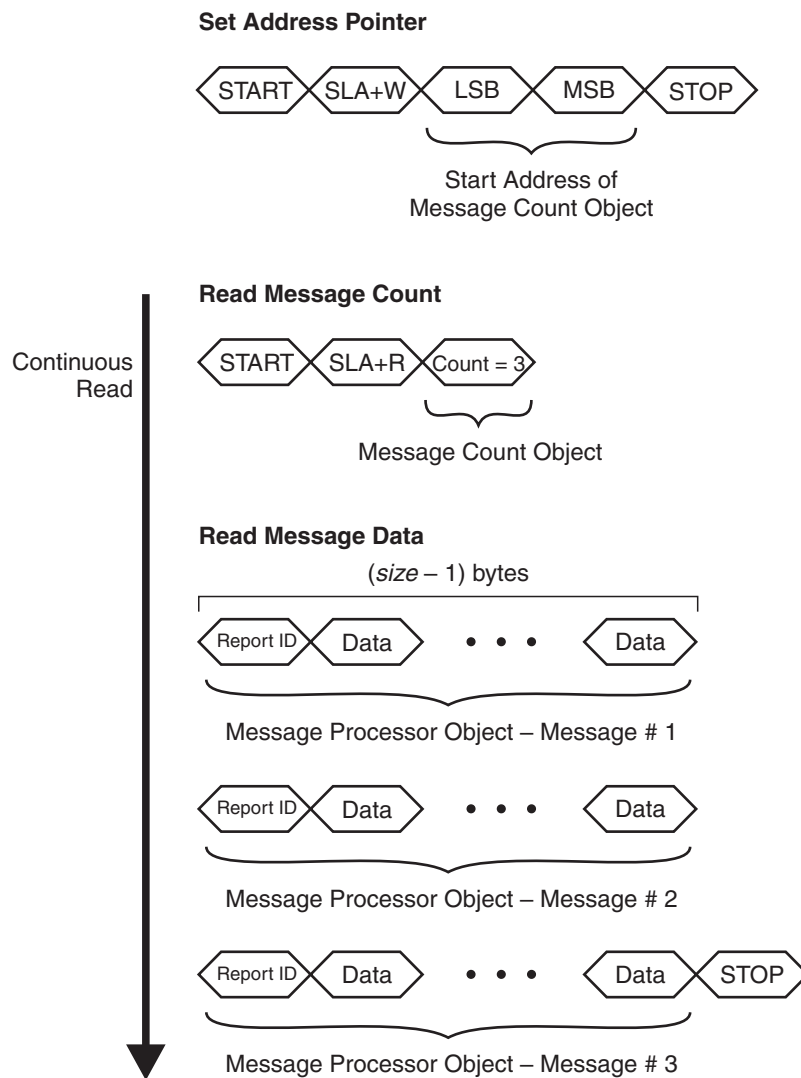
Notes: 1. STOP and START conditions are not necessary between messages.

2. The address pointer is automatically reset to the start of the Message Processor Object between reads.

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Figure 5-5. Continuous Message Read Example – I^{2}C Checksum Mode
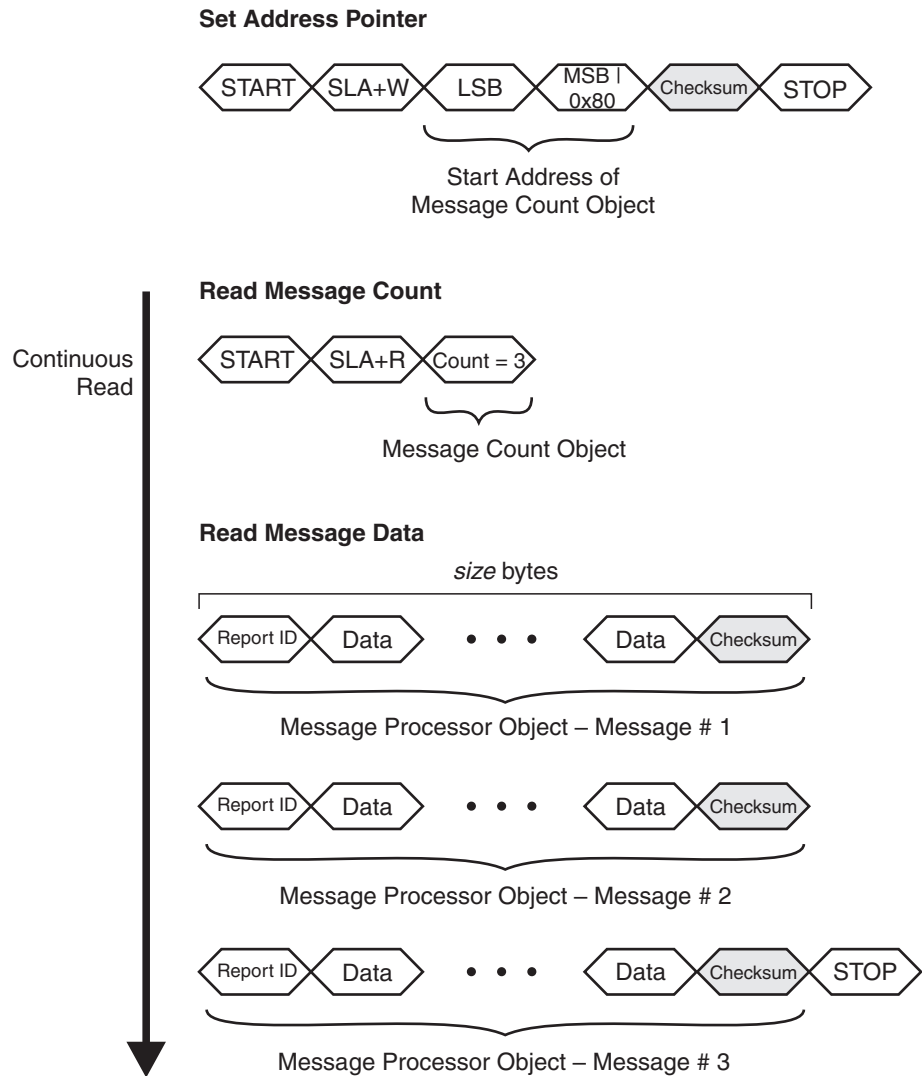
There are no checksums added on any other I^{2}C reads. An 8-bit CRC can be added, however, to all I^{2}C writes, as described in Section 5.4 on page 21.

An alternative method of reading messages using the $\overline{\text{CHG}}$ line is given in Section 5.7.

5.7 $\overline{\text{CHG}}$ Line

The $\overline{\text{CHG}}$ line is an active-low, open-drain output that is used to alert the host that a new message is available in the Message Processor T5 object. This provides the host with an interrupt-style interface with the potential for fast response times. It reduces the need for wasteful I^{2}C-compatible communications.

The $\overline{\text{CHG}}$ line remains low as long as there are messages to be read. The host should be configured so that the $\overline{\text{CHG}}$ line is connected to an interrupt line that is level-triggered. The host should not use an edge-triggered interrupt as this means adding extra software precautions.

The $\overline{\text{CHG}}$ line should be allowed to float during normal usage. This is particularly important after power-up or reset (see).

A pull-up resistor is required, typically 10 kΩ to Vdd.

The $\overline{\text{CHG}}$ line operates in two modes, as defined by the Communications Configuration T18 object (refer to the *mXT768E-AT 2.1 Protocol Guide*).

Figure 5-6. $\overline{\text{CHG}}$ Line Modes for I²C Transfers

Mode 0

I²C Interface — ACK — START | SLA-R | B0 | B1 | ··· | Bn | B0 | B1 | ··· | Bn | ··· | B0 | B1 | ··· | Bn | STOP — NACK
Message #1 — Message #2 — Message #m

$\overline{\text{CHG}}$ Line

$\overline{\text{CHG}}$ line high or low; see text

Mode 1

I²C Interface — START | SLA-R | B0 | B1 | ··· | Bn | B0 | B1 | ··· | Bn | ··· | B0 | B1 | ··· | Bn | STOP — ACK
Message #1 — Message #2 — Message #m

$\overline{\text{CHG}}$ Line

$\overline{\text{CHG}}$ line high or low; see text
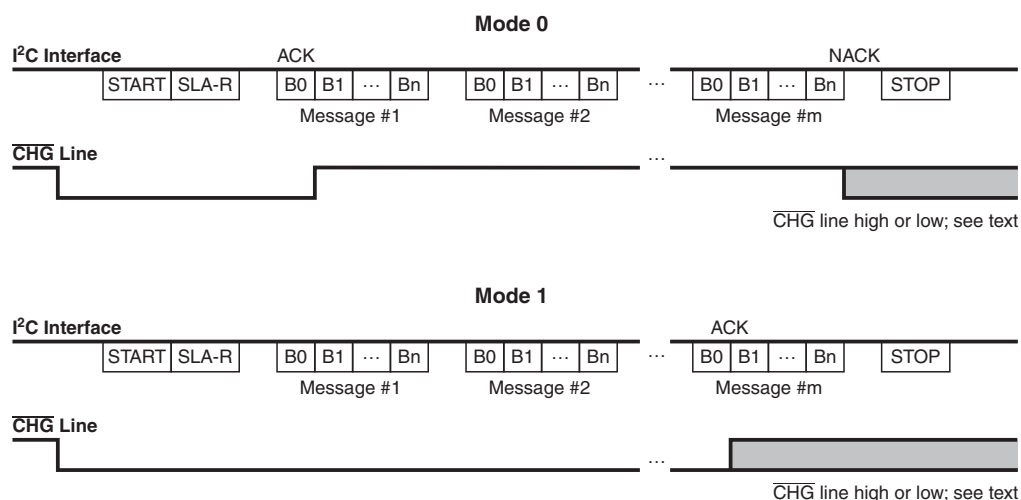
In Mode 0:

1. The $\overline{\text{CHG}}$ line goes low to indicate that a message is present.
2. The $\overline{\text{CHG}}$ line goes high when the first byte of the first message (that is, its report ID) has been sent and acknowledged (ACK sent) and the next byte has been prepared in the buffer.
3. The STOP condition at the end of an I²C transfer causes the $\overline{\text{CHG}}$ line to stay high if there are no more messages. Otherwise the $\overline{\text{CHG}}$ line goes low to indicate a further message.

Mode 0 allows the host to continually read messages. Messaging reading ends when a report ID of 255 ("invalid message") is received. Alternatively the host ends the transfer by sending a NACK after receiving the last byte of a message, followed by a STOP condition. If and when there is another message present, the $\overline{\text{CHG}}$ line goes low, as in step 1. In this mode the state of the $\overline{\text{CHG}}$ line does not need to be checked during the I²C read.

In Mode 1:

1. The $\overline{\text{CHG}}$ line goes low to indicate that a message is present.
2. The $\overline{\text{CHG}}$ line remains low while there are further messages to be sent after the current message.
3. The $\overline{\text{CHG}}$ line goes high again only once the first byte of the last message (that is, its report ID) has been sent and acknowledged (ACK sent) and the next byte has been prepared in the output buffer.

Mode 1 allows the host to continually read the messages until the $\overline{\text{CHG}}$ line goes high, and the state of the $\overline{\text{CHG}}$ line determines whether or not the host should continue receiving messages from the device.

Note: The state of the $\overline{\text{CHG}}$ line should be checked only between messages and not between the bytes of a message. The precise point at which the $\overline{\text{CHG}}$ line changes state cannot be predicted and so the state of the $\overline{\text{CHG}}$ line cannot be guaranteed between bytes.

The Communications Configuration T18 object can be used to configure the behavior of the $\overline{\text{CHG}}$ line. In addition to the $\overline{\text{CHG}}$ line operation modes described above, this object allows the use of edge-based interrupts, as well as direct control over the state of the $\overline{\text{CHG}}$ line. Refer to the *mXT768E-AT 2.1 Protocol Guide* for more information.

5.8 SDA, SCL

The I^{2}C bus transmits data and clock with SDA and SCL, respectively. These are open-drain. The device can only drive these lines low or leave them open. The termination resistors (Rp) pull the line up to Vdd if no I^{2}C device is pulling it down.

The termination resistors commonly range from 1 kΩ to 10 kΩ. They should be chosen so that the rise times on SDA and SCL meet the I^{2}C specifications (see Section 7.7 on page 33).

5.9 Clock Stretching

The device supports clock stretching in accordance with the I^{2}C specification. It may also instigate a clock stretch if a communications event happens during a period when the device is busy internally. The maximum clock stretch is approximately 10 – 15 ms.

The device has an internal bus monitor that can reset the internal I^{2}C hardware if SDA or SCL is stuck low for more than 200 ms. This means that if a prolonged clock stretch of more than 200 ms is seen by the device, then any ongoing transfers with the device may be corrupted. The bus monitor is enabled or disabled using the Communications Configuration T18 object. Refer to the *mXT768E-AT 2.1 Protocol Guide* for more information.

6. Getting Started With the mXT768E-AT

6.1 Establishing Contact

6.1.1 Communication with the Host

The host can use the I^{2}C interface (see Section 5.1 on page 20) to communicate with the device.

6.1.2 I^{2}C Interface

On power-up, the $\overline{\text{CHG}}$ line goes low to indicate that there is new data to be read from the Message Processor T5 object. If the $\overline{\text{CHG}}$ line does not go low, there is a problem with the device.

The host should attempt to read any available messages to establish that the device is present and running following power-up or a reset. Examples of messages include reset or calibration messages. The host should also check that there are no configuration errors reported.

6.2 Using the Object Protocol

The device has an object-based protocol that is used to communicate with the device. Typical communication includes configuring the device, sending commands to the device, and receiving messages from the device. Refer to the *mXT768E-AT 2.1 Protocol Guide* for more information.

The host must perform the following initialization so that it can communicate with the device:

1. Read the start positions of all the objects in the device from the Object Table and build up a list of these addresses.
2. Use the Object Table to calculate the report IDs so that messages from the device can be correctly interpreted.

6.3 Writing to the Device

There are two mechanisms for writing to the device:

- Using an I^{2}C write operation (see Section 4.3 on page 14).

To communicate with the device, you write to the appropriate object:

- To send a command to the device, you write the appropriate command to the Command Processor T6 object (refer to the *mXT768E-AT 2.1 Protocol Guide*).
- To configure the device, you write to an object. For example, to configure the device's power consumption you write to the global Power Configuration T7 object, and to set up a touchscreen you write to a Multiple Touch Touchscreen T9 object. Some objects are optional and need to be enabled before use. Refer to the *mXT768E-AT 2.1 Protocol Guide* for more information on the objects.

6.4 Reading from the Device

Status information is stored in the Message Processor T5 object. This object can be read to receive any status information from the device. There are two mechanisms that provide an interrupt-style interface for reading messages in the Message Processor T5 object:

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- Using the I^{2}C interface, the $\overline{\text{CHG}}$ line is asserted whenever a new message is available in the Message Processor T5 object (see Section 5.7 on page 24). See Section 5.5 on page 21 for information on the format of the I^{2}C read operation.

Note that the host should always wait to be notified of messages. The host should not poll the device for messages.

6.5   Configuring the Device

The objects are designed such that a default value of zero in their fields is a "safe" value that typically disables functionality. The objects must be configured before use and the settings written to the nonvolatile memory using the Command Processor T6 object. Refer to the *mXT768E-AT 2.1 Protocol Guide* for more information.

The following objects must be configured before use:

- Power Configuration
    - Set up the Idle Acquisition Interval, Active Acquisition Interval and Active to Idle Timeout.
- Acquisition Configuration

The following objects should also be configured and enabled, as required:

- Touch objects: Multiple Touch Touchscreen T9, Key Array T15, Proximity Key T52
    - Enable the object.
    - Configure the origin and the number of channels it occupies, if applicable. Configure the other fields in the object, as required. For example, set up the AKS group(s), specify the burst length and threshold.
    - Enable reporting to receive touch messages from the object.
- Signal processing objects: One-touch Gesture Processor T24, Two-touch Gesture Processor T27, Grip Suppression T40, Stylus T47, Noise Suppression T48, Adaptive Threshold T55, SlimSensor T56, Extra Touchscreen Data T57
    - Enable the object.
    - Configure the fields in the object, as required.
    - Enable reporting to receive signal processing messages from the object.
- Support objects: Communications Configuration T18, GPIO/PWM Configuration T19, CTE Configuration T46, Self Test T25, Generic Data, User Data T38,
    - Enable the object, if the object requires it.
    - Configure the fields in the object, as required.
    - Enable reporting, if the object supports messages, to receive messages from the object.

Refer to the *mXT768E-AT 2.1 Protocol Guide* for more information on configuring the objects.

7. Specifications

7.1 Absolute Maximum Specifications

Vdd	3.6 V
AVdd	3.6 V
Max continuous pin current, any control or drive pin	40 mA
Voltage forced onto any pin	–0.3 V to (Vdd or AVdd) + 0.3 V
Configuration parameters maximum writes	10,000

CAUTION: Stresses beyond those listed under *Absolute Maximum Specifications* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum specification conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

Operating temp	–40°C to +85°C
Storage temp	–65°C to +150°C
Vdd	2.7 V to 3.3 V (±5%)
AVdd	2.7 V to 3.3V (±5%)
Vdd vs AVdd power sequencing	No sequencing required
Vdd Supply ripple	See Section 7.9 on page 33
Cx transverse load capacitance per channel	0.63 pF to 5 pF
GPIO maximum output current	2.7 mA

7.3 DC Specifications

7.3.1 Digital Power (Vdd)

Parameter	Description	Min	Typ	Max	Units	Notes
Vdd	Operating limits	2.57		3.47	V	
Rate of rise [1]		0.002		2.5	V/µs	

1. These values are based on simulation and characterization of other maXTouch devices manufactured using the same process technology. These values are not covered by test limits in production

7.3.2 Analog Power (AVdd)

Parameter	Description	Min	Typ	Max	Units	Notes
AVdd	Operating limits	2.57		3.47	V	See Section 4.8.2 on page 17
Rate of rise [1]				2.5	V/µs	

1. These values are based on simulation and characterization of other maXTouch devices manufactured using the same process technology. These values are not covered by test limits in production

7.3.3   Input/Output

Ta (ambient temperature) = recommended range, unless otherwise noted

Parameter	Description	Min	Typ	Max	Units	Notes
Input ($\overline{\text{RESET}}$, SDA, SCL, GPIO)						
Vil	Low input logic level	−0.3		0.3 × Vdd	V	Vdd = 2.57 V to 3.47 V
Vih	High input logic level	0.7 × Vdd		Vdd + 0.3	V	Vdd = 2.57 V to 3.47 V
Iil	Low input leakage current			1	µA	Pull-up resistors disabled
Iih	High input leakage current			1	µA	
Output ($\overline{\text{CHG}}$, GPIO)						
Vol	Low output voltage			0.2 × Vdd	V	I_{OH} = 2.7 mA
Voh	High output voltage	0.8 × Vdd			V	I_{OH} = 2.7 mA
Iol	Low output current			2.7	mA	
Ioh	High output current			2.7	mA	

7.4   Supply Current

IDLEADCSPERX=ACTVADCSPERX=16, SlimSensor T56 Enabled

7.4.1   Analog current

Parameter	Description	Min	Typ	Max	Units	Notes
	Active average supply current		10.9		mA	100 Hz, 1 Touch
AIdd	Idle average supply current		1.58		mA	16 Hz, No Touch
	Sleep average supply current		0.1		mA	

7.4.2   Digital Current

Parameter	Description	Min	Typ	Max	Units	Notes
	Active average supply current		13.53		mA	100 Hz, 1 Touch
Idd	Idle average supply current		1.75		mA	16 Hz, No Touch
	Sleep average supply current		0.1		mA	

7.5   Power Consumption

I²C Interface – 3.3 V Supply Current

XSIZE = 24, YSIZE = 32, CHRGTIME = 75 (2.5 µs), IDLESYNCSPERX/ACTSYNCSPERX = 16,
SlimSensor T56 enabled, Optimal Integration and Noise cancellation enabled

- Aldd No Touch
- Aldd 1 Touch
- DIdd No Touch
- DIdd 1 Touch

I²C Interface – 3.3 V Supply Current

XSIZE = 24, YSIZE = 32, CHRGTIME = 75 (2.5 µs), IDLESYNCSPERX/ACTSYNCSPERX = 16
SlimSensor T56 disabled

- Aldd No Touch
- Aldd 1 Touch
- DIdd No Touch
- DIdd 1 Touch

7.6 Timing Specifications

7.6.1 Touch Latency

Touches = 1, XSIZE = 24, YSIZE = 32, CHRGTIME = 2.5 µs, Room Temperature

Parameter	Description	Min	Typ	Max	Units	Notes
Tlatency	83 Hz	6.4		20.3	ms	IDLEACQINT = ACTVACQINT = 12
	100 Hz	6.4		18.3	ms	IDLEACQINT = ACTVACQINT = 10
	143 Hz	6.4		15.4	ms	IDLEACQINT = ACTVACQINT = 7

7.6.2 Speed

Acquisition Rate vs Number of Moving Touches

XSIZE = 24, YSIZE = 32, CHRGTIME = 75 (2.5 µs), IDLESYNCSPERX/ACTSYNCSPERX = 16, Noise Suppression T48 disabled, SlimSensor T56 = On
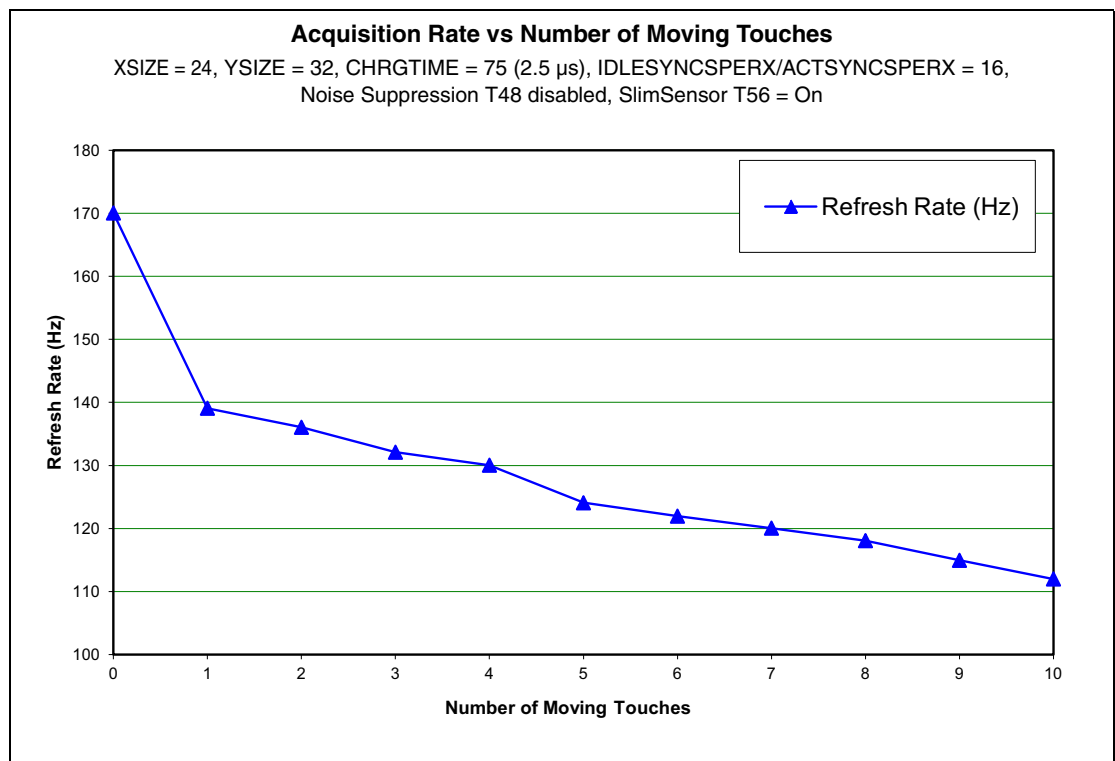
7.6.3 Reset Timings

Parameter	Min	Typ	Max	Units	Notes
Power on to $\overline{CHG}$ line low		47	67	ms	
Hardware reset to $\overline{CHG}$ line low		46.5	66	ms	
Software reset to $\overline{CHG}$ line low		194	276	ms	

7.7 I²C Specifications

Parameter	Operation
Addresses	0×4C or 0×4D
Maximum bus speed (SCL)	400 kHz
I²C specification	Version 2.1

7.8 Touch Accuracy and Repeatability

Touchscreen pitch $\leq$ 5 mm, front panel = 1 mm, touch size = 8 mm

Parameter	Min	Typ	Max	Units	Notes
Linearity		±0.5		mm	
Accuracy		±1		mm	
Accuracy at edge		±2		mm	
Repeatability		±0.25		%	X axis with 12-bit resolution

7.9 Power Supply Ripple and Noise

Parameter	Min	Typ	Max	Units	Notes
Vdd			±50	mV	Across frequency range 1Hz to 1 MHz
AVdd			±10	mV	Across frequency range 1Hz to 1 MHz

The test circuit used for the charts is shown in Figure 7-1.

Figure 7-1. Circuit Used for Power Supply Ripple Characterization Charts
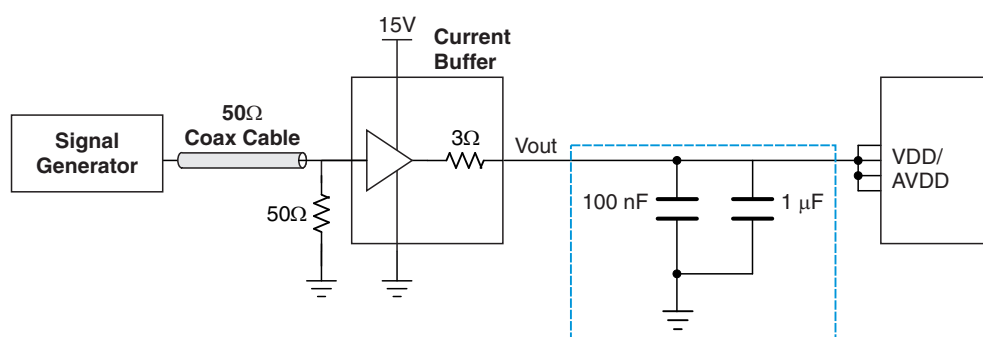
Note: Bypass capacitors are <5 mm away from the chip.

7.10 ESD Information

1.5 kΩ/100 pF/3 pulses		
Parameter	**Value**	**Reference Standard**
Electrostatic Discharge HBM	±2000V	MIL– STD883 Method 3015.7
Electrostatic Discharge CDM	± 250 V	JEDEC-22A TEST METHOD C101-A

7.11 Thermal Packaging

7.11.1 Thermal Data

Parameter	Typ	Unit	Condition	Package
Junction to ambient thermal resistance	49.7	°C/W	Still air	TQFP 100, 14 X 14 mm
Junction to case thermal resistance	14.2	°C/W		TQFP 100, 14 X 14 mm

7.11.2 Junction Temperature

The average chip junction temperature, T_J in °C can be obtained from the following:

1. $T_J = T_A + (P_D \ x \ \theta_{JA})$
2. $T_J = T_A + (P_D \ x \ (\theta_{HEATSINK} + \theta_{JC}))$

where:

- θ_{JA} = package thermal resistance, Junction to ambient (°C/W), provided in Section 7.11.1.
- θ_{JC} = package thermal resistance, Junction to case thermal resistance (°C/W), provided in Section 7.11.1.
- $\theta_{HEATSINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- P_D = device power consumption (W) estimated from data provided in Section 7.9 on page 33.
- T_A is the ambient temperature (°C).

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or no

t. If a cooling device is required, the second equation should be used to calculate the resulting average chip-junction temperature T_J in °C.

7.12   Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/s max
Preheat Temperature 175°C ±25°C	150 – 200°C
Time Maintained Above 217°C	60 – 150s
Time within 5°C of Actual Peak Temperature	30s
Peak Temperature Range	260°C
Ramp down Rate	6°C/s max
Time 25°C to Peak Temperature	8 minutes max

7.13 Mechanical Dimensions
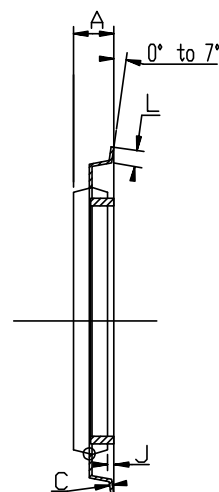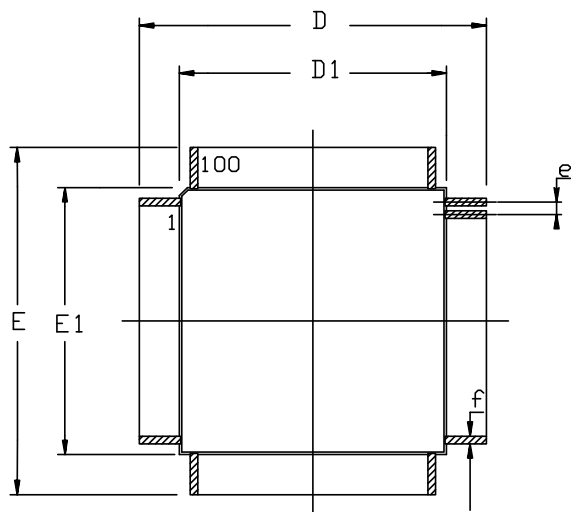
COMMON DIMENSIONS IN MM

SYMBOL	Min	Max	NOTES
A	----	1.20	
A1	0.95	1.05	
C	0.09	0.20	
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
J	0.05	0.15	
L	0.45	0.75	
e	0.50 BSC		
f	0.17	0.27	

04/02/2010
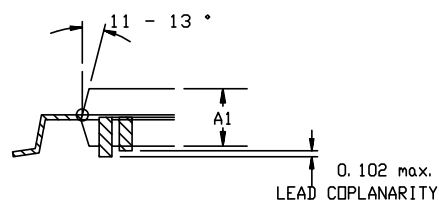
	TITLE	DRAWING No.	REV.
Atmel Nantes S.A. La Chantrerie - BP 70602 44306 Nantes Cedex 3 - France	MT, 100 - Lead, 14x14 mm Body Size, 1.0 mm Body Thickness 0.5 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	MT	E

9712GX–AT42–01/15

7.14 Part Marking

Pin 1 ID

Abbreviation of
Part Number

Date
(year and week)

Lot Code
(variable text)

ATMEL

MXT768E

-T

YYWW V CC

LOTCODE

Country Code

Die Revision
For example V
shown
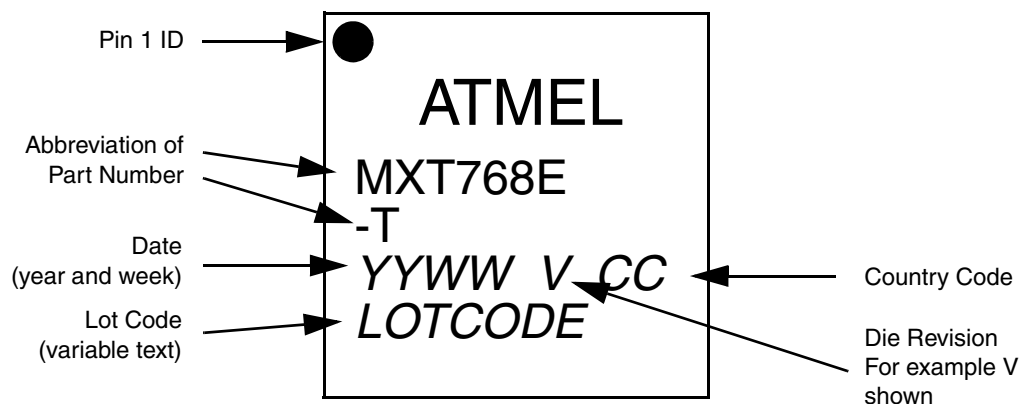
7.15 Part Number

Part Number	Reference Number	Description
ATMXT768E-AT (trays)	GBC	100-pin 14 × 14 × 1 mm TQFP RoHS compliant
ATMXT768E-ATR (tape and reels)	GBC	100-pin 14 × 14 × 1 mm TQFP RoHS compliant

7.16 Moisture Sensitivity Level (MSL)

MSL Rating	Peak Body Temperature	Specifications
MSL3	260ºC	IPC/JEDEC J-STD-020

Appendix A.   PCB Design Considerations

A.1   Introduction

The following sections give the design considerations that should be adhered to when designing a PCB layout for use with the mXT768E-AT. Of these, power supply and ground tracking considerations are the most critical.

By observing the following design rules, and with careful preparation for the PCB layout exercise, designers will be assured of a far better chance of success and a correctly functioning product.

A.2   Printed Circuit Board

Atmel recommends the use of a four layer printed circuit board for mXT768E-AT applications. This, together with careful layout, will ensure that the board meets relevant EMC requirements for both noise radiation and susceptibility, as laid down by the various national and international standards agencies.

Standard component footprint, PCB/FPCB mask opening, pad finish, stencil design, solder reflow parameters are suitable for assembly of the mXT768E-AT. The assembly provider should be contacted for industry best practices when designing applications with the mXT768E-AT

A.3   Supply Rails and Ground Tracking

Power supply and clock distribution are the most critical parts of any board layout. Because of this, it is advisable that these be completed before any other tracking is undertaken. After these, supply decoupling, and analog and high speed digital signals should be addressed. Track widths for all signals, especially power rails should be kept as wide as possible in order to reduce inductance.

The Power and Ground planes themselves can form a useful capacitor. Flood filling for either or both of these supply rails, therefore, should be used where possible. It is important to ensure that there are no floating copper areas remaining on the board: all such areas should be connected to the 0V plane. The flood filling should be done on the outside layers of the board.

A.4   Power Supply Decoupling

As a rule, a suitable decoupling capacitor should be placed on each and every supply pin on all digital devices. It is important that these capacitors are placed as close to the chip's supply pins as possible (less than 5mm away). The ground connection of these capacitors should be tracked to 0V by the shortest, heaviest traces possible.

Capacitors with a Type II dielectric, such as X5R or X7R and with a value of at least 100nF, should be used for this purpose.

In addition, at least one 'bulk' tantalum decoupling capacitor, with a minimum value of 4.7 µF should be placed on each power rail, close to where the supply enters the board.

Surface mounting capacitors are preferred to wire leaded types due to their lower ESR and ESL. It is often possible to fit these decoupling capacitors underneath and on the opposite side of the PCB to the digital ICs. This will provide the shortest tracking, and most effective decoupling possible.

Refer to the application note *Selecting Decoupling Capacitors for Atmel's PLDs* (doc0484.pdf; available on Atmel's website) for further general information on decoupling capacitors.

A.5 Suggested Voltage Regulator Manufacturers

The AVdd supply stability is critical for the mXT768E-AT because this supply interacts directly with the analog front end. Atmel therefore recommends that the supply for the analog section of the board be supplied by a regulator that is separate from the logic supply regulator. This reduces the amount of noise injected into the sensitive, low signal level parts of the design.

A single low value series resistor (around 1Ω) is required from the regulator output to the analog supply input on the mXT768E-AT device. This, together with the regulator output capacitor, and the capacitors at the DC input to the device, forms a simple filter on the supply rail.

A low noise device should be chosen for the regulator. If possible this should have provision for adding a capacitor across the internal reference for further noise reduction. Reference should be made to the manufacturer's datasheet.

The voltage regulators listed in Table 7-1 have been tested and found to work well with the mXT768E-AT. They have compatible footprints and pin-out specifications, and are available in the SOT-23 package.

Table 7-1.   Recommended Voltage Regulators

Manufacturer	Part Number	Pin
Linear Technology	LT1761ES5-BYP	Vdd only
Texas Instruments	TPS79301DBVR-Q1	AVdd and Vdd
Texas Instruments	TPS79328DBVR-Q1 (2.8 V)	AVdd and Vdd
Texas Instruments	TPS79330DBVR-Q1 (3.0 V)	AVdd and Vdd
Texas Instruments	TPS79333DBVR-Q1 (3.3 V)	AVdd and Vdd

Note some manufacturers claim that minimal or no capacitance is required for correct regulator operation. However, in all cases, a minimum of a 1.0 µF ceramic, low ESR capacitor at the input and output of these devices should be used. The manufacturers' datasheets should always be referred to when selecting capacitors for these devices and the typical recommended values, types and dielectrics adhered to.

A.6 Analog I/O

In general, tracking for the analog I/O signals from the mXT768E-AT device should be kept as short as possible. These normally go to a connector which interfaces directly to the touchscreen.

Ensure that adequate ground-planes are used. An analog ground plane should be used in addition to a digital one. Care should be taken to ensure that both ground planes are kept separate and are connected together only at the point of entry for the power to the PCB. This is usually at the input connector.

A.7 Component Placement

It is important to orient all devices so that the tracking for important signals (such as power and clocks) are kept as short as possible. This simple point is often overlooked when initially planning a PCB layout and can save hours of work at a later stage.

A.8 Digital Signals

In general, when tracking digital signals, it is advisable to avoid sharp directional changes, sensitive signal tracks (such as analog I/O) and any clock or crystal tracking.

A good ground return path for all signals should be provided, where possible, to ensure that there are no discontinuities in the ground return path.

A.9 EMC and Other Observations

The following recommendations are not mandatory, but may help in situations where particularly difficult EMC or other problems are present:

- Try to keep as many signals as possible on the inside layers of the board. If suitable ground flood fills are used on the top and bottom layers, these will provide a good level of screening for noisy signals, both into and out of the PCB.
- Ensure that the on-board regulators have sufficient tracking around and underneath the devices to act as a heatsink. This heatsink will normally be connected to the 0V or ground supply pin. Increasing the width of the copper tracking to any of the device pins will aid in removing heat. There should be no solder mask over the copper track underneath the body of the regulators.
- Ensure that the decoupling capacitors, especially tantalum, or high capacity ceramic types, have the requisite low ESR, ESL and good stability/temperature properties. Refer to the regulator manufacturer's datasheet for more information.

A.10 Self-capacitance Layout Considerations

If the two self-capacitance channels are to be used, the chip should be placed to minimize the SNSK trace length to reduce low frequency pickup, and to reduce stray Cx which degrades gain. The Cs and Rs resistors (see the schematics in) should be placed as close to the body of the chip as possible so that the trace between Rs and the SNSK pin is very short. This reduces the antenna-like ability of this trace to pick up high frequency signals and feed them directly into the chip.

Keep the electrode and its SNSK trace away from other signal, power, and ground traces. Any adjacent trace or ground plane will cause an increase in Cx load and desensitize the device. The possible signal-to-noise ratio benefits of a ground plane around or under the electrode are more than negated by the decreased gain from the circuit. Metal areas near the electrode will also reduce the field strength and increase Cx loading and should be avoided, if possible.

For best EMC performance the circuit should be made entirely with SMT components.

In some cases it may be desirable to increase sensitivity of a self-capacitance channel; for example, when it is used as a proximity sensor. Sensitivity can often be increased by using a larger electrode or reducing panel thickness. Increasing electrode size can have diminishing returns, as high values of Cx will reduce sensor gain. Note that increasing the electrode's surface area will not substantially increase touch sensitivity if its diameter is already much larger in surface area than the object being detected.

The value of Cs also has a dramatic effect on sensitivity, and this can be increased in value with the trade-off of slower response time and more power. Panel material can also be changed to one having a higher dielectric constant, which will better help to propagate the field.

Appendix B.   Reference Configuration

The values listed below are used in the reference unit to validate the interfaces and derive the characterization data provided in .

The fields that are not listed have their values set to 0 (which is replaced by a default value). See *mXT768E-AT 2.1 Protocol Guide* for information about the individual objects and their fields.

The values for the user's application will depend on the circumstances of that particular project and will vary from those listed here. Further tuning will be required to achieve an optimal performance..

Field	Value
Power Configuration T7 – GEN_POWERCONFIG_T7 (Instance 0)	
IDLEACQINT	255
ACTVACQINT	255
Acquisition Configuration T8 – GEN_ACQUISITIONCONFIG_T8 (Instance 0)	
CHRGTIME	75
TCHDRIFT	20
DRIFTST	20
ATCHCALSTHR	1
Multiple Touch Touchscreen T9 – TOUCH_MULTITOUCHSCREEN_T9 (Instance 0)	
CTRL	143
XSIZE	24
YSIZE	32
BLEN	128
TCHTHR	50
NUMTOUCH	10
MRGHYST	10
MRGTHR	10
AMPHYST	10
TCHHYST	10
CTE Configuration T46 – SPT_CTECONFIG_T46 (Instance 0)	
IDLESYNCSPERX	8
ACTVSYNCSPERX	8
SlimSensor T56 – PROCI_SHIELDLESS_T56 (Instance 0)	
CTRL	1
OPTINT	1
INTTIME	48
INTDELAY[0]	20
INTDELAY[1]	20

Field	Value
INTDELAY[2]	20
INTDELAY[3]	21
INTDELAY[4]	21
INTDELAY[5]	21
INTDELAY[6]	21
INTDELAY[7]	22
INTDELAY[8]	22
INTDELAY[9]	22
INTDELAY[10]	22
INTDELAY[11]	22
INTDELAY[12]	22
INTDELAY[13]	23
INTDELAY[14]	23
INTDELAY[15]	23
INTDELAY[16]	23
INTDELAY[17]	23
INTDELAY[18]	23
INTDELAY[19]	23
INTDELAY[20]	23
INTDELAY[21]	24
INTDELAY[22]	24
INTDELAY[23]	24
NCNCL	1

Appendix C.   Glossary of Terms

Channel

One of the capacitive measurement points at which the sensor controller can detect capacitive change.

Jitter

The peak-to-peak variance in the reported location for an axis when a fixed touch is applied. Typically jitter is random in nature and has a Gaussian [1] distribution, therefore measurement of peak-to-peak jitter must be conducted over some period of time, typically a few seconds. Jitter is typically measured as a percentage of the axis in question.

For example a 100 x 100 mm touchscreen that shows ±0.5 percent jitter in X and ±1 percent jitter in Y would show a peak deviation from the average reported coordinate of ±0.5 mm in X and ±1 mm in Y. Note that by defining the jitter relative to the average reported coordinate, the effects of linearity are ignored.

Linearity

The measurement of the peak-to-peak deviation of the reported touch coordinate in one axis relative to the absolute position of touch on that axis. This is often referred to as the nonlinearity. Nonlinearities in either X or Y axes manifest themselves as regions where the perceived touch motion along that axis (alone) is not reflected correctly in the reported coordinate giving the sense of moving too fast or too slow. Linearity is measured as a percentage of the axis in question.

For each axis, a plot of the true coordinate versus the reported coordinate should be a perfect straight line at 45°. A non linearity makes this plot deviate from this ideal line. It is possible to correct modest nonlinearities using on-chip linearization tables, but this correction trades linearity for resolution in regions where stronger corrections are needed (because there is a stretching or compressing effect to correct the nonlinearity, so altering the resolution in these regions). Linearity is typically measured using data that has been sufficiently filtered to remove the effects of jitter. For example, a 100 mm slider with a nonlinearity of ±1 percent reports a position that is, at most, 1 mm away in either direction from the true position.

Multitouch

The ability of a touchscreen to report multiple concurrent touches. The touches are reported as separate sets of XY coordinates.

One-touch Gesture

A touch gesture that consists of a single touch. The combination of the duration of the touch and any change in position (that is, movement) of the touch characterizes a specific gesture. For example, a tap gesture is characterized by a short-duration touch followed by a release, and no significant movement.

Resolution

The measure of the smallest movement on a slider or touchscreen in an axis that causes a change in the reported coordinate for that axis. Resolution is normally expressed in bits and tends to refer to resolution across the whole axis in question. For example, a resolution

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1. Sometimes called Bell-shaped or Normal distribution.

of 10 bits can resolve a movement of 0.0977 mm on a slider 100 mm long. Jitter in the reported position degrades usable resolution.

Touchscreen

A two-dimensional arrangement of electrodes whose capacitance changes when touched, allowing the location of touch to be computed in both X and Y axes. The output from the XY computation is a pair of numbers, typically 12-bits each, ranging from 0 to 4095, representing the extents of the touchscreen active region.

Two-touch Gesture

A touch gesture that consists of two simultaneous touches. The change in position of the two touches in relation to each other characterizes a specific gesture. For example, a pinch gesture is characterized by two long-duration touches that have a decreasing distance between them (that is, they are moving closer together).

Appendix D. QMatrix Primer

D.1 Acquisition Technique

QMatrix capacitive acquisition uses a series of pulses to deposit charge into a sampling capacitor, Cs. The pulses are driven on X lines from the controller. The rising edge of the pulse causes current to flow in the mutual capacitance, Cx, formed between the X line and a neighboring receiver electrode or Y line. While one X line is being pulsed, all others are grounded. This leads to excellent isolation of the particular mutual capacitances being measured [1], a feature that makes for good inherent touchscreen performance.

After a fixed number of pulses (known as the burst length) the sampling capacitor's voltage is measured to determine how much charge has accumulated. This charge is directly proportional to Cx and therefore changes if Cx [2] changes. The transmit-receive charge transfer process between the X lines and Y lines causes an electric field to form that loops from X to Y. The field itself emanates from X and terminates on Y. If the X and Y electrodes are fixed directly [3] to a dielectric material like plastic or glass, then this field tends to channel through the dielectric with very little leakage of the field out into free-space (that is, above the panel). Some proportion of the field does escape the surface of the dielectric, however, and so can be influenced during a touch.

When a finger is placed in close proximity (a few millimeters) or directly onto the dielectric's surface, some of this stray field and some of the field that would otherwise have propagated via the dielectric and terminated onto the Y electrode, is diverted into the finger and is conducted back to the controller chip via the human body rather than via the Y line.

This means that less charge is accumulated in Cs, and hence the terminal voltage present on Cs, after all the charge transfer pulses are complete, becomes less. In this way, the controller can measure changes in Cx during touch. This means that the measured capacitance Cx goes down during touch, because the coupled field is partly diverted by the touching object.

The spatial separation between the X and Y electrodes is significant to make the electric field to propagate well in relation to the thickness of the dielectric panel.

D.2 Moisture Resistance

A useful side effect of the QMatrix acquisition method is that placing a floating conductive element between the X and Y lines tends to increase the field coupling and so increases the capacitance Cx. This is the opposite change direction to normal touch, and so can be quite easily ignored or compensated for by the controller. An example of such floating conductive elements is the water droplets caused by condensation.

As a result, QMatrix-based touchscreens tend not to go into false detect when they are covered in small non-coalesced water droplets. Once the droplets start to merge, however, they can become large enough to bridge the field across to nearby ground return paths (for example, other X lines not currently driven, or ground paths in mechanical chassis components). When this happens, the screen's behavior can become erratic.

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1. A common problem with other types of capacitive acquisition technique when used for touchscreens, is that this isolation is not so pronounced. This means that when touching one region of the screen, the capacitive signals also tend to change slightly in nearby channels too, causing small but often significant errors in the reported touch position.
2. To a first approximation.
3. Air gaps in front of QMatrix sensors massively reduce this field propagation and kill sensitivity. Normal optically clear adhesives work well to attach QMatrix touchscreens to their dielectric front panel.

There are some measures used in these controllers to help with this situation, but in general there comes a point where the screen is so contaminated by moisture that false detections become inevitable. It should also be noted that uniform condensation soon becomes non-uniform once a finger has spread it around. Finger grease renders the water highly conductive, making the situation worse overall.

In general, QMatrix has industry-leading moisture tolerance but there comes a point when even the best capacitive touchscreen suffers due to moisture on the dielectric surface.

D.3   Interference Sources

D.3.1   Power Supply

The device can tolerate short-term power supply fluctuations. If the power supply fluctuates slowly with temperature, the device tracks and compensate for these changes automatically with only minor changes in sensitivity. If the supply voltage drifts or shifts quickly, the drift compensation mechanism is not able to keep up, causing sensitivity anomalies or false detections.

The device itself uses the AVdd power supply as an analog reference, so the power should be very clean and come from a separate regulator. A standard inexpensive Low Dropout (LDO) type regulator should be used that is not also used to power other loads, such as LEDs, relays, or other high current devices. Load shifts on the output of the LDO can cause AVdd to fluctuate enough to cause false detection or sensitivity shifts. The digital Vdd supply is far more tolerant to noise.

CAUTION: A regulator IC shared with other logic can result in erratic operation and is not advised.

Noise on AVdd can appear directly in the measurement results. Vdd should be checked to ensure that it stays within specification in terms of noise, across a whole range of product operating conditions.

Ceramic bypass capacitors on AVdd and Vdd, placed very close (<5 mm) to the chip are recommended. A bulk capacitor of at least 1 µF and a higher frequency capacitor of around 10 nF to 100 nF in parallel are recommended; both must be X7R or X5R dielectric capacitors.

D.3.2   Other Noise Sources

Refer to QTAN0079, *Buttons, Sliders and Wheels Sensor Design Guide*, for information (downloadable from the Touch Technology area of the Atmel website).

Appendix E.   I²C Basics (I²C Operation)

7.17   Interface Bus

The device communicates with the host over an I²C bus. The following sections give an overview of the bus; more detailed information is available from www.i2C-bus.org. Devices are connected to the I²C bus as shown in Figure E-1. Both bus lines are connected to Vdd via pull-up resistors. The bus drivers of all I²C devices must be open-drain type. This implements a wired AND function that allows any and all devices to drive the bus, one at a time. A low level on the bus is generated when a device outputs a zero.

Figure E-1.   I²C Interface Bus
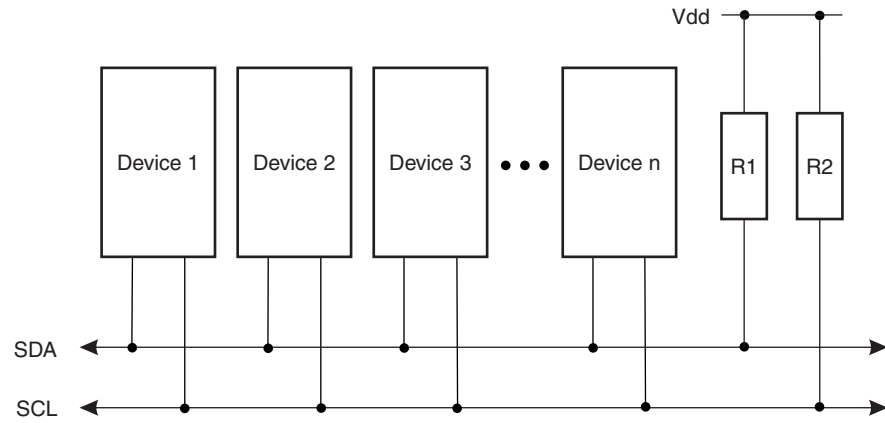
E.1   Transferring Data Bits

Each data bit transferred on the bus is accompanied by a pulse on the clock line. The level of the data line must be stable when the clock line is high; the only exception to this rule is for generating START and STOP conditions.

Figure E-2.   Data Transfer
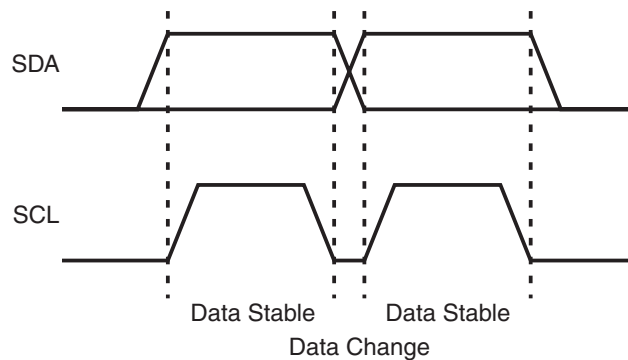
E.2   START and STOP Conditions

The host initiates and terminates a data transmission. The transmission is initiated when the host issues a START condition on the bus, and is terminated when the host issues a STOP condition. Between the START and STOP conditions, the bus is considered busy. As shown in Figure E-3, START and STOP conditions are signaled by changing the level of the SDA line when the SCL line is high.

Figure E-3.   START and STOP Conditions
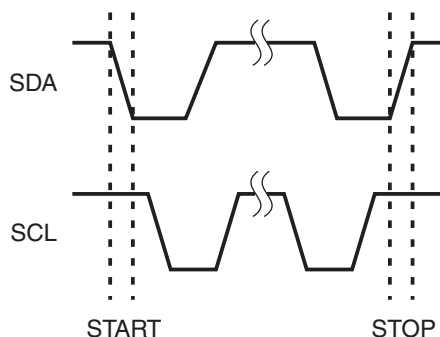
E.3   Address Byte Format

All address bytes are 9 bits long, consisting of 7 address bits, one READ/WRITE control bit and an acknowledge bit. If the READ/WRITE bit is set, a read operation is performed, otherwise a write operation is performed. When the device recognizes that it is being addressed, it will acknowledge by pulling SDA low in the ninth SCL (ACK) cycle. An address byte consisting of a slave address and a READ or a WRITE bit is called SLA+R or SLA+W, respectively.

The most significant bit of the address byte is transmitted first. The address sent by the host must be consistent with that selected with the option jumpers.

Figure E-4.   Address Byte Format
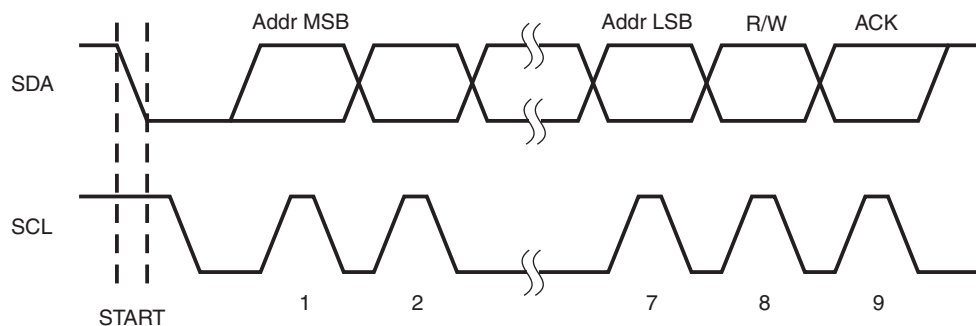
E.4   Data Byte Format

All data bytes are 9 bits long, consisting of 8 data bits and an acknowledge bit. During a data transfer, the host generates the clock and the START and STOP conditions, while the receiver is responsible for acknowledging the reception. An acknowledge (ACK) is signaled by the receiver pulling the SDA line low during the ninth SCL cycle. If the receiver leaves the SDA line high, a NACK is signaled.

Figure E-5. Data Byte Format
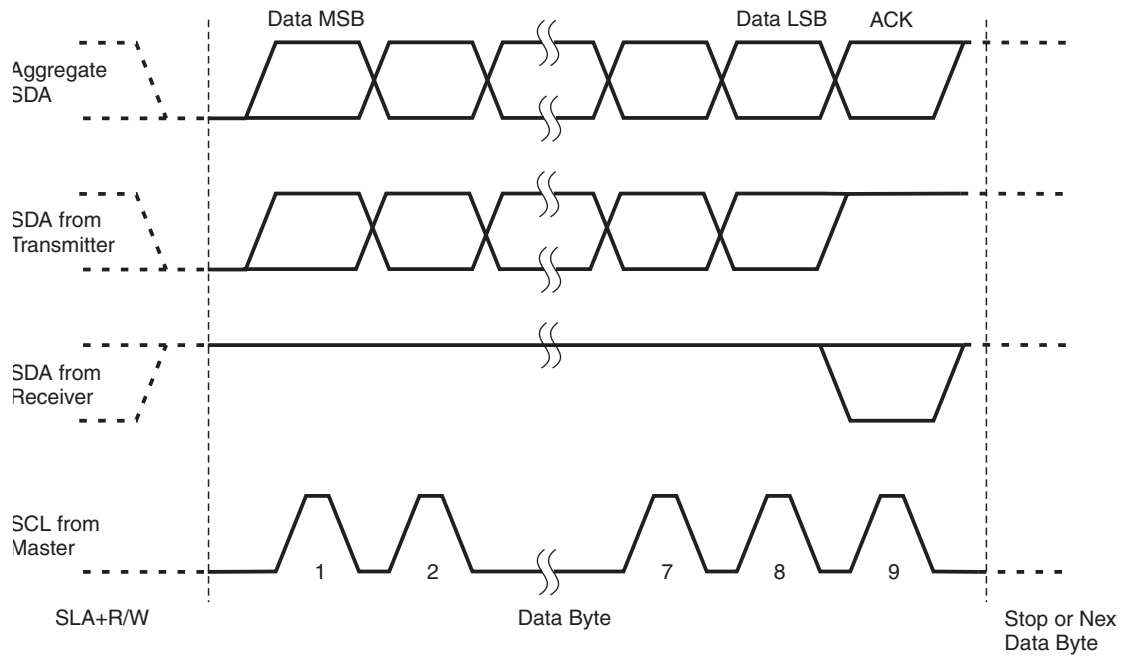
E.5 Combining Address and Data Bytes into a Transmission

A transmission consists of a START condition, an SLA+R/W, one or more data bytes and a STOP condition. The wired "ANDing" of the SCL line is used to implement handshaking between the host and the device. The device extends the SCL low period by pulling the SCL line low whenever it needs extra time for processing between the data transmissions.

Note: Each write or read cycle must end with a stop condition. The device may not respond correctly if a cycle is terminated by a new start condition.

Figure E-6 shows a typical data transmission. Note that several data bytes can be transmitted between the SLA+R/W and the STOP.

Figure E-6. Byte Transmission

Table of Contents

Revision History

Revision Number	History
Revision AX – May 2012	Initial release for firmware revision 2.1– Preliminary
Revision BX – June 2012	Updated Specifications for firmware revision 2.1
Revision CX – July 2012	Updated with Characterization data for firmware revision 2.1
Revision DX – October 2012	Minor updates to aid clarity – Release Updated Characterization data
Revision EX – February 2013	Minor corrections to the analog and digital voltage ranges
Revision FX – February 2014	Corrections to order numbers
Revision GX – January 2015	Minor correction to park marking

Notes

Atmel