Murata Power Solutions

D1U54-D-2500-12-HxxC Series

54mm 1U Front End DC-DC Power Supply Converter

FEATURES

- 2500W continuous 12Vdc main output power
- Cold Redundant power management features
- Highly Efficient, >95% at 50% load
- PMBus™ 1.2 Compliant I²C interface; LED status indicator
- 12V main output
- 3.3V, 5.0V & 12V Standby Output Options
- 1U height: 2.15" x 12.65" x 1.57"
- > 58 Watts per cubic inch density
- N+1 redundant, Hot Swap Capable
- Active (digital) current sharing on 12V main output; Integral ORing /isolation provided for both outputs; compatible with DC input series
- Internal cooling fan (variable speed)
- Overvoltage, overcurrent, overtemperature Protection

RoHS COMPLIANT 25

For full details go to
www.murata-ps.com/rohs

PMBus

PRODUCT OVERVIEW

D1U54-D-2500-12-HxxC is a series of highly efficient Low Voltage DC (LVDC) input front end power supplies featuring a 12Vdc main output, capable of active current sharing and a standby output. A multifunctional status LED, hardware logic signals and PMBus™ digital communications cold redundant capability are standard features. The low profile 1U, >58W/cubic inch package make this series ideal for delivering reliable, efficient power to servers, workstations, storage systems and other 12V distributed power architectures.

ORDERING GUIDE

Model Number	Output power -48 to -60Vdc Nominal	Main Output	Standby Output	Airflow
D1U54-D-2500-12-HA3C	2515W	12.0Vdc	5.0Vdc	F⇨B
D1U54-D-2500-12-HA4C				B⇨F
D1U54-D-2500-12-HB3C	2536W		12.0Vdc	F⇨B
D1U54-D-2500-12-HB4C				B⇨F
D1U54-D-2500-12-HC3C	2515W		3.3Vdc	F⇨B
D1U54-D-2500-12-HC4C				B⇨F

INPUT CHARACTERISTICS

Parameter	Conditions		Min.	Nom.	Max.	Units
Input Source Voltage DC Operating Range	High Line		-40.8	-48/-60	-72	Vdc
Turn-on Input Voltage	Ramp up		-39	-40	-40.5	Vdc
Turn-off Input Voltage	Ramp down		-35.5	-36	-36.5	
Maximum current	-48V - -60V dc				63	Adc
DC Input Inrush Peak Current	Cold start; between 0 to 200ms	-40Vdc			60	Apk
		-72Vdc			120	
Efficiency	-48Vdc input; fan power excluded	20% load		94.0		%
		50% load		95.0		
		100% load		92.0		
Reverse Polarity Protection	Reversed input cables; no internal or external fuse/breaker interruption		+40		+72	Vdc

OUTPUT VOLTAGE CHARACTERISTICS

Output Voltage	Parameter	Conditions	Min.	Typ.	Max.	Units
12V	Output Setpoint Accuracy	50% load; Tamb =25°C; Measured at PSU side of connector	11.94	12.00	12.06	Vdc
	Line and Load Regulation[2]		11.88	12.00	12.18	
	Ripple Voltage & Noise[1,2]	20MHz Bandwidth; Min Load Capacitance			120	mV p-p
	Output Current	2500W (-40 to-72Vdc) Continuous			208.3	Adc
	Load Capacitance				30,000	µF
12VSB	Output Setpoint	50% load; Tamb =25°C	11.94	12.00	12.06	Vdc
	Line and Load Regulation[3]	Measured at PSU side of connector	11.70	12.00	12.30	
	Ripple Voltage & Noise[1,3]	20MHz Bandwidth; Min Load Capacitance			120	mV p-p
	Output Current		0		3.0	Adc
	Load Capacitance				1000	µF
3.3VSB	Output Setpoint	50% load; Tamb =25°C		3.30		Vdc
	Line and Load Regulation[3]	Measured at PSU side of connector	3.14		3.46	
	Ripple Voltage & Noise[1,3]	20MHz Bandwidth; Min Load Capacitance			75	mV p-p
	Output Current		0		3.0	Adc
	Load Capacitance				3000	µF
5.0VSB	Output Setpoint	50% load; Tamb =25°C		5.00		Vdc
	Line and Load Regulation[3]	Measured at PSU side of connector	4.76		5.24	
	Ripple Voltage & Noise[1,3]	20MHz Bandwidth; Min Load Capacitance			75	mV p-p
	Output Current		0		3.0	Adc
	Load Capacitance				3000	µF

[1] Ripple and noise are measured with 0.1 µF of ceramic capacitance and 10 µF of tantalum capacitance on each of the power supply outputs. A short coaxial cable to the scope termination is used and minimum output bus capacitance specified in above table.
[2] Minimum load of 6A
[3] Minimum load of 0.1A

OUTPUT CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Startup Time	DC ramp up; delay until Main output start			3	s
Transient Load Response	12V Main: 10% to 60% load step (50% max load change); 1A/µs slew rate; 2,000µF load capacitance	-5		+5	%
	Recovery Time to Within 1% (voltage prior to transient load step)		2		ms
	12VSB: 10% to 60% load step (50% max load change); 1A/µs slew rate; 500µF load capacitance	-5		+5	%
	Recovery Time to Within 1% (voltage prior to transient load step)		2		ms
Current sharing accuracy	At 200A, two power modules sharing		±5		%
Hot Swap Transients	All outputs remain in regulation	-5		+5	
Holdup Time	-48Vdc Input;12V Main, 100% load	1			ms
	-48Vdc Input;12VSB, 100% load	3			ms

ENVIRONMENTAL CHARACTERISTICS

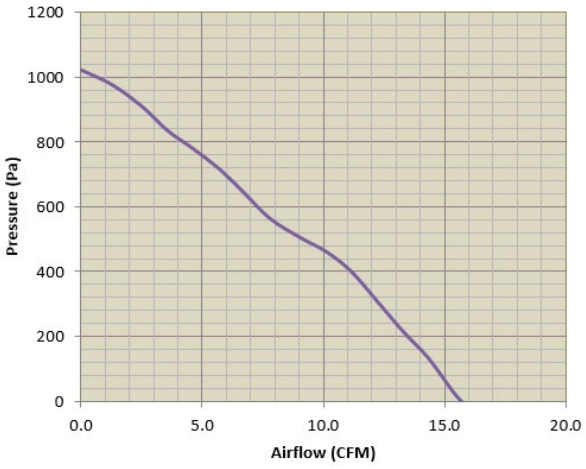
Parameter	Conditions	Min.	Typ.	Max.	Units
Storage Temperature Range		-40		70	°C
Operating Temperature Range (Sea Level)	100% max. load; no output power derating	-5		+50	
NEBS; GR-63-CORE	Abnormal[1] operating +55°C; adjusted for NEBS operating altitude (1800m)	-5		61	
Humidity	Operating; non-condensing	5		95	%
	Non-operating; non-condensing			95	
Altitude Operating[2]				3000	m
Shock	Non-operating; IEC600 68-2-27, test Ea. 30G, 11msec half-sine, 3 shocks per face, 6 faces.			30	G
Operational Vibration	Sine sweep; 5-150Hz			2	
	Random vibration, 5-500Hz			1.11	
MTBF	Per Telcordia SR-332 Issue 3, M1C3 @ 40°C			729K	Hrs.
Safety Approval Standards	IEC 62368-1:2014 CAN/CSA-C22.2 No. 62368-1-14, UL 62368-1, 2nd edition GB4943.1-2011(CQC)14+A11				
Input Fuse	Single 80A/75VDC fast acting fuse; located the input "-48VIN" connection.				
Weight	2.6lbs/1.175kg				

[1]Abnormal operation limited to 96hrs continuous and for not more than 15 days in any one year

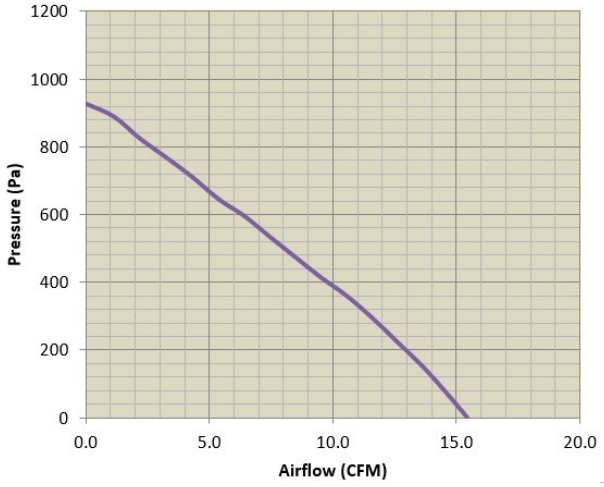
[2]Derating may apply due the effects of system backpressure; prefer derating curves for details

AIRFLOW PERFORMANCE CHARACTERISTICS

P-Q Curve Front to Back models; Fan speed: 100% Duty Cycle



P-Q Curve Back to Front Models; Fan speed: 100% Duty Cycle



PROTECTION CHARACTERISTICS

Output Voltage	Parameter	Conditions	Min.	Typ.	Max.	Units
	Over temperature (intake) [2,3]	Shutdown and auto-recovery, main output both B⇨F & F⇨B Airflows	71	75	79	°C
Main 12V	Overvoltage	Main 12V Output; latching[1] (12VSB maintains operation)	13.0		15	Vdc
	Overcurrent	Five (5) "hiccup" auto recovery cycles, followed by a latched shutdown[1]	220		260	Adc
12VSB	Overvoltage	Latching[1] (both outputs shutdown).	13.0		14.5	Vdc
	Overcurrent	Sustained "hiccup" auto recovery cycles until overcurrent is removed	2.1		3.5	A
5VSB	Overvoltage	Latching[1] (both outputs shutdown).	5.4		6.0	Vdc
	Overcurrent	Sustained "hiccup" auto recovery cycles until overcurrent is removed	3.1		5.0	A
3.3VSB	Overvoltage	Latching[1] (both outputs shutdown).	3.6		4.0	Vdc
	Overcurrent	Sustained "hiccup" auto recovery cycles until overcurrent is removed	3.1		5.0	A

[1] Latch-off requires recycling either the AC input or PS_ON to resume operation

[2] Warning indication (PMbus status register bits and Amber LED status) occurs at 70ºC nominal and recovers at 65ºC nominal; fault indication and shutdown engage at 75 ºC nominal and recovers at 70ºC nominal.

[3] Operating the power supply above the maximum operating temperature (see "ENVIRONMENTAL CHARACTERISTICS") is considered an abnormal condition, may negatively impact power supply life, and is not recommended.

ISOLATION CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Insulation Safety Rating / Test Voltage	Input to Output - Basic	1500			Vdc
	Input to Chassis - Basic	1500			Vdc
Isolation (function only)	Output to Chassis	500			Vdc

EMISSIONS AND IMMUNITY

Characteristic	Standard	Compliance
Conducted Emissions	FCC 47 CFR Part15/CISPR22/EN55032	Class A with 6dB margin[3]
ESD Immunity	IEC/EN 61000-4-2	±8KV Contact; ±15KV air discharge; Criteria A
Radiated Field Immunity	IEC/EN 61000-4-3	10V/m, 1KHz, 80% AM, 80MHz to 1GHz Criteria A
Electrical Fast Transients/Burst Immunity	IEC/EN 61000-4-4	Level 2 (1kV) criteria A[1]
Surge Immunity	IEC/EN 61000-4-5	Level 2 500V DM 1kV CM, criteria A[1]
RF Conducted Immunity	IEC/EN 61000-4-6	Level 2, 3Vrms, 1KHz, 80% AM, 150kHz to 80MHz criteria A
Voltage Dips, Interruptions	NEBS GR-1089-CORE.i07 ATIS-600315.208	Meets the applicable transients of GR-1089-CORE.I07 for DC Input source. Meets applicable transients of ATIS-600315.2018

[1] Measured at power module DC input connector

[2] Installed in end user system and contingent upon final system design

[3] Radiated performance is designed to meet Class A limits; however contingent on deployment; final qualification and certification testing to be performed by End User in system installation

STATUS INDICATORS AND CONTROL SIGNALS (BICOLOUR LED)

Condition	LED Status (Power)
Standby - ON; Main output - OFF; DC PRESENT	Blinking green, 1Hz
Standby - ON; Main output – ON, No faults present	Solid green
Fault Detected: Main output, VSB output, Fan, overtemperature, input overvoltage and coincides with setting of PMBus STATUS_X Register bits	Solid Amber
DC Input absent and/or no I2C slave address detected (See ADDR signal for configuration details); VSB OVP	OFF
Power Supply Warning Event	Blinking Amber
Cold Redundant mode – "COLD_STANDBY" /"FORCED STANDBY" MODE	Blinking green 2Hz

STATUS AND CONTROL SIGNALS

Signal Name	I/O	Description	Interface Details
DC_OK (Default)/ RAPID_ON	Output	Multi-function signal and is configured as one of the following: **DC_OK** (Default setting at initial power up): Output is driven high when input source is available and within acceptable limits. The output is driven low to indicate loss of input power. **RAPID_ON** is a two state analog signal forms the cold redundant bus with up to four (4) load connected PSUs. This signal is used exclusively by the PSU for cold redundant mode operation, and is configured via PMBus™; see ACAN-117 and wiring diagram for details Rapid_ON signal/bus provides these three functions: Pull-up bus voltage: Bus pull-up is provided by the single PSU or the first PSU assigned the roll of "ACTIVE & MASTER" aka "COLD_REDUNDANT ACTIVE". More than one PSU can be assigned as "ACTIVE" only the first PSU assigned this roll provides the pull-up path and is why this PSU is referred to as the "Master". Each bus connected PSU drives the Rapid_ON bus low when any fault is detected. Each bus connected PSU powers on its main output rapidly within 100µS after detection of LOW state. **Note:** "Rapid_ON" pin configuration is retained once setup via PMBus™, even if Input power is recycled and remains the new default setting until commanded to INPUT_OK via PMBus™.	**DC_OK** Pulled up via 511R to internal 5V bias supply and pulled down to DC Return via 10K OHM resistor. **RAPID_ON:** Pulled 511R to 5V internal bias supply of the ACTIVE & MASTER PSU; Pull-Down = 10K. Bus voltage reduces with the QTY of bus connected power supplies
PW_OK (Output OK)	Output	The signal is asserted, driven high, by the power supply to indicate that the main output is valid. If the main output fails, the PW_OK signal will de-assert and is driven low. The PW_OK output is driven low to indicate that the Main output is outside of lower limit of regulation	Pulled up internally via 10K to VDD. A logic high >2.0Vdc A logic low <0.8Vdc Driven low by internal CMOS buffer (open drain output).
SMB_ALERT (FAULT/WARNING)	Output	The signal output is driven low to indicate that the power supply has detected a warning/fault, and any status register bits flagged (except Status_CML). It is intended to alert the system accordingly. This output shall be driven high when the power is operating correctly (within specified limits). The signal will revert to a high level when the warning/fault stimulus (that originally caused the alert) is removed. The LED indicator(s) mirrors this alert pin.	Pulled up internally via 10K to VDD. A logic high >2.0Vdc A logic low <0.8Vdc Driven low by internal CMOS buffer (open drain output).
PRESENT_L (Power Supply Absent)	Output	The signal is used to detect the presence (installed) of a PSU by the host system. The signal is connected to PSU logic SGND within the power module.	Passive connection to +VSB_Return. A logic low <0.8Vdc
PS_ON	Input	This signal is pulled up internally to the internal housekeeping supply (within the power supply). The power supply main 12VDC output will be enabled when this signal is pulled low to +VSB_Return. In the low state the signal input shall not source more than 1mA of current. The 12VDC output will be disabled when the input is driven higher than 2.4V, or open circuited. Cycling this signal shall clear latched fault conditions. (Power Supply Enable/Disable "Mate Last, Break First" (MLBF) Signal	Pulled up internally via 10K to VDD. A logic high >2.0Vdc A logic low <0.8Vdc Input is via CMOS Schmitt trigger buffer.
ADDR	Input	An external pull-down resistor ≤180K must be placed on the system/host side between the ADDR pin and +12V Main/VSB_Return to enable/turn-on the main output. This same resistor also sets the slave addresses as defined in the following table:	DC voltage between the limits of 0 and +3.3Vdc. System side pull-down resistor required, ≤180K
SCL (Serial Clock) SDA (Serial Data)	Both	A serial communications line compatible with PMBus™ Power Systems Management Protocol Part 1 – General Requirements Rev 1.2. No additional internal capacitance is added that would affect the speed of the bus. The signal is provided with a series isolator device to disconnect the internal power supply bus in the event that the power module is unpowered.	Pulled up via 5.11K to internal 3.3VDC VIL is 0.8V maximum VOL is 0.4V maximum VIH is 2.1V minimum
V1_SENSE & V1SENSE_RTN	Input	Remote sense connections intended to be connected at and sense the voltage at the point of load. The voltage sense will interact with the internal module regulation loop to compensate for voltage drops due to connection resistance between the output connector and the load. If remote sense compensation is not required, the voltage can be configured for local sense by: 1. V1_SENSE directly connected to power blades 4 to 6 (inclusive) 2. V1_SENSE_RTN directly connected to power blades 1 to 3 (inclusive)	Compensation for up to 0.12Vdc total connection drop (output and return connections).
ISHARE	Both	The current sharing signal is connected between sharing units (forming an ISHARE bus). It is an input and/or an output (bi-directional analog bus) as the voltage on the line controls the current share between sharing units. A power supply will respond to a change in this bus voltage, but a power supply can also change the voltage depending on the load drawn from it. On a single unit the voltage on the pin (and the common ISHARE bus would read 8VDC at 100% load (module capability). For two identical units sharing the same 100% load this would read 4VDC for perfect current sharing (i.e. 50% module load capability per unit).	Analogue voltage: +8V maximum, 13.1K to Main 12V_RTN

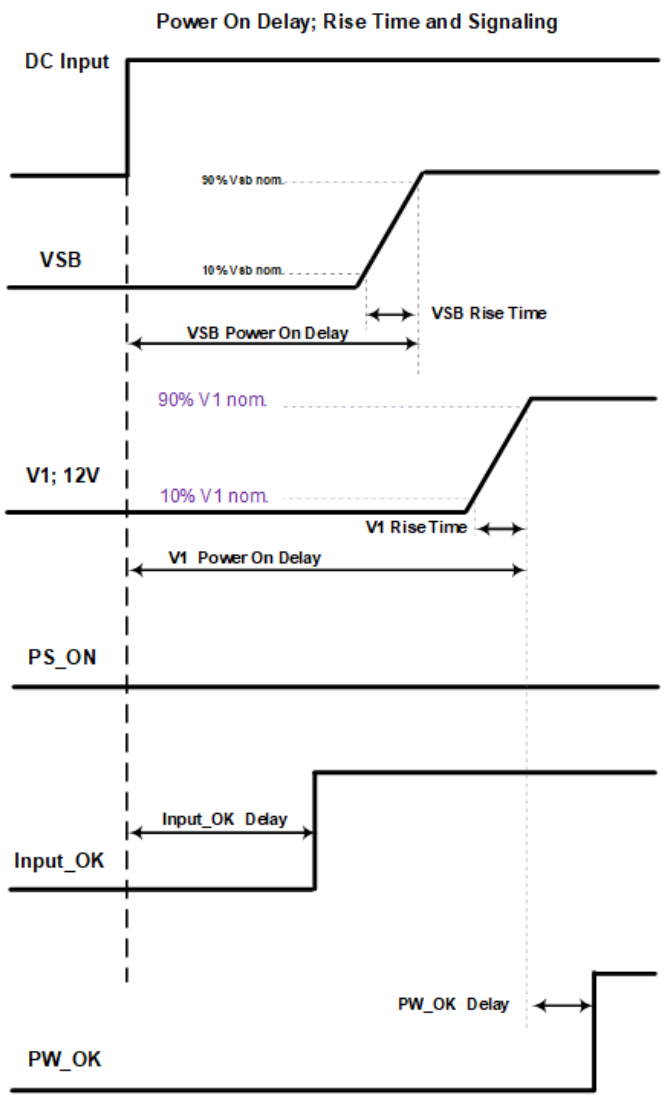
External Resistor Value (K-ohm, ≤+/5%) Pin D2	INTERNAL CONTROLLER	EXTERNAL EEPROM
0.82	0xB0	0xA0
2.7	0xB2	0xA2
5.6	0xB4	0xA4
8.2	0xB6	0xA6
15	0xB8	0xA8
27	0xBA	0xAA
56	0xBC	0xAC
180	0xBE	0xAE

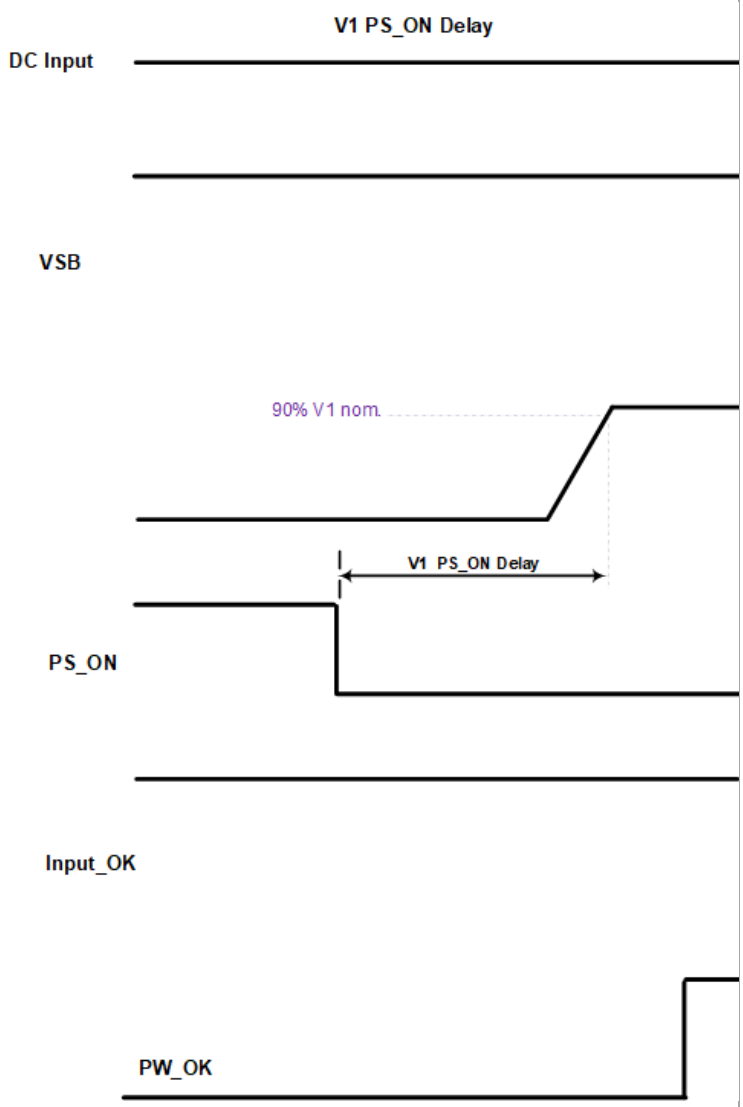
TIMING SPECIFICATIONS

Unless otherwise specified, the following notes apply to all timing specifications:

1. Ta= 25°C, Vin & Vin nom. = -48V
2. Resistive load, 100% full load, both outputs
3. Signal names used interchangeably: V1= 12V main output; V2=VSB output; PS_ON = Enable; PGood=PW_OK; Input_OK = ACOK

Turn-On Delay & Output Rise Time:





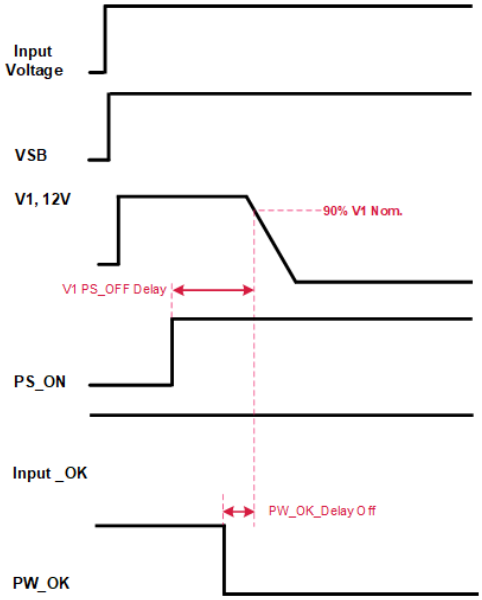
Time	Description	Min.	Max.
V1 Rise time	V1 rising from 10% to 90% V1 nom.; See Figure 1	1ms	20ms
Vsb Rise time	Vsb rising from 10% to 90% Vsb nom.; See Figure 2	1ms	20ms
Vsb Power-on-delay	From application of Vin nom. to Vsb reaching 90% Vsb, nom.; See Figure 3	-	2700ms
V1 Power-on-delay	From application of Vin to V1 reaching 90% of Vout nom. See Figure 4	-	3000ms
V1 PS_ON delay	From PS_ON signal edge to V1 reaching 90% of Vout nom.; See Figure 5	-	500ms
V1 PW_OK delay	From V1 reaching 90% to asserted PW_OK signal; See Figure 6	-	150ms
Input_OK delay	From application of Vin to assertion of Input_OK Signal edge; See Figure 7	-	1200ms

TIMING SPECIFICATIONS

Unless otherwise specified, the following notes apply to all timing specifications and performance oscillograms:

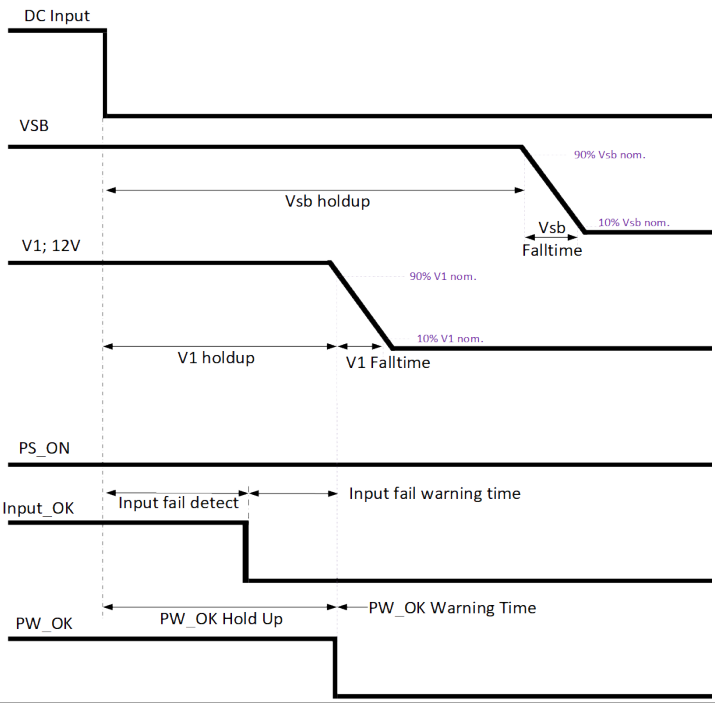
1. Ta= 25°C, Vin & Vin nom. = -48V
2. Resistive load, 100% full load, both outputs
3. Signal names used interchangeably: V1= 12V main output; V2=VSB output; PS_ON = Enable; PGood=PW_OK; Input_OK = ACOK

Turn-Off (Shutdown by PS_ON)



Turn-Off Timing	Description	Min.	Max.
V1 PS_OFF delay	From the rising edge of PS_ON signal to V1 falling below 90% V1 nom. See Figure 8	-	7ms
PW_OK_Delay_Off	Warning time, loss of V1 output (falls to 90% Vout nom.) due to PS_ON signal being negated (upon change from low to high state), See Figure 9	200µs	-

Power Removal Holdup



Power Removal Timing	Description	Min	Max
Vsb holdup	From loss of Vin to Vsb falling to 90% Vsb nom, 2A load.; See Figure 10	3ms	-
V1 holdup	From loss of Vin to V1 falling to 90% Vout nom.; See Figure 11	1ms	-
Input fail detect	From loss of Vin to falling edge of Input_OK signal; See Figure 12	-	1ms
Input fail warning time	Input_OK signal warning time: loss of output due to loss of input, measured from falling edge of Input_fail detect to V1 falling to 90% Vout nom.; see Figure 15	0.5ms	-
PW_OK Hold Up	From loss of input power; see Figure 13	0.75ms	
PW_OK Warning Time	Note: this signal does not guarantee V1 loss warning time (due to loss of input power, Figure 14).	-500 µs	1ms

TYPICAL PERFORMANCE OSCILLOGRAMS

ON/OFF Signal Timing

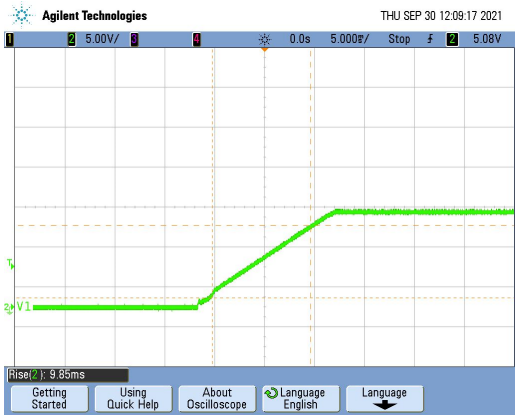


Figure 1: V1 Risetime

Figure 2: V2 Risetime

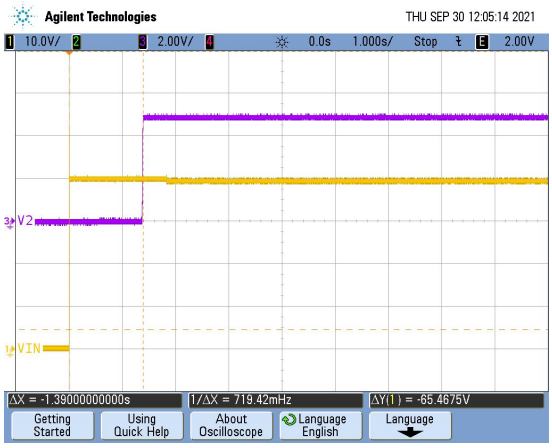


Figure 3: Vsb Power-On Delay

Figure 4: V1 Power-on delay (Vin=40Vdc)

Figure 5: V1 PS_ON Delay

Figure 6: V1 PW_OK Delay

TYPICAL PERFORMANCE OSCILLOGRAMS

ON/OFF Signal Timing

Figure 7: Input_OK Delay

Figure 8: V1 Off Delay by PS_ON

Figure 9: PW_OK_Delay_Off By PS_ON

Figure 10: Vsb_holdup

Figure 11: V1 Holdup

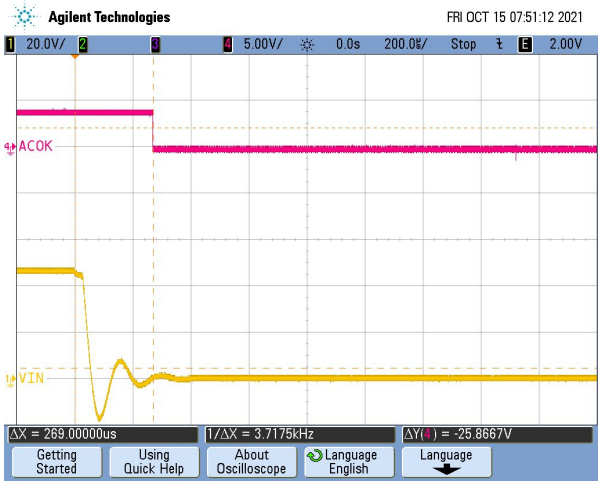


Figure 12: Input Fail Detect

TYPICAL PERFORMANCE OSCILLOGRAMS

ON/OFF Signal Timing

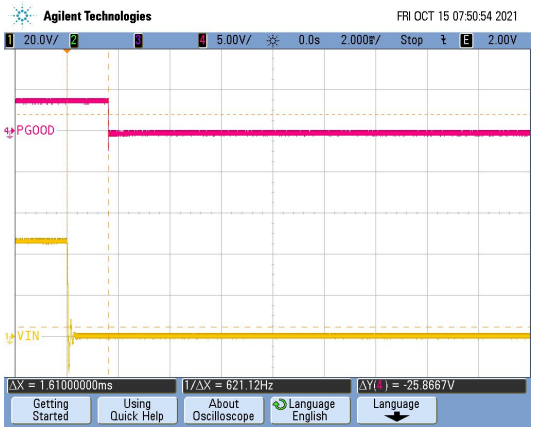
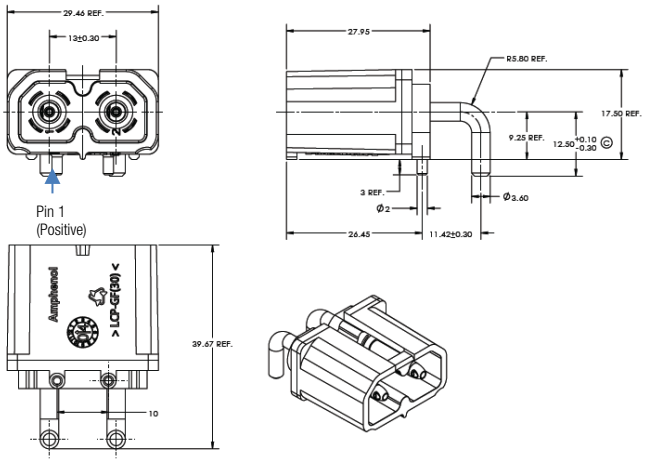
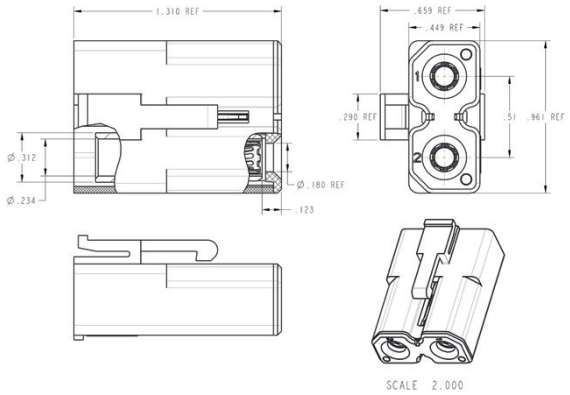


Figure 13: PW_OK Holdup

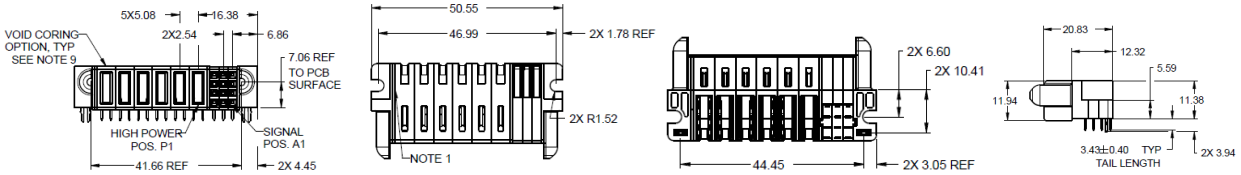
Figure 14: PW_OK Warning Time

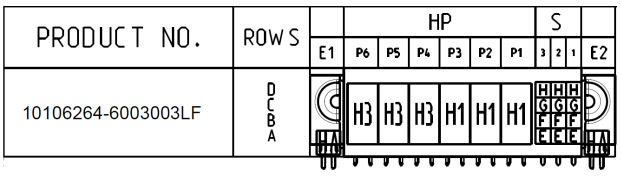
Figure 15: Input Fail Warning Time

CONNECTOR, DC INPUT

Part Number	Description	Outline
• Manufacturer: Amphenol • Manufacturers Type: Amphenol, RADSOK® Receptacle • Manufacturers Part Number: • C10-752109-000 • Material: Housing LCP Black; Pin Copper, Silver Plated; Clip Beryllium Copper • Electrical: Rated 250VDC; Max Continuous Load Current 69ADC	Power Module; two position PCB mounted Receptacle Connector Pin 1 = Positive, Pin 2 = Negative	
• Manufacturer: Amphenol • Manufacturers Type: Amphenol, RADSOK® Plug • Manufacturers Part Number: • C10-752158-000; BLACK, 3,6MM - AWG 6 • Material: Housing PBT Black; Contact Copper, Silver Plated; Positioner PBT Black • Electrical: Rated 250VDC; Max Continuous Load Compatible with Receptacle	Mating two position Plug Connector with Crimp Terminals	

DC OUTPUT & SIGNAL INTERFACE MATING CONNECTOR

Part Number	Description
• Manufacturer: Amphenol FCI • Manufacturers Type: Power Blade RA STB PLUG • Manufacturers Part Number: 10106264-6003003LF (PSU Side connector 10106262-6003006LF)	



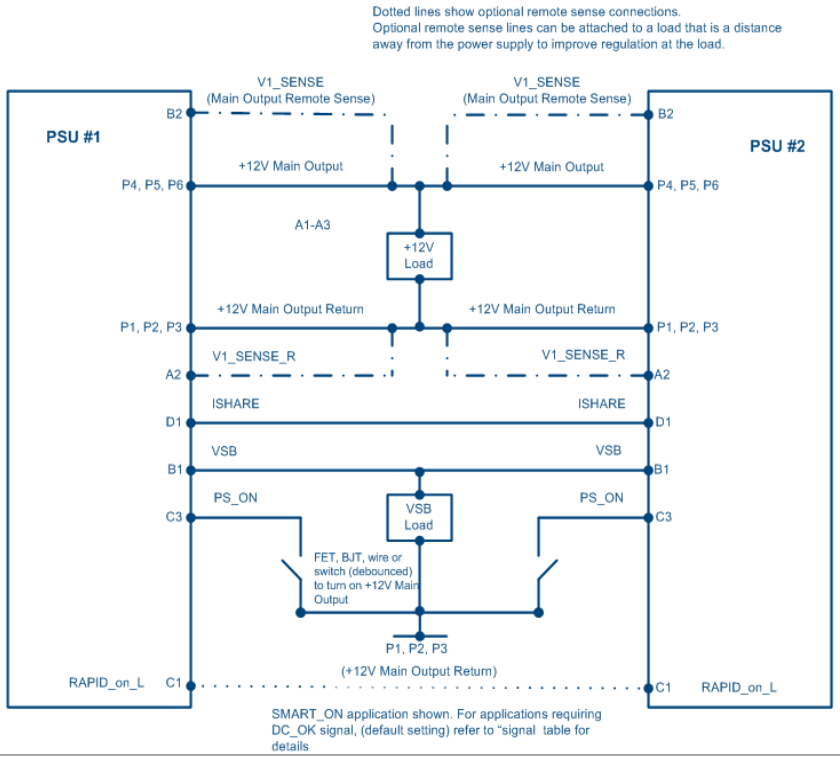
CODE	DESCRIPTION
E	STD SIGNAL CONTACT, ROW A
F	STD SIGNAL CONTACT, ROW B
G	STD SIGNAL CONTACT, ROW C
H	STD SIGNAL CONTACT, ROW D
H1	MFBL HIGH POWER CONTACT(3.43)
H3	STD HIGH POWER CONTACT(3.43)
HA	METAL HOLD DOWN

DC OUTPUT & SIGNAL INTERFACE PIN MAPPING

Pin	Signal Name	Comments
P4, P5, P6	V1_OUT	+ 12V Output;
P1, P2, P3	V1_RTN	+ 12V main and VStby Output return
A3	SDA	Short Pin; I2C data signal line
B3	SCL	Short Pin; I2C clock signal line
C3	PS_ON	Short Pin; Remote on/off (short pin)
D3	SMB_ALERT	Short Pin; I2C alert signal
A2	V1_SENSE_R	- Remote Sense return

Pin	Signal Name	Comments
B2	V1_SENSE	+ Remote Sense
C2	PW_OK	Power OK
D2	ADDR/PS_INHIBIT	Dual function I2C address selection and PS_INHIBIT
A1	PRESENT_L	PS_Present
B1	VSTANDBY	+ Standby output
C1	DCOK / RAPID_ON	Selectable via PMBus
D1	ISHARE	Current share bus

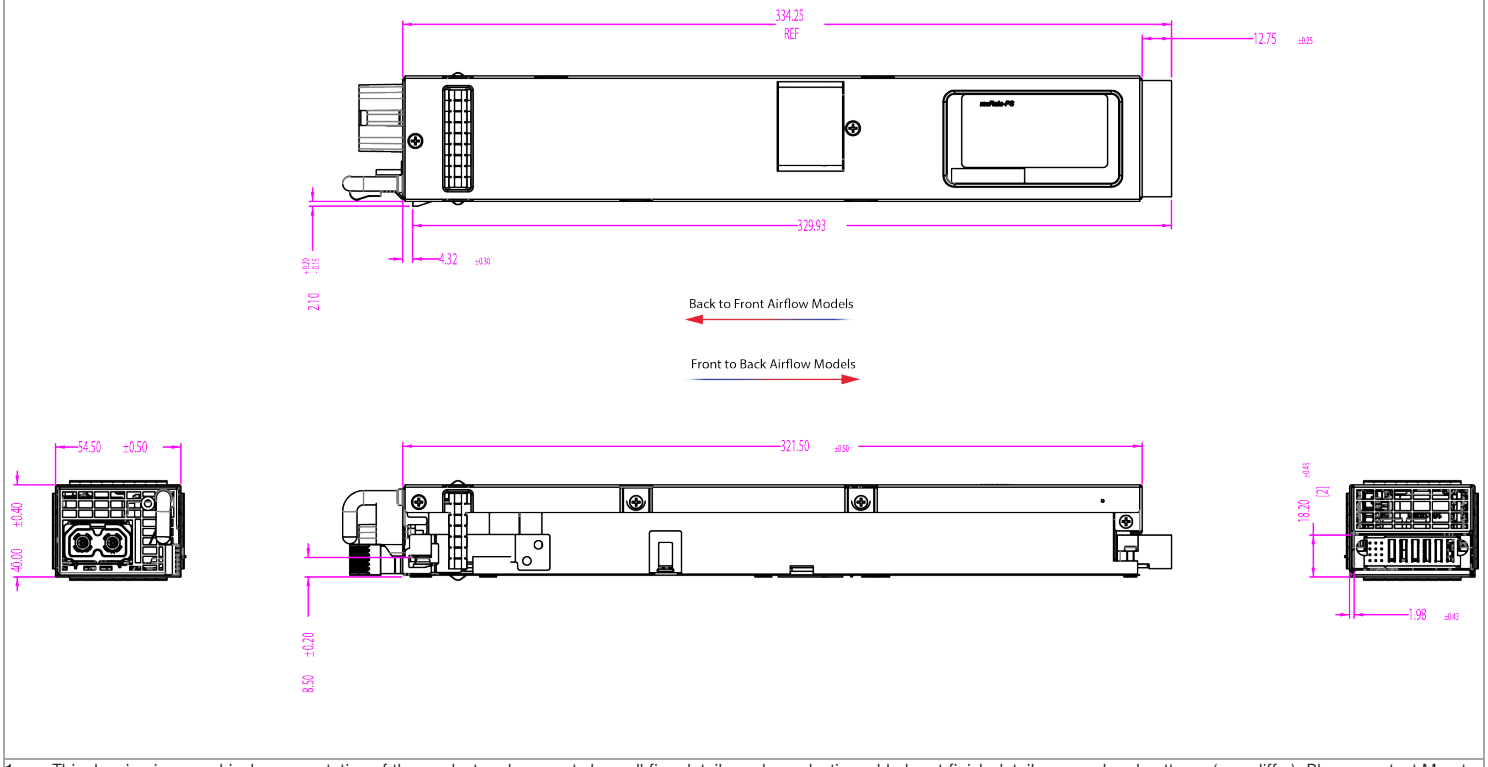
WIRING DIAGRAM



CURRENT SHARING NOTES

1. Main Output current sharing is achieved using the active current share method.
2. Current sharing can be achieved with or without the remote (V_SENSE) connected to the common load.
3. +VSB Outputs can be tied together for redundancy but total combined output power must not exceed the rated standby power of a single unit. The +VSB output has an internal ORING MOSFET for additional redundancy/internal short protection.
4. Main output power of units sharing must not exceed the rated power of a single unit during power up.
5. The current sharing pin D1 is connected between sharing units (forming an ISHARE bus). It is an input and/or an output (bi-directional analog bus) as the voltage on the line controls the current share between sharing units. A power supply will respond to a change in this voltage but a power supply can also change the voltage depending on the load drawn from it. On a single unit the voltage on the pin (and the common ISHARE bus would read approximately 8VDC at 100% load (power module capability). For two units sharing the same load this would read approximately 4VDC for perfect current sharing (i.e. 50% power capability per unit).
6. The load for both the main 12V and the VSB outputs at initial startup shall not be allowed to exceed the capability of a single unit. The load can be increased after a delay of 3 sec (minimum), to allow all sharing units to achieve steady state regulation

MECHANICAL OUTLINE



1. This drawing is a graphical representation of the product and may not show all fine details such as plastic molded part finish details, screw head patterns (may differ). Please contact Murata for 3D model for details
2. Dimensions in mm
3. Subject to change. Contact factory for latest version.
4. File Reference: D75090021321 rev. A

OPTIONAL ACCESSORIES

Description	Part Number
Connector Card	D1U54P-12-CONC2K

APPLICATION NOTES

Document Number	Description	Link (to be activated)
ACAN-82	D1U54P-12-CONC2K, Output Connector Card	URL Link: Click to open
ACAN-117	D1U54-D-2500-12-HBxC PMBus™ Protocol	URL Link: Click to open

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ISO 9001 REGISTERED

This product is subject to the following operating requirements and the Life and Safety Critical Application Sales Policy: Refer to: https://www.murata-ps.com/requirements/