AN13049

Wi-Fi/Bluetooth/802.15.4 M.2 Key E Pinout Definition

Rev. 6.0 — 17 March 2025 **Application note**

Document information

Information	Content
Keywords	AN13049, Wi-Fi, Bluetooth, 802.15.4, M.2, pinout, Tri-Radio
Abstract	This document defines M.2 usage for both NXP Wi-Fi/Bluetooth and Tri-Radio M.2 module design.

1 Introduction

M.2 is a form factor for mobile adapters defined by the PCI-SIG (http://www.pcisig.com). The pinouts for M.2 sockets are defined in the PCI Express M.2 Specification.

M.2 sockets with mechanical Key E are used on platforms based on NXP MPUs and MCUs to support wireless connectivity modules based on NXP Wi-Fi/Bluetooth/802.15.4 radios.

Some of the signals defined in the pinout are used to connect optional sideband and debug signals used by NXP Wi-Fi/Bluetooth/802.15.4 radios.

To ensure proper connection for the sideband and debug signals, this document defines the pin assignments for M.2 sockets (mechanical Key E) on platforms based on NXP MPUs and MCUs.

This document defines M.2 usage for both NXP Wi-Fi/Bluetooth and Tri-Radio M.2 module design.

Figure 1 shows NXP Single/Dual Radio M.2 interface block diagram.

Figure 2 shows NXP Tri-Radio M.2 interface block diagram. It must add SPI interface for 802.15.4 device, and add an I/O expander to support sideband control signals.

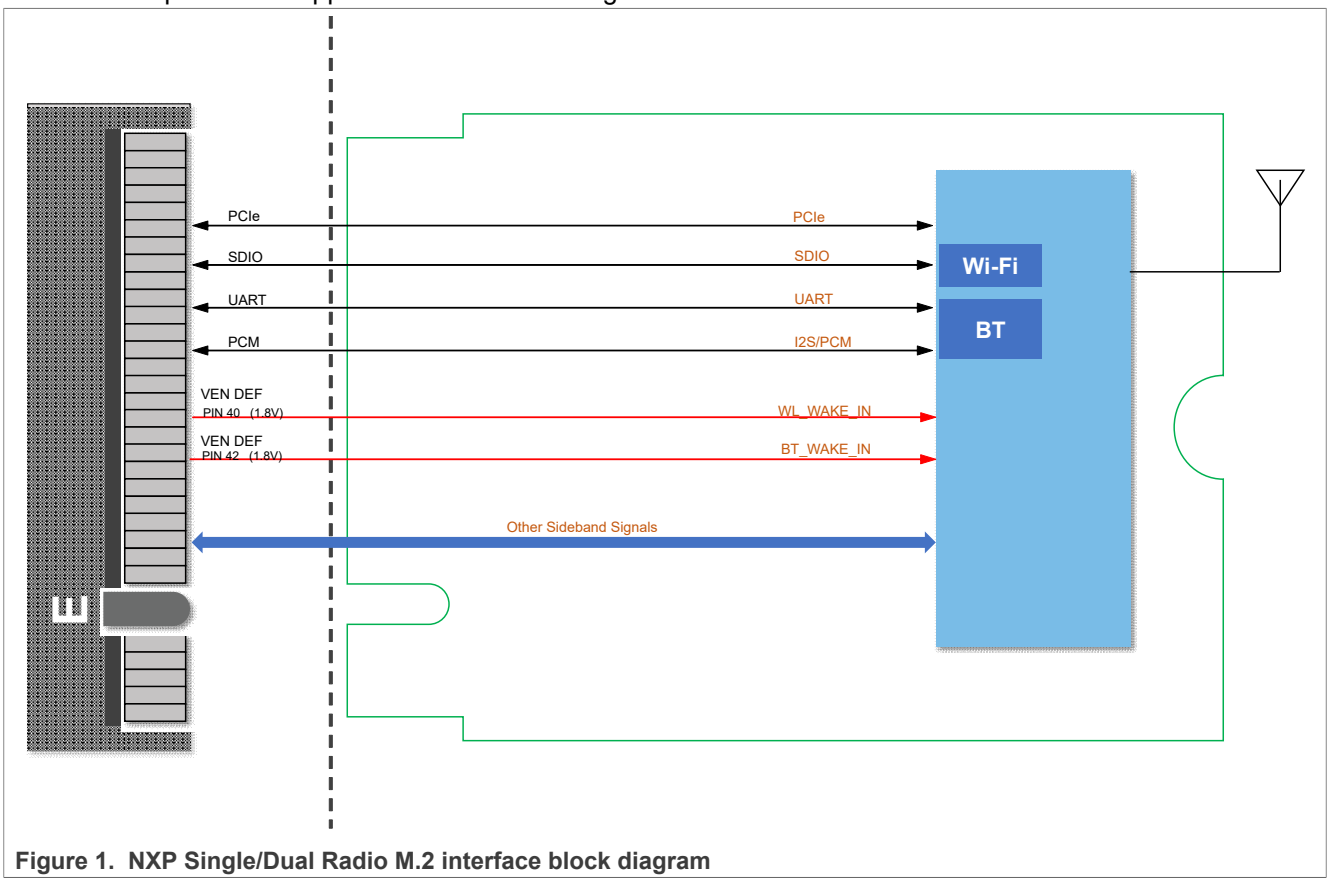

Figure 1. NXP Single/Dual Radio M.2 interface block diagram

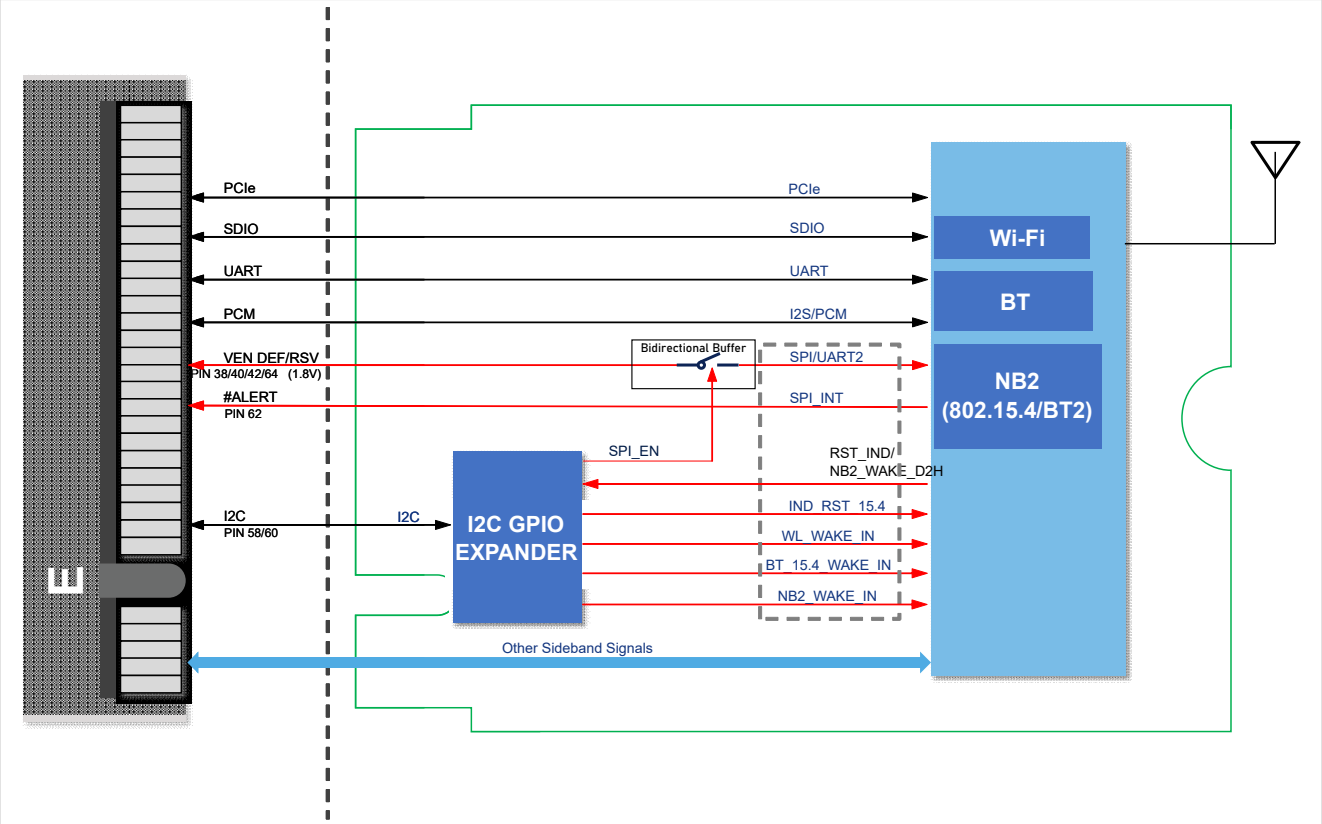

Figure 2. NXP Tri-Radio M.2 interface block diagram

Before building your board, check the interface connector specification from the wireless module vendor to confirm the pinout used by the module.

For the full definition of the socket pinout, see the *PCI Express M.2 Specification*, available from PCI-SIG website (http://www.pcisig.com).

Note: *All the pins that are not listed in this document are recommended to follow the PCI Express M.2 Type E specification or should not be connected.*

2 Usage signals for Wi-Fi/Bluetooth and Tri-Radio

This section describes the NXP defined sideband control and SPI signals between the NXP Radio module and MPU/MCU.

Table 1 shows the pin assignments utilized for sideband and SPI signals.

Note: *For details on the mandatory and optional lines, see the module data sheet.*

Table 1. Sideband and SPI signals

Pin	PCIe M.2 Signal	Type[1]	Voltage	Usage for NXP Single/Dual Radio	Usage for NXP Tri-Radi
10	PCM_SYNC	I/O	1.8 V	PCM_SYNC: PCM frame sync signal	PCM_SYNC: PCM frame sync signal. BLE_HOST_TRIG: Host_Trigger pin for Bluetooth LE.

Table 1. Sideband and SPI signals*...continued*

Pin	PCIe M.2 Signal	Type[1]	Voltage	Usage for NXP Single/Dual Radio	Usage for NXP Tri-Radi
20	UART_ WAKE#	I	3.3 V	BT_WAKE_OUT: Bluetooth radio to wake up the MPU/MCU. Active Low by default. Connect to MPU/MCU GPIO open-drain. Pullup required on a platform.	BT_15.4_WAKE_OUT: Bluetooth radio to wake up the MPU/MCU. Active Low by default. Connect to MPU/MCU GPIO open-drain. Pullup required on a platform.
21	SDIO_WAKE#	I	1.8 V	WL_WAKE_OUT: Wi-Fi radio to wake up the MPU/MCU. Active Low by default. Connect to MPU/MCU open-drain. Pullup required on platform.	Same as single/dual radio.
23	SDIO_ RESET#	O	1.8 V	IND_RST_WL: Independent software reset for Wi-Fi. Active Low by default. Connect to MPU/MCU GPIO.	IND_RST_WL: Independent software reset for Wi-Fi. PDn_NB2: Power down narrow band device-2. Active Low by default. Connect to MPU/MCU GPIO.
38	VENDOR DEFINED	I/O	1.8 V	NC	SPI_TXD(O): SPI transmit signal. UART2_CTS(I): UART2 clear-to-send signal.
40	VENDOR DEFINED	I/O	1.8 V	WL_WAKE_IN: MPU/MCU to wake up the Wi-Fi radio. Active Low by default. Connect to MPU/MCU GPIO.	SPI_RXD: SPI receive signal. UART2_RX: UART2 serial input signal. .
42	VENDOR DEFINED	O	1.8 V	BT_WAKE_IN: MPU/MCU to wake up the Bluetooth radio. Active Low by default. Connect to MPU/MCU GPIO.	SPI_CLK: SPI clock signal. UART2_RTS: UART2 request-to-send output signal.
44	COEX3	I/O	1.8 V	Talk to the NXP support team.	Same as single/dual radio.
46	COEX2	I	1.8 V	Talk to the NXP support team. COEX_RXD: UART receive signal for COEX.	Same as single/dual radio.
48	COEX1	O	1.8 V	Talk to the NXP support team. COEX_TXD: UART transmit signal for COEX.	Same as single/dual radio.
54	W_ DISABLE2#	O	3.3 V	IND_RST_BT: Independent software reset for Bluetooth. Active low by default connect to MPU/MCU GPIO.	IND_RST_BT: Independent software reset for Bluetooth. PDn_NB1: Power down narrow band device-1. Active low by default connect to MPU/MCU GPIO.

Table 1. Sideband and SPI signals...*continued*

Pin	PCIe M.2 Signal	Type[1]	Voltage	Usage for NXP Single/Dual Radio	Usage for NXP Tri-Radi
56	W_ DISABLE1#	O	3.3 V	PDn: Full power down for the Wi-Fi/ Bluetooth radio or controls the PMIC ENABLE signal. High = Normal Low = Full Power-down mode Connect to MPU/MCU GPIO.	PDn: Full power down for the Wi-Fi/Bluetooth radio or controls the PMIC ENABLE signal. PDn_WLAN: Power down Wi-Fi device. Active Low by default. Connect to MPU/MCU GPIO.
58	I2C_DATA	I/O	1.8 V	NC	I2C SDA: I2C data for I/O expander. Open-drain. Pullup required on a platform. See Table 2.
60	I2C_CLK	O	1.8 V	NC	I2C SCL: I2C clock from MPU/MCU for I/O expander. See Table 2.
62	ALERT#	I	1.8 V	NC	SPI_INT: SPI interrupt signal. Open-drain. Pullup required on a platform.
64[2]	RESERVED	O	1.8 V	NC	SPI_FRM: SPI frame signal. UART2_TX: UART2 serial output signal.

[1] Type refers to the signal direction:
- Type O means that a signal is an output from the MPU/MCU to the adapter.
- Type I means that the signal is an input to the MPU/MCU from the adapter.

[2]
- To avoid the potential risk on which 1.8 V is designed on other platforms, optionally add a serial 100-1K ohm resistor on the path from SPI_FRM to M.2 PIN64.
- On the Tri-radio M.2 adapter side for the SPI signals, follow the SPI signal definitions based on M.2 Spec Rev 3.0 in the application note document. Do not follow the M.2 Spec Rev 4.0 signal definitions.
- On the host side, the SPI signal definitions on M.2 connector should be consistent as mentioned in the application note document. Otherwise, the 802.15.4 transceiver of the Tri-radio M.2 adapter cannot work normally. However, this does not impact the Wi-Fi and Bluetooth of the Tri-radio adapter.

2.1 I2C I/O expander for sideband signals

For a Tri-Radio M.2 module, it uses an I2C expander to support sideband control signals. It is important to use an NXP PCAL6408A part. It is an 8-bit general-purpose I/O expander that provides GPIO expansion via the I2C bus interface (Default I2C Address: 0x20). See the I/O expander port assignment or the sideband signals in Table 2.

Table 2. I/O expander function

Symbol	Type	Voltage	NXP Usage	Description
P0	O	VIO	SPI Buffer enable	Enable SPI Buffer when Tri-radio is designed. Active high by default. Pull down required on M.2 board.
P1	O	VIO	IND_RST_15.4	Independent software reset for 802.15.4 radio. Active low by default.
P2	O	VIO	WL_WAKE_IN	MPU/MCU to wake up the Wi-Fi radio. Active low by default.

Table 2. I/O expander function*...continued*

Symbol	Type	Voltage	NXP Usage	Description
P3	O	VIO	BT_15.4_W AKE_IN	MPU/MCU to wake up the Bluetooth and 802.15.4 radio. Active low by default.
P4	I	VIO	RST_IND NB2_WAKE_D2H	RST_IND: Independent software reset indicator output signal to host. NB2_WAKE_D2H: Narrow band device-2 to wake up the MPU/MCU. Active Low by default.
P5	O	VIO	NB2_WAKE_IN	MPU/MCU to wake up the narrow band device-2. Active low by default.
P6-P7	Reserved			Not used. Recommend to add test pads on P6-P7.

3 Host and audio interfaces

The wireless connectivity module may support an audio interface.

The modules may also support various host interfaces including SDIO, UART[1], or PCI Express.

For the pin assignments on these interfaces, see the PCI_Express_M.2_Spec document on http://www.pcisig.com.

4 JTAG debug signals

The JTAG debug signals JTAG_TDI, JTAG_TDO, JTAG_TCK, and JTAG_TMS are used to support Software development. Keeping a JTAG connector (Hirose FH12-10S-0.5SH(55)) or test pads on the M.2 module is recommended.

5 COEX signals

There are some coexistence (COEX) signals not defined in the M.2 Key-E interface. The sideband signals of coexistence and audio Host Trig must bring out to header pins.

Table 3. COEX signals

NXP Usage	Type	Voltage	Description
BLE_HOST_TRIG0/1/2	I/O	VIO	Host_Trigger pins for Bluetooth LE and host. Host GPIOs must support a capture function.
PTA coexistence interface	I/O	VIO	PTA COEX signal connecting to External radio. EXT_REQ: Request from the external radio. EXT_PRI: External radio input priority signal. EXT_GNT: External radio grants an output signal.
Second UART coexistence interface	I/O	VIO	Second UART COEX signal connecting to External radio. COEX TXD2: UART transmits a signal to COEX. COEX RXD2: UART receives a signal from COEX.

1 CTS and RTS flow control lines are requested for Bluetooth control.

Note: *It is recommended to add a power/ground pin on the header.*

6 Revision history

Table 4 summarizes the changes to this document.

Table 4. Revision history

Document ID	Release date	Description
AN13049 v.6.0	17 March 2025	Updated Table 1 and Table 2.
AN13049 v.5.0	17 February 2025	Updated Figure 2, Table 1, and Section 2.1. Added Section 5.
AN13049 v.4.0	30 May 2023	Updated Section 2 and added Section 3.
AN13049 v.3.0	17 January 2022	Added the usage for Tri-Radio design. Removed the JTAG signals from the M.2 pins.
AN13049 v.2.0	16 September 2021	Updated Section 1 and Section 2.
AN13049 v.1.0	12 November 2020	Initial version

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