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MOSFET – Power, Single, N-Channel

100 V, 17.8 mΩ, 33 A

Product Preview

FDD86080-F085

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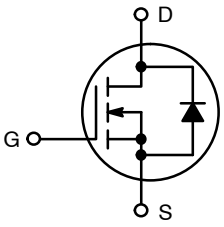
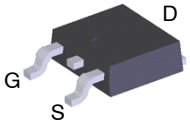
Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR−Free and are RoHS Compliant

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
100 V	17.8 mΩ @ 10 V	33 A



POWER MOSFET



DPAK
TO−252
CASE 369AS

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	100	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25°C	I_D	33.6	A
		T_C = 100°C		23.7	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	44.1	W
		T_C = 100°C		22.1	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	I_D	8.9	A
		T_A = 100°C		6.3	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	P_D	3.1	W
		T_A = 100°C		1.5	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	199	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	36.8	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 2 A)			E_{AS}	234	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

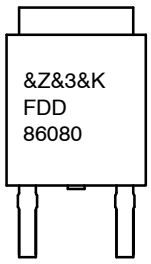
THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State	$R_{\theta JC}$	3.4	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	48.7	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
FDD86080	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA	100	–	–	V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$		–	58.5	–	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 100 V, T_J = 25°C	–	–	1	μA
Zero Gate Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	–	–	±100	nA
ON CHARACTERISTICS (Note 4)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 58 μA	2	3.2	4.5	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$		–	−7.5	–	mV/°C
Drain to Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A	–	15.3	17.8	mΩ
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 50 V	–	777	–	pF
Output Capacitance	C_{oss}		–	478	–	
Reverse Transfer Capacitance	C_{rss}		–	6.6	–	
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 50 V, I_D = 10 A	–	10.6	–	nC
Threshold Gate Charge	$Q_{g(th)}$		–	1.5	–	
Gate to Source Charge	Q_{gs}		–	4	–	
Gate to Drain “Miller” Charge	Q_{gd}		–	2	–	
Plateau Voltage	V_{GP}		–	5.1	–	V
SWITCHING CHARACTERISTICS						
Turn−On Delay Time	$t_{d(ON)}$	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 10 A, R_g = 6 Ω	–	5.5	–	ns
Turn−On Rise Time	t_r		–	9.6	–	
Turn−Off Delay Time	$t_{d(OFF)}$		–	10.4	–	
Turn−Off Fall Time	t_f		–	7.5	–	
DRAIN−SOURCE DIODE CHARACTERISTICS						
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 10 A, V_{GS} = 0 V	–	0.84	1.2	V
Reverse Recovery Time	T_{RR}	V_{GS} = 0 V, dI_{SD}/dt = 100 A/μs, I_S = 10 A	–	35	–	ns
Charge Time	t_a		–	18	–	
Discharge Time	t_b		–	17	–	
Reverse Recovery Charge	Q_{RR}		–	28	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

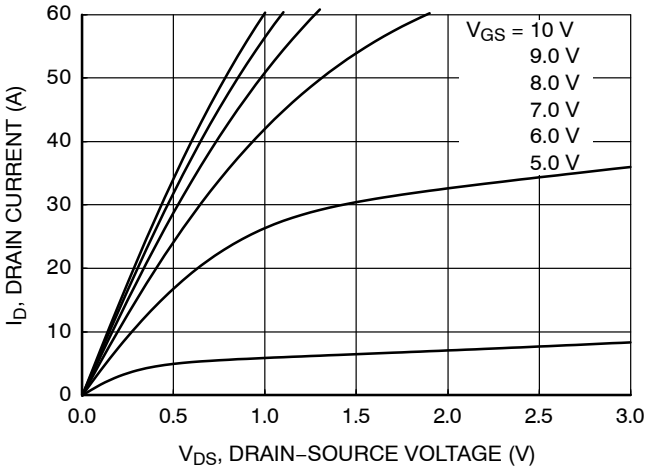


Figure 1. On−Region Characteristics

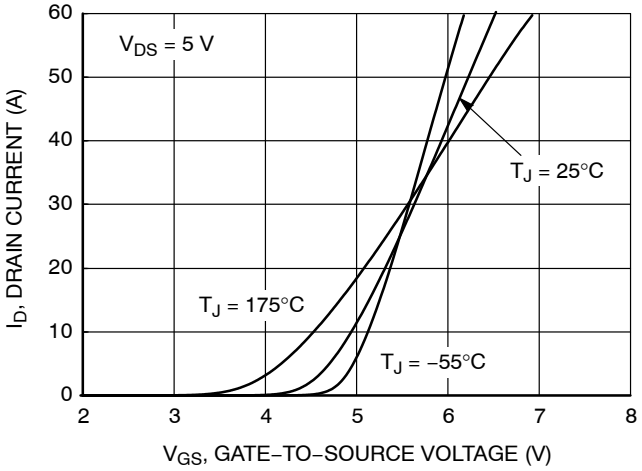


Figure 2. Transfer Characteristics

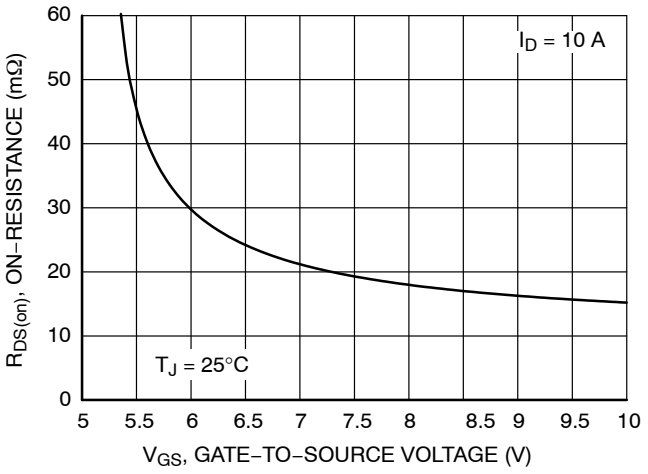


Figure 3. On−Resistance vs. V_{GS}

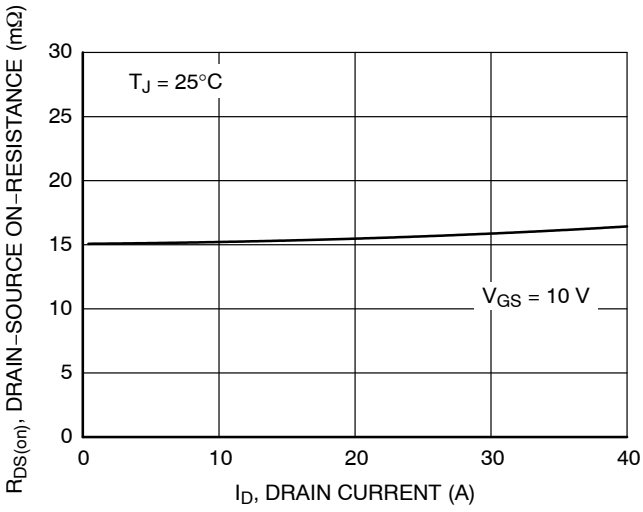


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

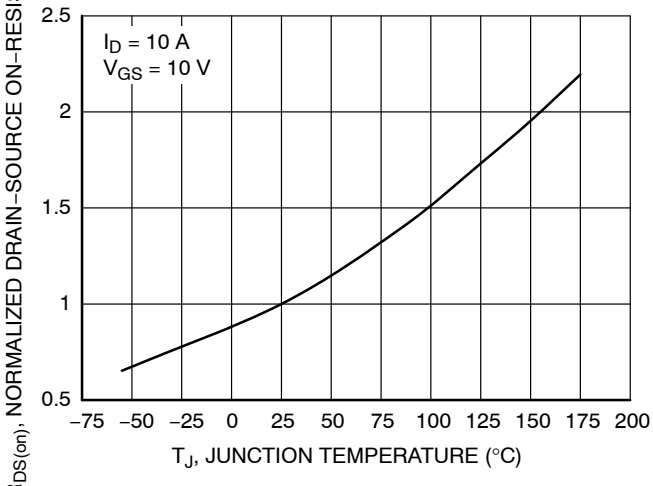


Figure 5. On−Resistance Variation with Temperature

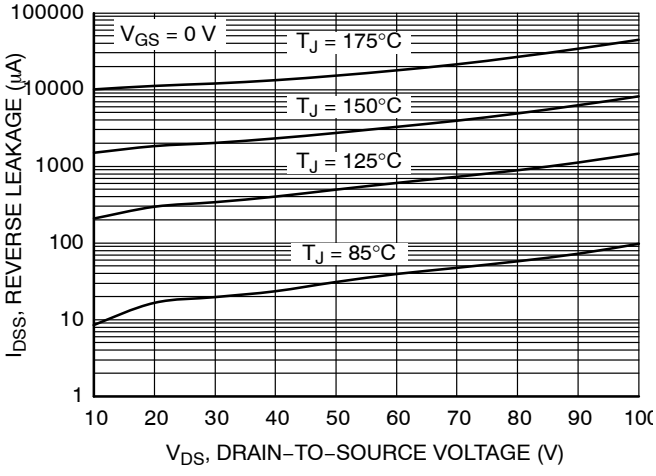


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

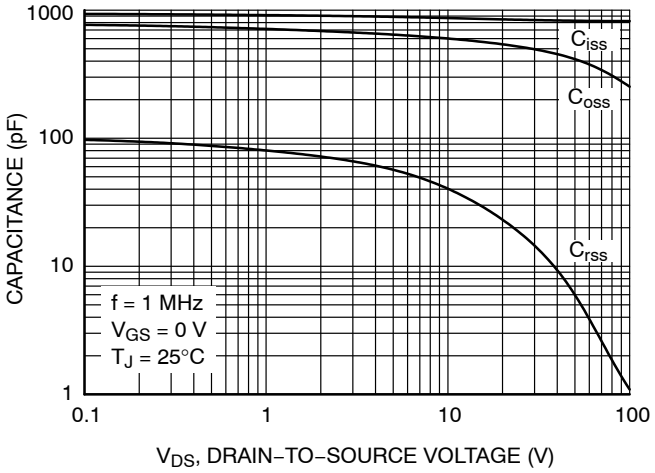


Figure 7. Capacitance Variation

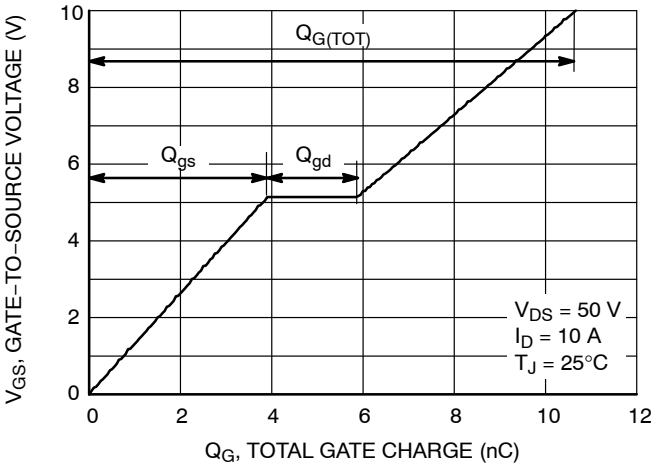


Figure 8. Gate−to−Source Voltage vs. Total Gate Charge

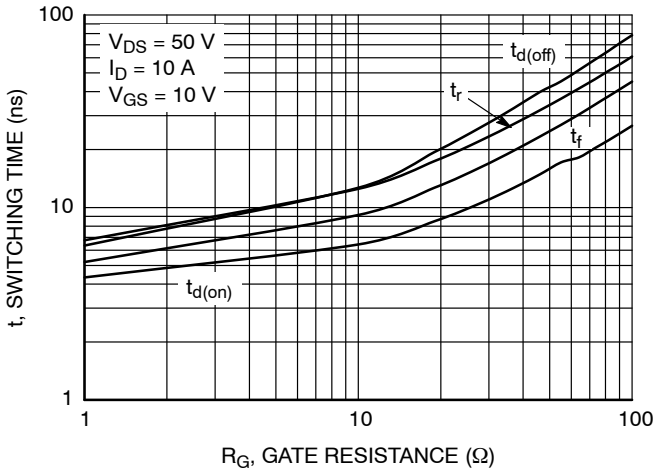


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

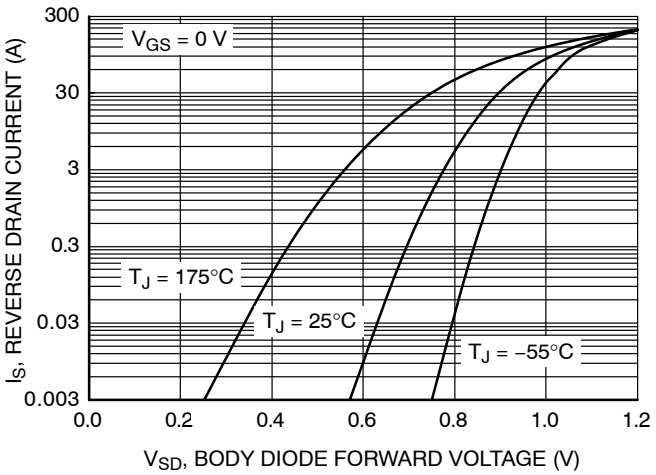


Figure 10. Diode Forward Voltage vs. Current

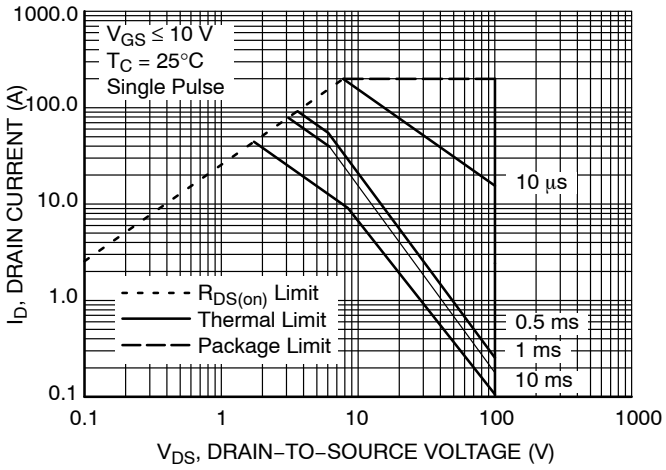


Figure 11. Maximum Forward Bias Safe Operating Area

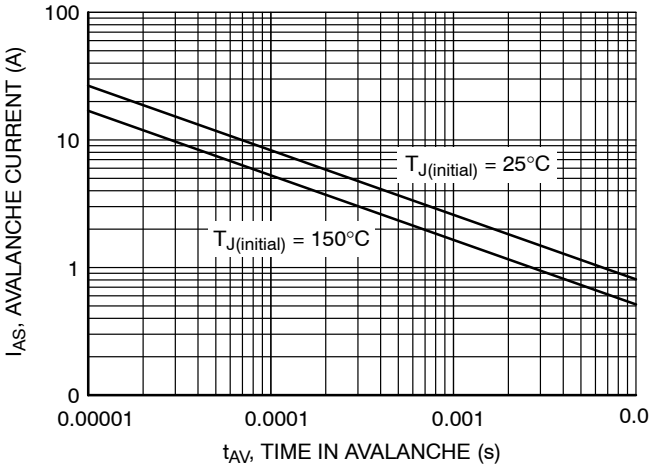


Figure 12. Avalanche Characteristics

TYPICAL CHARACTERISTICS

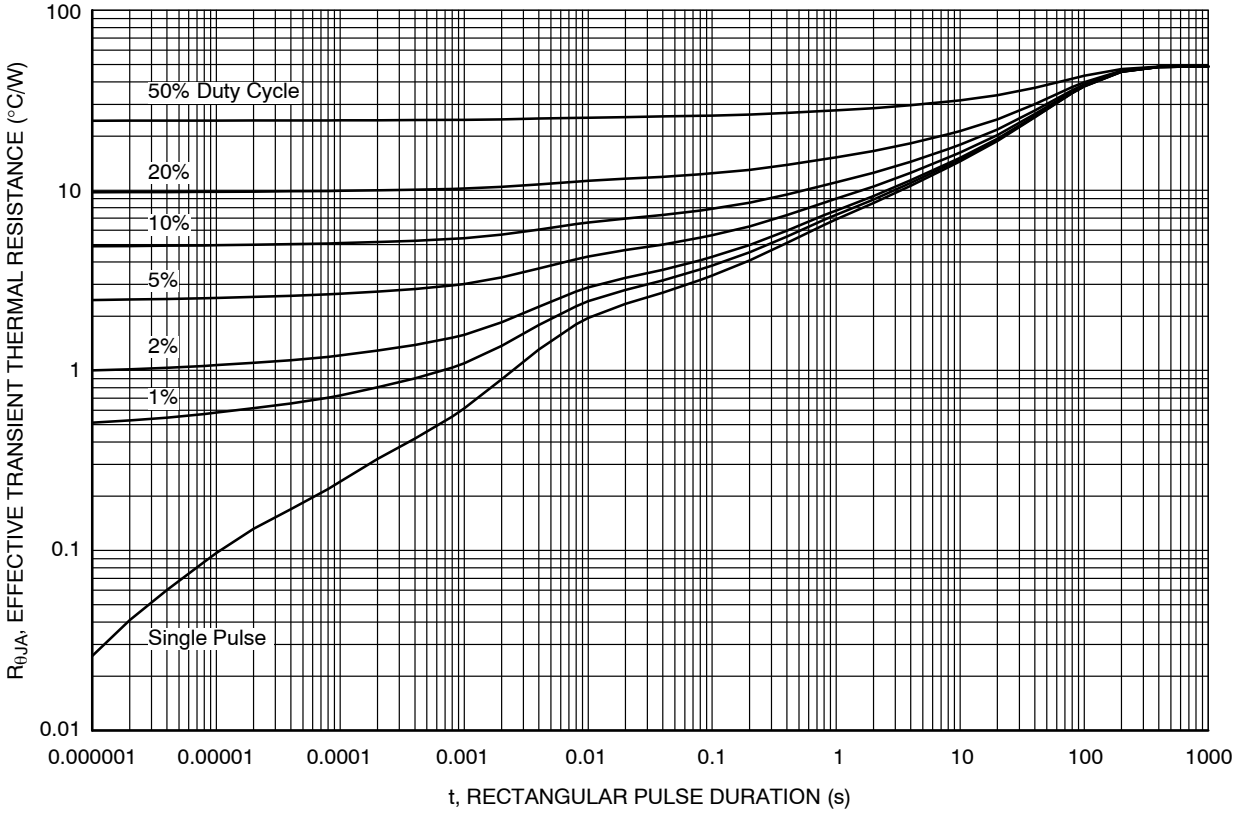


Figure 13. Thermal Response

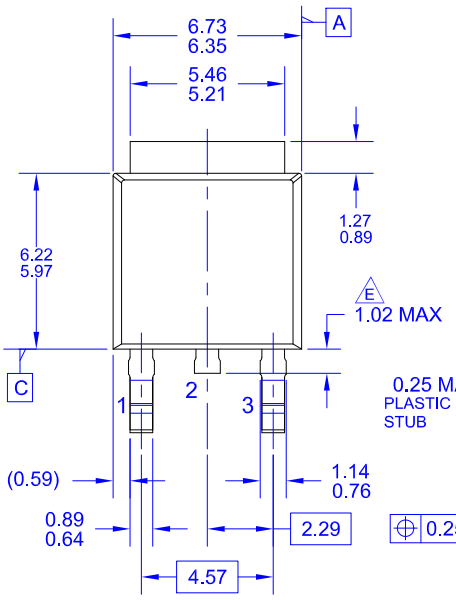
DEVICE ORDERING INFORMATION

Device	Marking	Package	Reel Size	Tape Width	Shipping†
FDD86080−F085	FDD86080	DPAK (TO−252) (Pb−Free)	13″	16 mm	2500 / Tape & Reel

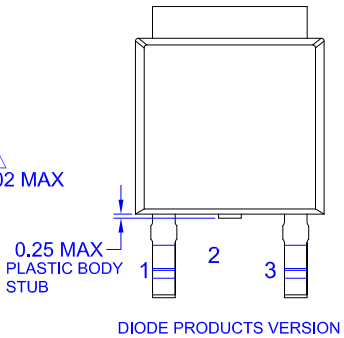
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

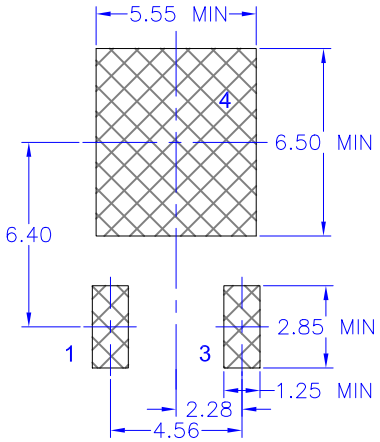
DPAK3 (TO−252 3 LD)
CASE 369AS
ISSUE O



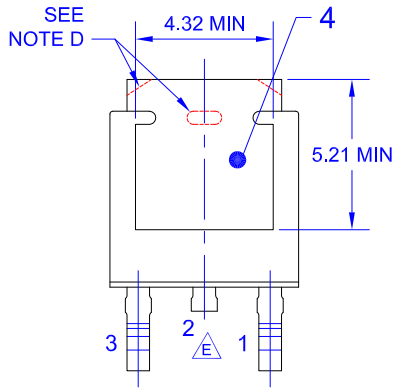
NON-DIODE PRODUCTS VERSION



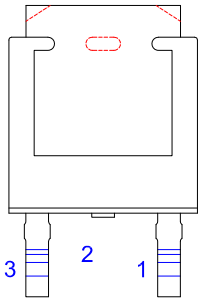
DIODE PRODUCTS VERSION



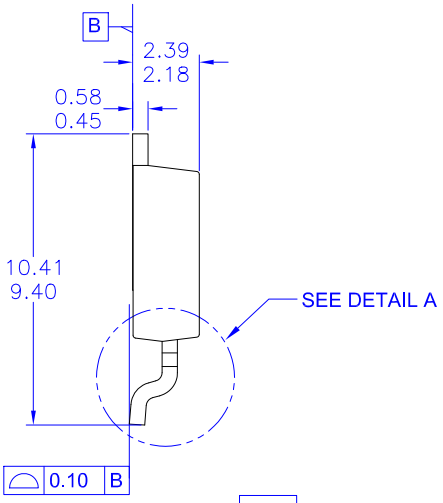
LAND PATTERN RECOMMENDATION

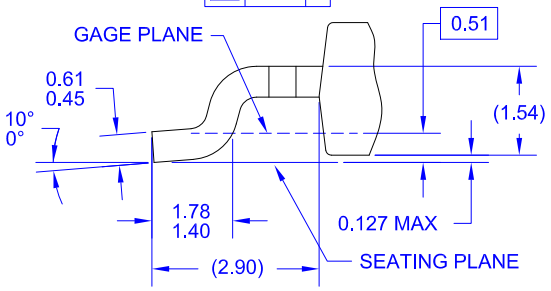


NON-DIODE PRODUCTS VERSION



DIODE PRODUCTS VERSION





DETAIL A
(ROTATED -90°)
SCALE: 12X

NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

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Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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