

EcoSPARK[®] 3 Ignition IGBT

200 mJ, 400 V, N-Channel Ignition IGBT

FGD2040G3-F085

Features

- SCIS Energy = 200 mJ at $T_J = 25^\circ\text{C}$
- Low Saturation Voltage
- Logic Level Gate Drive
- AEC-Q101 Qualified and PPAP Capable
- RoHS Compliant

Applications

- Automotive Ignition Coil Driver Circuits
- High Current Ignition System
- Coil on Plug Applications

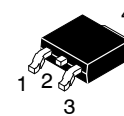
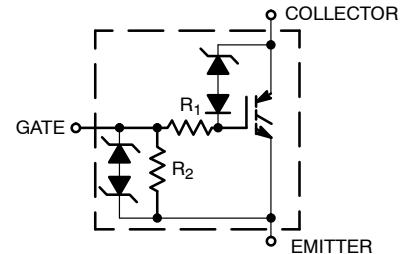
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter	Value	Units
BV_{CER}	Collector-to-Emitter Breakdown Voltage ($I_C = 1\text{ mA}$)	400	V
BV_{ECS}	Emitter-to-Collector Voltage – Reverse Battery Condition ($I_C = 10\text{ mA}$)	28	V
$ESCIS_{25}$	ISCIS = 11.5 A, L = 3.0 mHy, $R_{GE} = 1\text{ K}\Omega$, $T_C = 25^\circ\text{C}$ (Note 1)	200	mJ
$ESCIS_{150}$	ISCIS = 9.1 A, L = 3.0 mHy, $R_{GE} = 1\text{ K}\Omega$, $T_C = 150^\circ\text{C}$ (Note 2)	125	mJ
I_{C25}	Collector Current Continuous at $V_{GE} = 5.0\text{ V}$, $T_C = 25^\circ\text{C}$	23.6	A
I_{C110}	Collector Current Continuous at $V_{GE} = 5.0\text{ V}$, $T_C = 110^\circ\text{C}$	13.6	A
V_{GEM}	Gate-to-Emitter Voltage Continuous	± 10	V
P_D	Power Dissipation Total, $T_C = 25^\circ\text{C}$	125	W
	Power Dissipation Derating, $T_C > 25^\circ\text{C}$	0.83	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 175	$^\circ\text{C}$
T_L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	300	$^\circ\text{C}$
T_{PKG}	Reflow soldering according to JESD020C	260	$^\circ\text{C}$
ESD	HBM – Electrostatic Discharge Voltage at 100 pF, 1500 Ω	4	kV
	CDM – Electrostatic Discharge Voltage at 1 Ω	2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

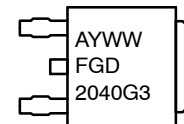
1. Self Clamped inductive Switching Energy (ESCIS25) of 200 mJ is based on the test conditions that is starting $T_J = 25^\circ\text{C}$, L = 3 mHy, ISCIS = 11.5 A, $V_{CC} = 100\text{ V}$ during inductor charging and $V_{CC} = 0\text{ V}$ during time in clamp.
2. Self Clamped inductive Switching Energy (ESCIS150) of 125 mJ is based on the test conditions that is starting $T_J = 150^\circ\text{C}$, L = 3mHy, ISCIS = 9.1 A, $V_{CC} = 100\text{ V}$ during inductor charging and $V_{CC} = 0\text{ V}$ during time in clamp.

200 mJ, 400 V
 $V_{CE(on)} = 1.6\text{ V}$
 @ $I_C = 6\text{ A}$, $V_{GE} = 4\text{ V}$



DPAK (SINGLE GAUGE)
 CASE 369C

MARKING DIAGRAM



A = Assembly Location
 Y = Year
 WW = Work Week
 FGD2040G3 = Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FGD2040G3–F085

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction-to-Case – Steady State (Drain)	$R_{\theta JC}$	1.2	°C/W

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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OFF CHARACTERISTICS

BV_{CER}	Collector-to-Emitter Breakdown Voltage	$I_{CE} = 2\text{ mA}$, $V_{GE} = 0\text{ V}$, $R_{GE} = 1\text{ k}\Omega$, $T_J = -40\text{ to }150^\circ\text{C}$		370	–	430	V
BV_{CES}	Collector-to-Emitter Breakdown Voltage	$I_{CE} = 10\text{ mA}$, $V_{GE} = 0\text{ V}$, $R_{GE} = 0$, $T_J = -40\text{ to }150^\circ\text{C}$		390	–	450	V
BV_{ECS}	Emitter-to-Collector Breakdown Voltage	$I_{CE} = -75\text{ mA}$, $V_{GE} = 0\text{ V}$, $T_J = 25^\circ\text{C}$		28	–	–	V
BV_{GES}	Gate-to-Emitter Breakdown Voltage	$I_{GES} = \pm 2\text{ mA}$		± 12	± 14	–	V
I_{CER}	Collector-to-Emitter Leakage Current	$V_{CE} = 250\text{ V}$ $R_{GE} = 1\text{ k}\Omega$	$T_J = 25^\circ\text{C}$	–	–	25	μA
			$T_J = 150^\circ\text{C}$	–	–	1	mA
I_{ECS}	Emitter-to-Collector Leakage Current	$V_{EC} = 24\text{ V}$	$T_J = 25^\circ\text{C}$	–	–	1	mA
			$T_J = 150^\circ\text{C}$	–	–	40	
R_1	Series Gate Resistance			–	144	–	Ω
R_2	Series Gate Resistance			10K	–	26K	Ω

ON CHARACTERISTICS

$V_{CE(SAT)}$	Collector-to-Emitter Saturation Voltage	$I_{CE} = 6\text{ A}$, $V_{GE} = 4\text{ V}$, $T_J = 25^\circ\text{C}$	–	1.34	1.6	V
$V_{CE(SAT)}$	Collector-to-Emitter Saturation Voltage	$I_{CE} = 10\text{ A}$, $V_{GE} = 4.5\text{ V}$, $T_J = 150^\circ\text{C}$	–	1.86	2.1	V

DYNAMIC CHARACTERISTICS

$Q_{G(ON)}$	Gate Charge	$I_{CE} = 10\text{ A}$, $V_{CE} = 12\text{ V}$, $V_{GE} = 5\text{ V}$		–	14.9	–	nC
$V_{GE(TH)}$	Gate-to-Emitter Threshold Voltage	$I_{CE} = 1\text{ mA}$ $V_{CE} = V_{GE}$	$T_J = 25^\circ\text{C}$	1.3	1.6	2.2	V
			$T_J = 150^\circ\text{C}$	0.75	1.2	1.8	
V_{GEP}	Gate-to-Emitter Plateau Voltage	$V_{CE} = 12\text{ V}$, $I_{CE} = 10\text{ A}$		–	4.3	–	V

SWITCHING CHARACTERISTICS

$t_{d(ON)R}$	Current Turn-On Delay Time–Resistive	$V_{CE} = 14\text{ V}$, $R_L = 1\text{ }\Omega$, $V_{GE} = 5\text{ V}$, $R_G = 470\text{ }\Omega$, $T_J = 25^\circ\text{C}$	–	0.4	1	μs
t_{rR}	Current Rise Time–Resistive		–	1.6	3	
$t_{d(OFF)L}$	Current Turn-Off Delay Time–Inductive	$V_{CE} = 300\text{ V}$, $L = 1\text{ mH}$, $V_{GE} = 5\text{ V}$, $R_G = 470\text{ }\Omega$, $I_{CE} = 6.5\text{ A}$, $T_J = 25^\circ\text{C}$	–	2.9	6	
t_{fL}	Current Fall Time–Inductive		–	3.7	8	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DEVICE ORDERING INFORMATION

Device	Package	Shipping [†]
FGD2040G3–F085	DPAK (Pb–Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

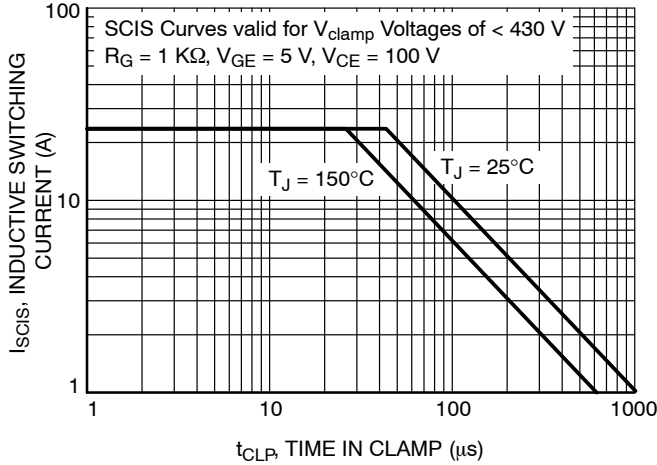


Figure 1. Self Clamped Inductive Switching Current vs. Time in Clamp

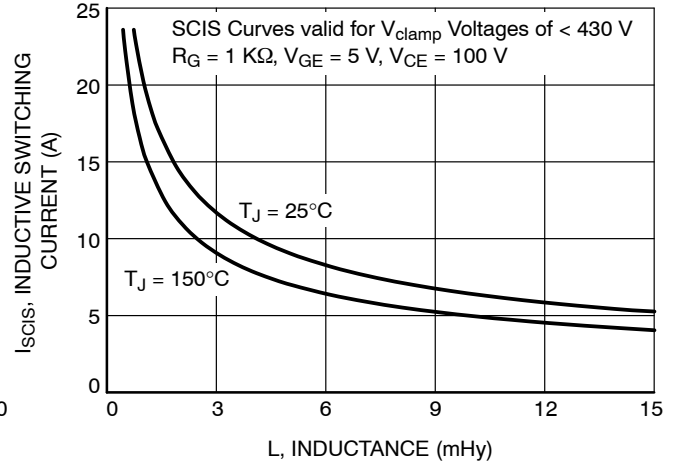


Figure 2. Self Clamped Inductive Switching Current vs. Inductance

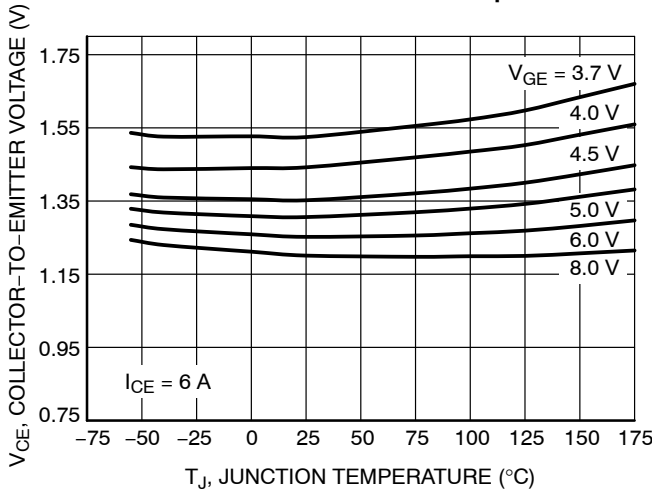


Figure 3. Collector-to-Emitter On-State Voltage vs. Junction Temperature

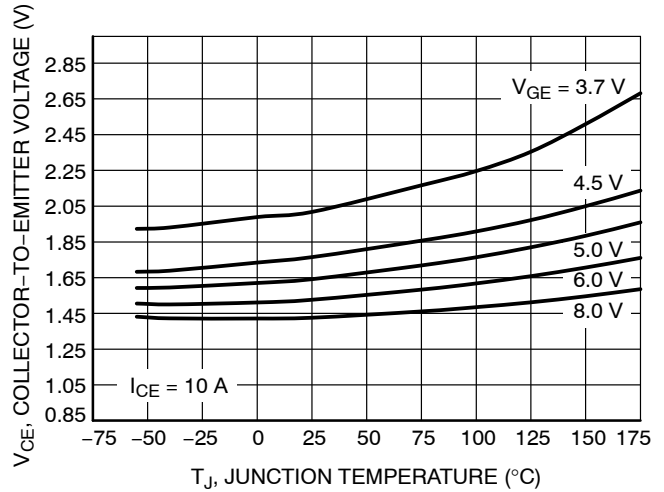


Figure 4. Collector-to-Emitter On-State Voltage vs. Junction Temperature

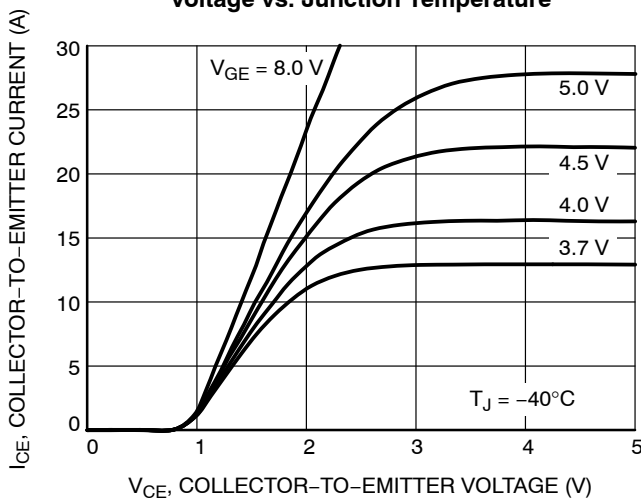


Figure 5. Collector-to-Emitter On-State Voltage vs. Collector Current

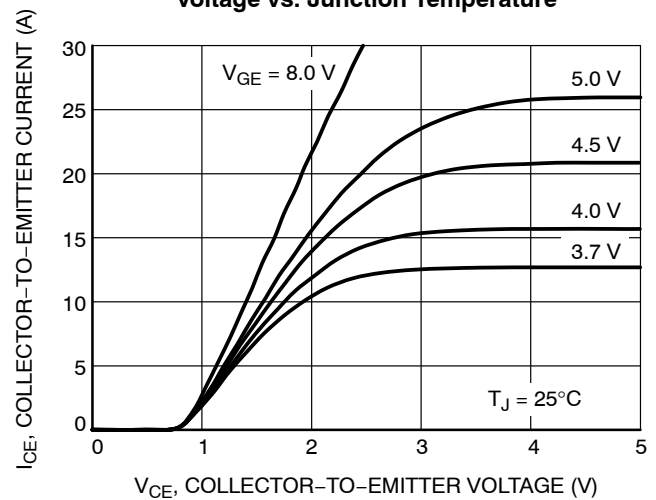


Figure 6. Collector-to-Emitter On-State Voltage vs. Collector Current

TYPICAL CHARACTERISTICS

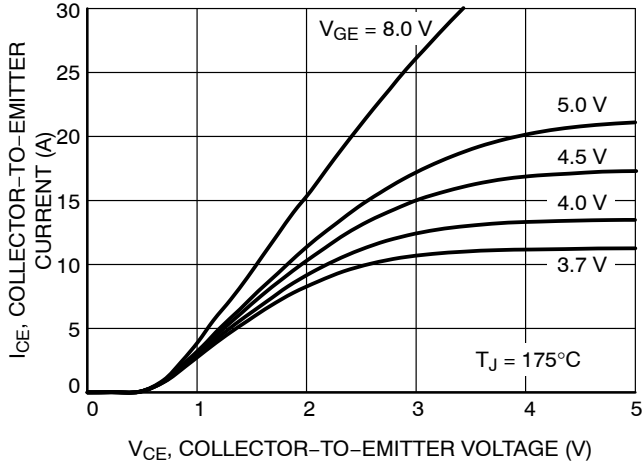


Figure 7. Collector-to-Emitter On-State Voltage vs. Collector Current

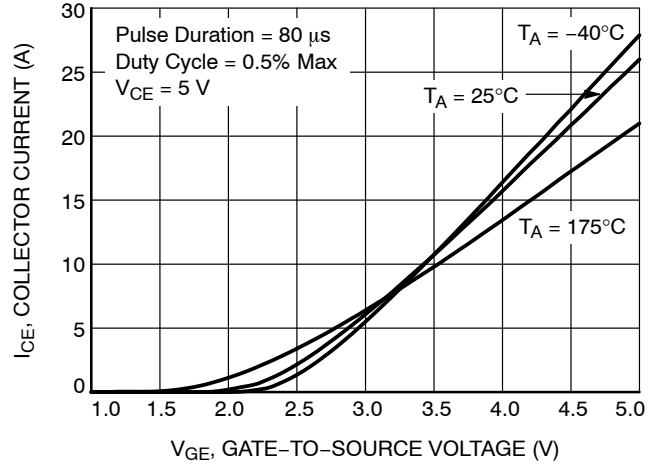


Figure 8. Transfer Characteristics

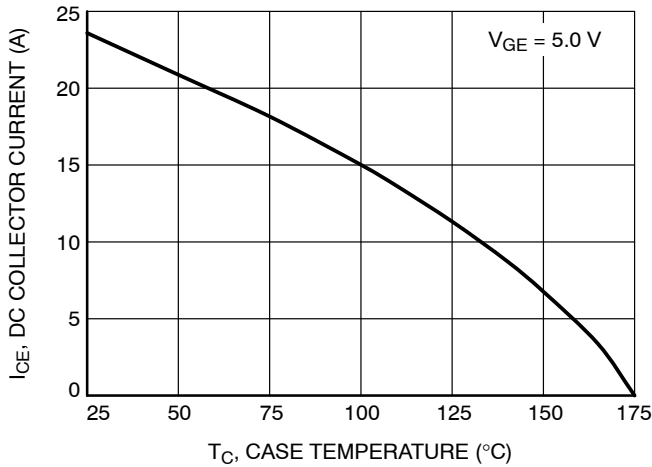


Figure 9. DC Collector Current vs. Case Temperature

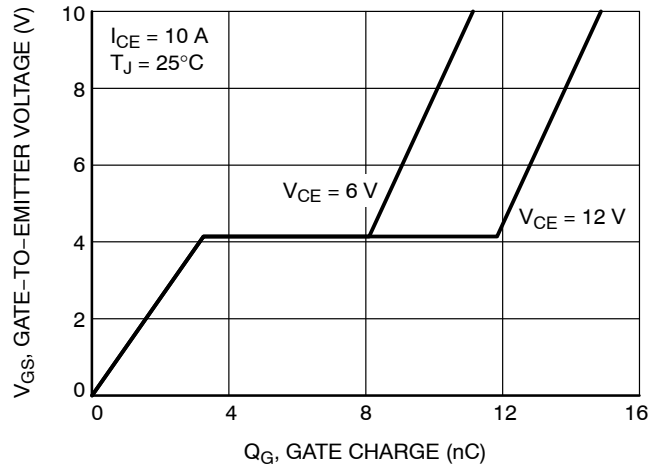


Figure 10. Gate Charge

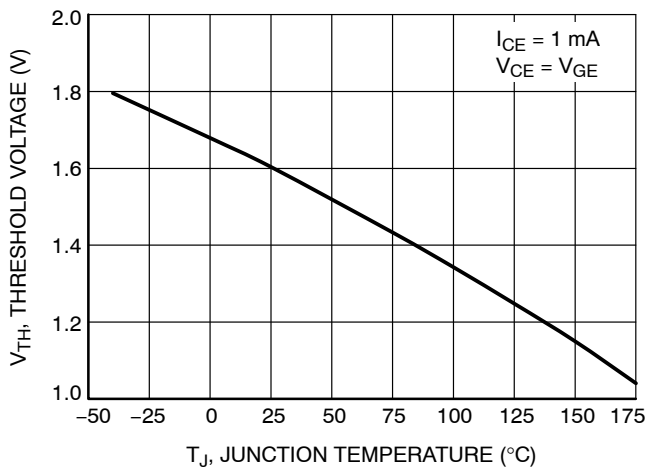


Figure 11. Threshold Voltage vs. Junction Temperature

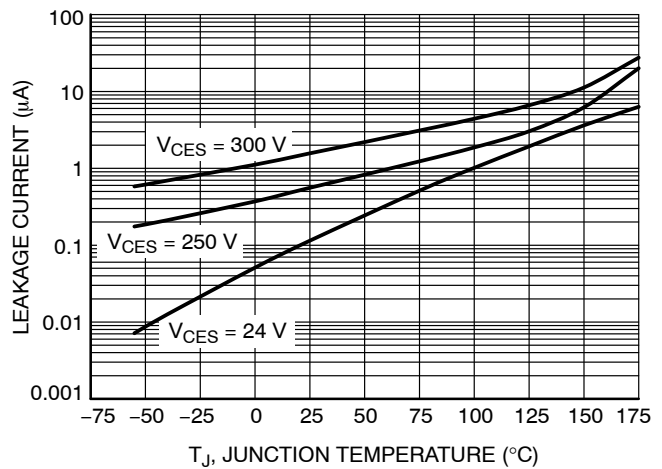


Figure 12. Leakage Current vs. Junction Temperature

TYPICAL CHARACTERISTICS

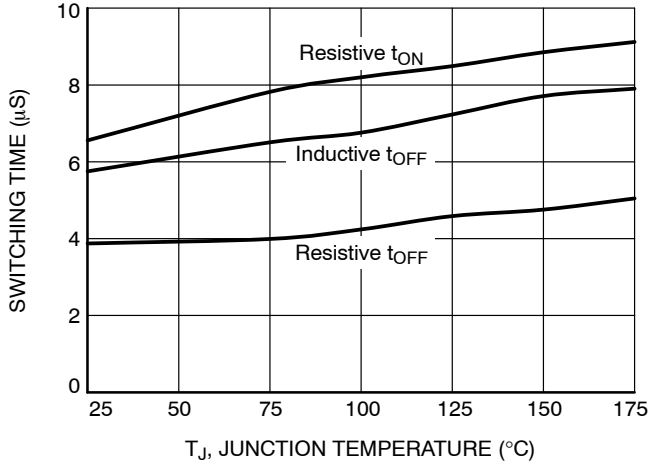


Figure 13. Switching Time vs. Junction Temperature

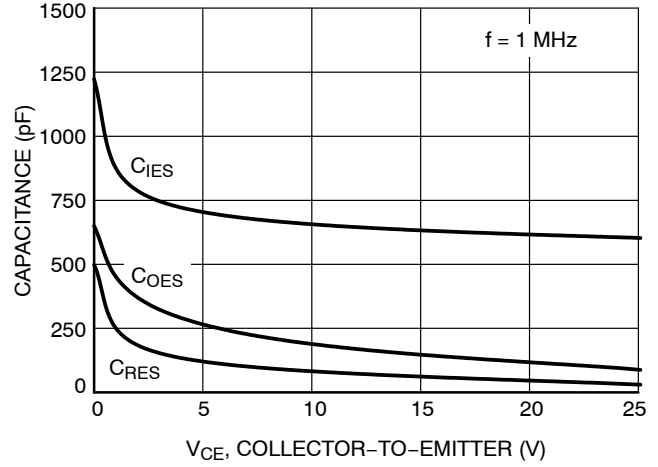


Figure 14. Capacitance vs. Collector-to-Emitter Voltage

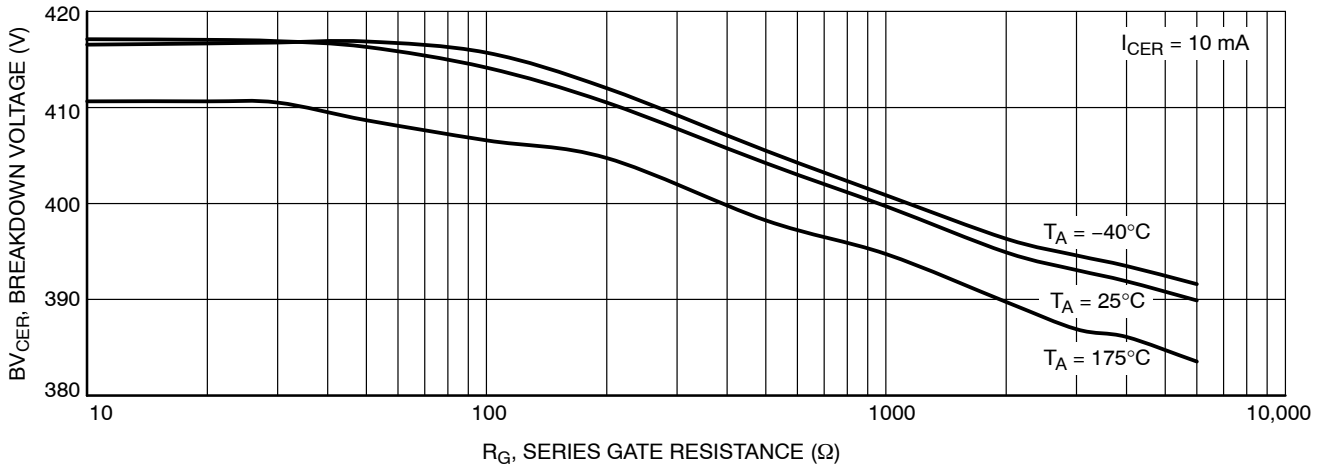


Figure 15. Break Down Voltage vs. Series Resistance

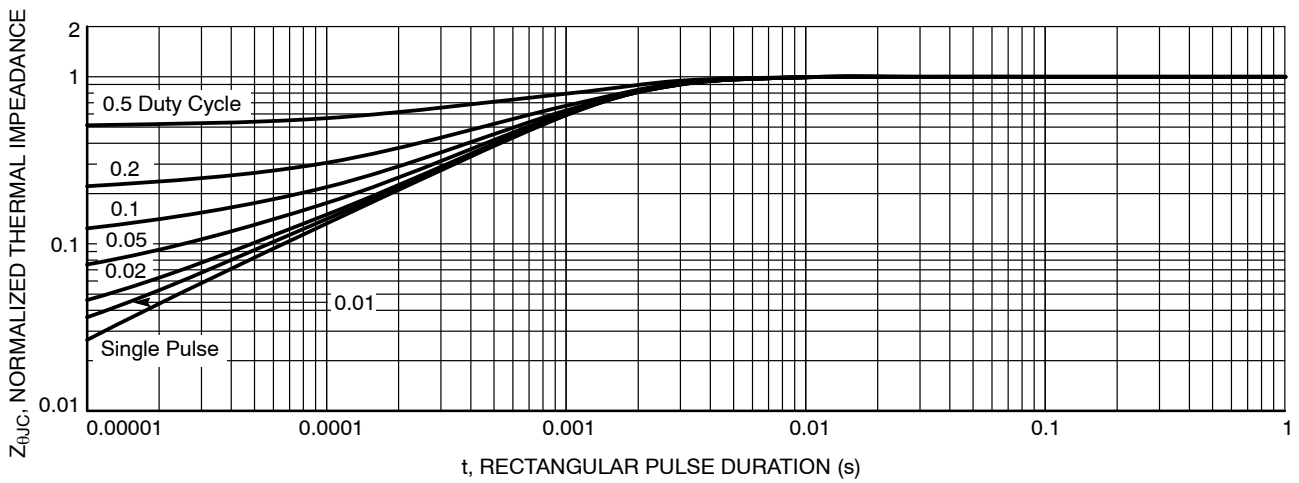


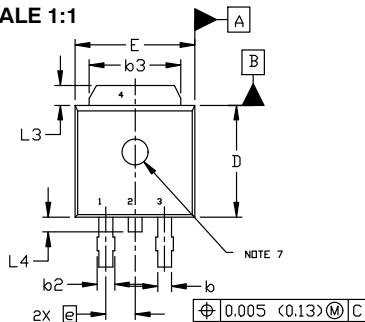
Figure 16. IGBT Normalized Transient Thermal Impedance, Junction-to-Case



DPAK (SINGLE GAUGE)
CASE 369C
ISSUE G

DATE 31 MAY 2023

SCALE 1:1



TOP VIEW



SIDE VIEW



BOTTOM VIEW



BOTTOM VIEW

ALTERNATE
CONSTRUCTIONS



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

STYLE 1:

PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:

PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:

PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:

PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:

PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:

PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:

PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:

PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:

PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:

PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

NOTES:

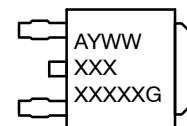
1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---

GENERIC
MARKING DIAGRAM*



IC



Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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