

# MOSFET - Power, Single N-Channel, SUPERFET<sup>®</sup>, FAST, TOLL-4L

## 600 V, 80 mΩ, 32 A

### NTBL080N60S5H

The SUPERFET V MOSFET FAST series helps maximize system efficiency by the extremely low switching losses in hard switching application. The TOLL package offers improved thermal performance and excellent switching performance by providing a Kelvin Source configuration and lower parasitic source inductance.

#### Features

- 650 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(ON)} = 64\text{ m}\Omega$
- 100% Avalanche Tested
- Pb-Free, Halogen Free / BFR Free and are RoHS Compliant

#### Applications

- Telecom / Server Power Supplies
- EV Charger / UPS / Solar / Industrial Power Supplies

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

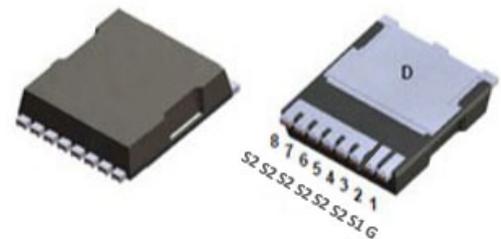
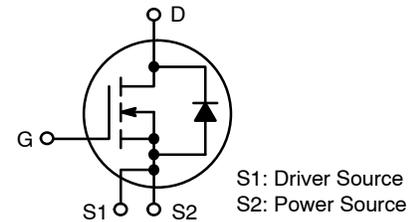
Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	600	V
Gate-to-Source Voltage	$V_{GS}$	DC	$\pm 30$
		AC ( $f > 1\text{ Hz}$ )	$\pm 30$
Continuous Drain Current	$I_D$	$T_C = 25^\circ\text{C}$	32
		$T_C = 100^\circ\text{C}$	20
Power Dissipation	$P_D$	208	W
Pulsed Drain Current (Note 1)	$T_C = 25^\circ\text{C}$	$I_{DM}$	112
Pulsed Source Current (Body Diode) (Note 1)		$I_{SM}$	112
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	32	A
Single Pulse Avalanche Energy	$I_L = 5.8\text{ A}$ $R_G = 25\ \Omega$	$E_{AS}$	287
Avalanche Current		$I_{AS}$	5.8
Repetitive Avalanche Energy (Note 1)	$E_{AR}$	2.08	mJ
MOSFET dv/dt	dv/dt	120	V/ns
Peak Diode Recovery dv/dt (Note 2)		20	
Lead Temperature for Soldering Purposes (1/8" from Case for 10 Seconds)	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating; pulse-width limited by maximum junction temperature.
2.  $I_{SD} \leq 16\text{ A}$ ,  $di/dt \leq 200\text{ A/s}$ ,  $V_{DD} \leq 400\text{ V}$ , starting  $T_J = 25^\circ\text{C}$ .

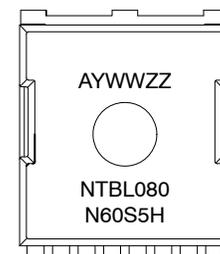
$V_{(BR)DSS}$	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
600 V	80 mΩ @ 10 V	32 A

#### N-CHANNEL MOSFET



#### H-PSOF8L CASE 100DC

#### MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Assembly Lot Code
- NTBL080N60S5H = Specific Device Code

#### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTBL080N60S5H	H-PSOF8L	2000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTBL080N60S5H

## THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.6	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	43	$^{\circ}C/W$

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^{\circ}C$ unless otherwise stated)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0 V, I_D = 1 mA, T_J = 25^{\circ}C$	600			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 10 mA$ , Referenced to $25^{\circ}C$		630		$mV/^{\circ}C$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0 V, V_{DS} = 600 V, T_J = 25^{\circ}C$			2	$\mu A$
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 30 V, V_{DS} = 0 V$			$\pm 100$	nA

### ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10 V, I_D = 16 A, T_J = 25^{\circ}C$		64	80	$m\Omega$
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 3.3 mA, T_J = 25^{\circ}C$	2.7		4.3	V
Forward Transconductance	$g_{FS}$	$V_{DS} = 20 V, I_D = 16 A$		32.8		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0 V, f = 250 KHz,$ $V_{DS} = 400 V$		3127		pF
Output Capacitance	$C_{OSS}$			46		
Time Related Output Capacitance	$C_{OSS(tr)}$	$I_D = \text{Constant}, V_{DS} = 0 \text{ to } 400 V,$ $V_{GS} = 0 V$		719		
Energy Related Output Capacitance	$C_{OSS(er)}$		$V_{GS} = 0 V, V_{DS} = 0 \text{ to } 400 V$		77.1	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10 V, V_{DD} = 400 V,$ $I_D = 16 A$		55.8		nC
Gate-to-Source Charge	$Q_{GS}$			15.1		
Gate-to-Drain Charge	$Q_{GD}$			14.6		
Gate-Resistance	$R_G$	$f = 1 MHz$		1.17		$\Omega$

### SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 0/10 V, V_{DD} = 400 V,$ $I_D = 16 A, R_G = 4.7 \Omega$		22.9		ns
Rise Time	$t_r$			6.15		
Turn-Off Delay Time	$t_{d(OFF)}$			67		
Fall Time	$t_f$			2.54		

### SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0 V, I_{SD} = 16 A, T_J = 25^{\circ}C$			1.2	V
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0 V, I_{SD} = 16 A,$ $di_S/dt = 100 A/\mu s, V_{DD} = 400 V$		383		ns
Reverse Recovery Charge	$Q_{RR}$			6092		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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# NTBL080N60S5H

## TYPICAL CHARACTERISTICS

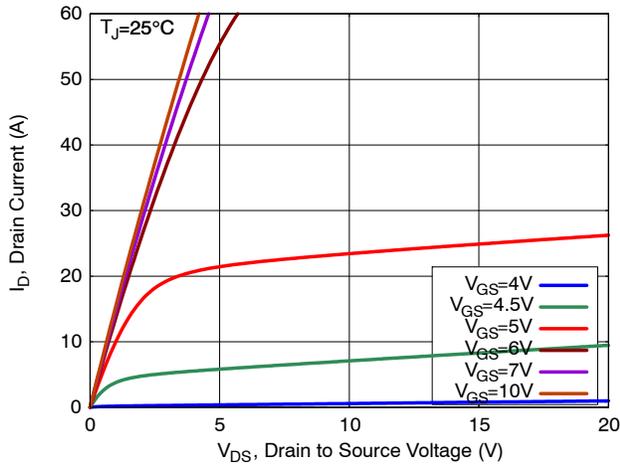


Figure 1. On-Region Characteristics

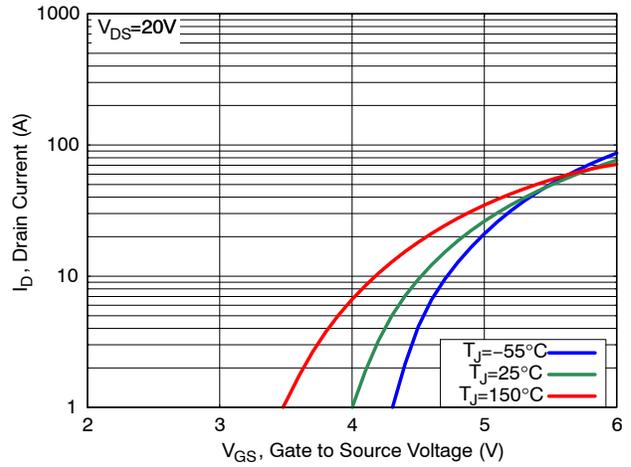


Figure 2. Transfer Characteristics

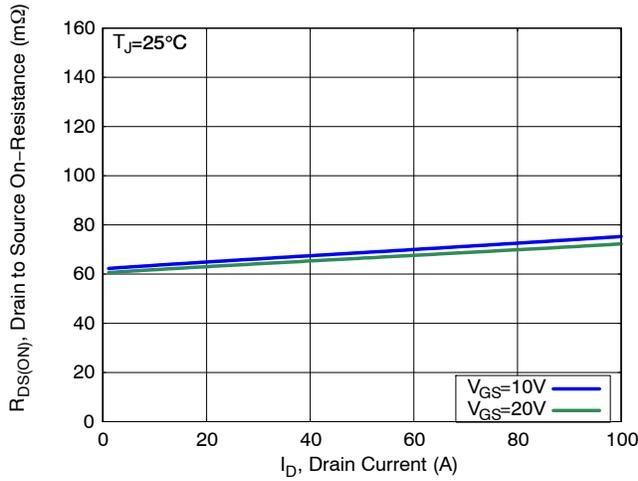


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

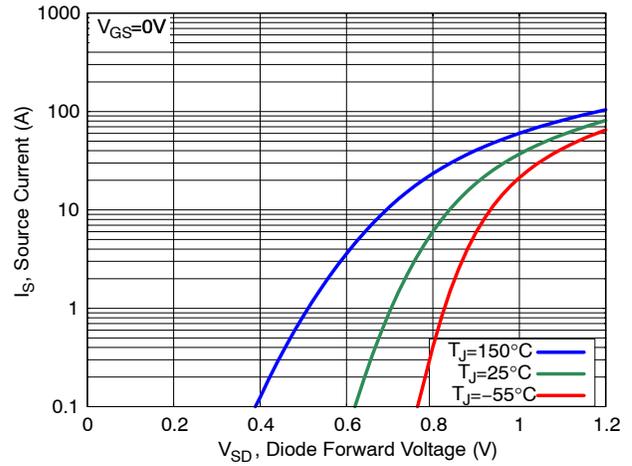


Figure 4. Diode Forward Voltage vs. Source Current

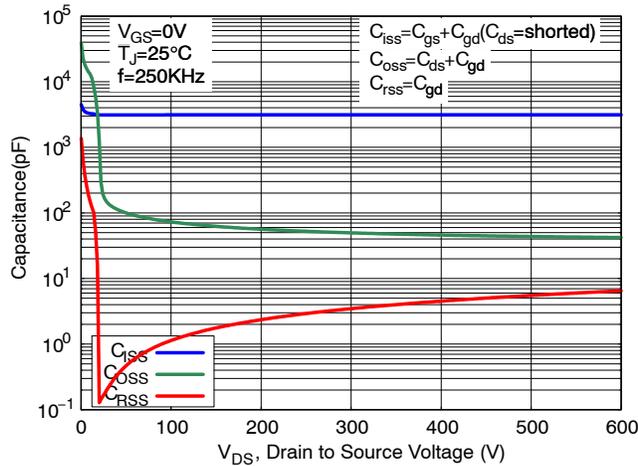


Figure 5. Capacitance Characteristics

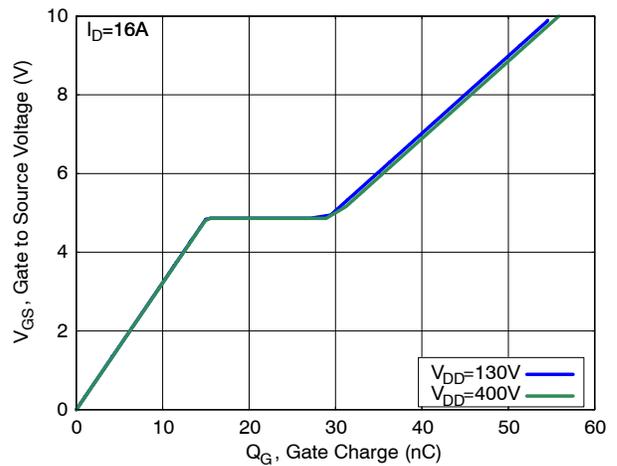
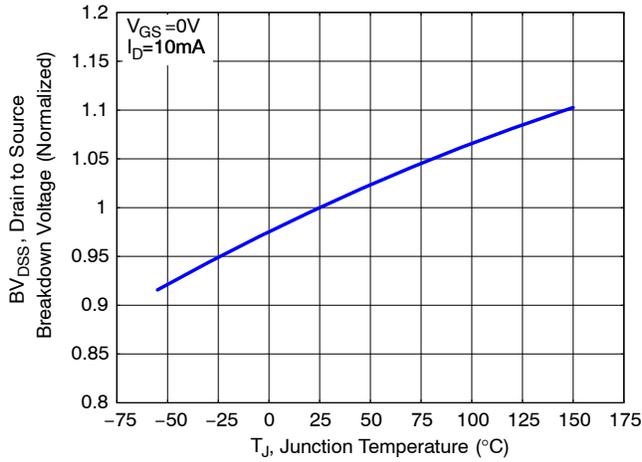


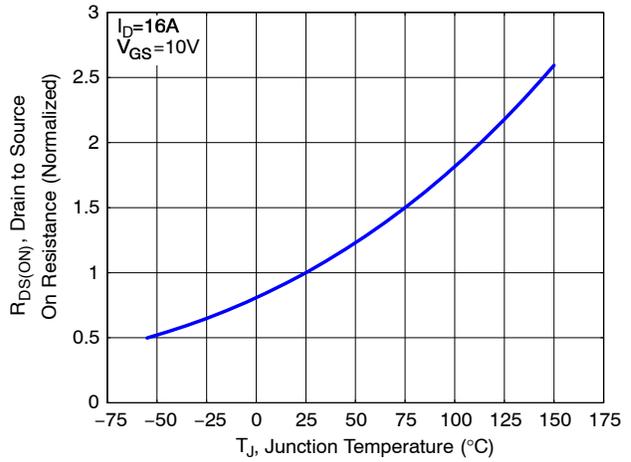
Figure 6. Gate Charge Characteristics

# NTBL080N60S5H

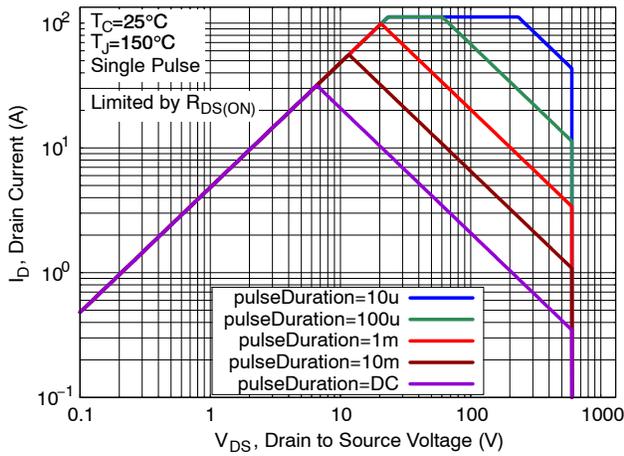
## TYPICAL CHARACTERISTICS



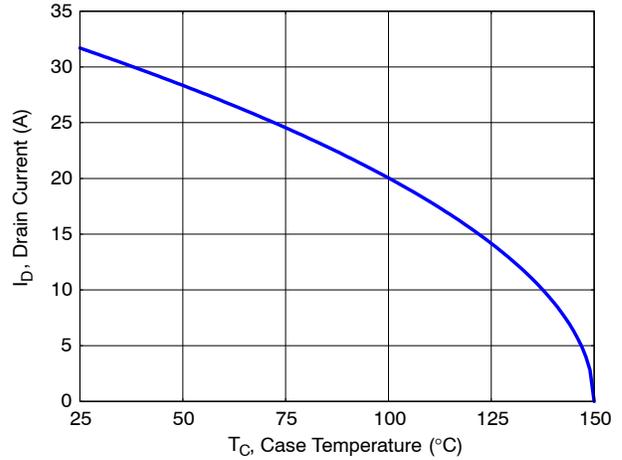
**Figure 7. Breakdown Voltage Variation vs. Temperature**



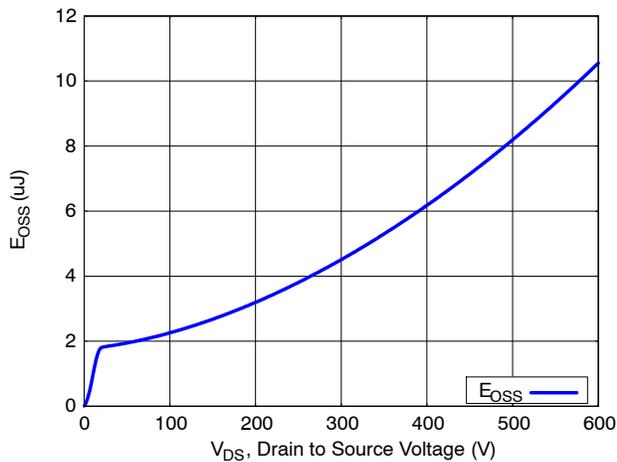
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Eoss vs. Drain-to-Source Voltage**

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## TYPICAL CHARACTERISTICS

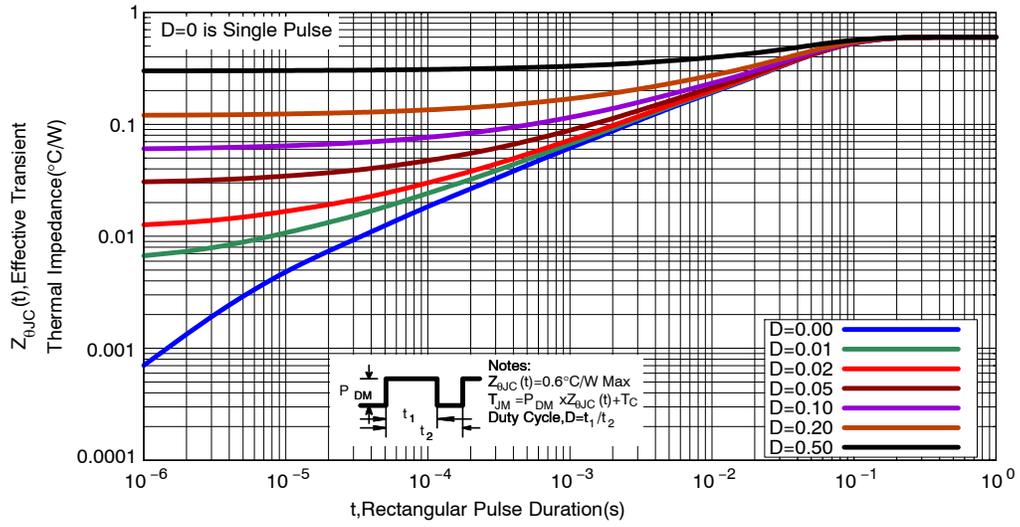
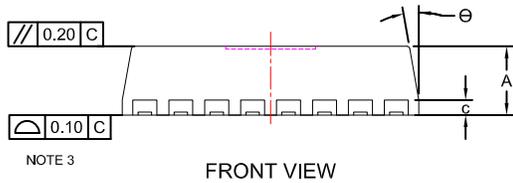
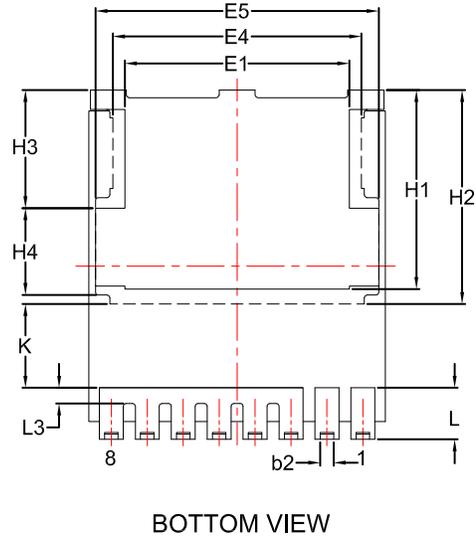
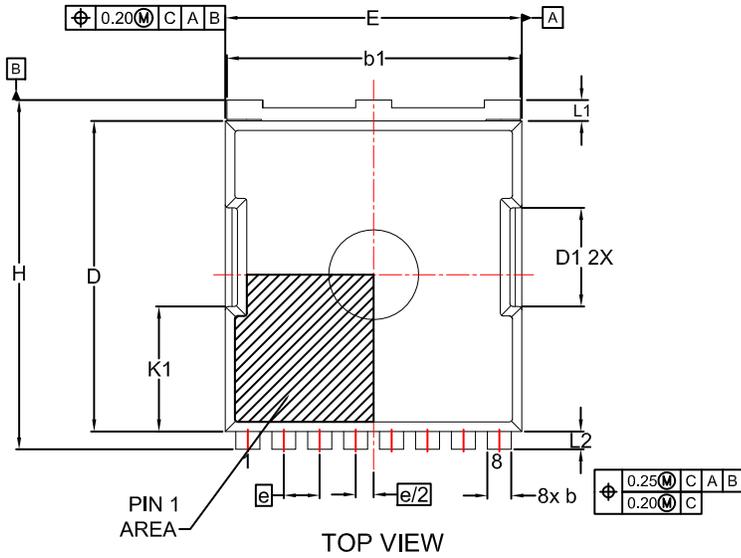


Figure 12. Transient Thermal Impedance

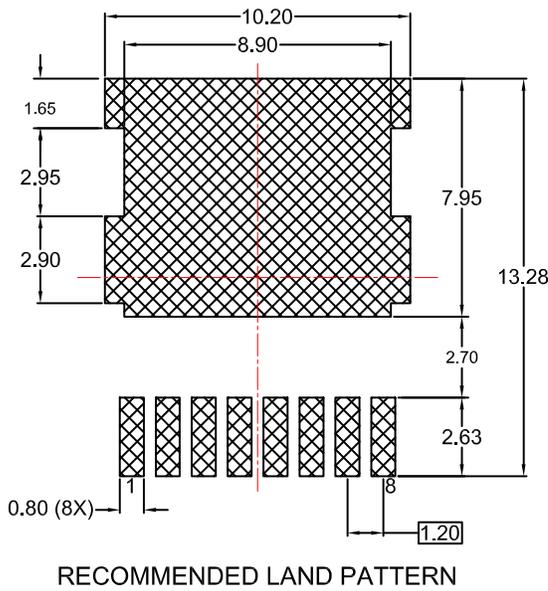
# NTBL080N60S5H

## PACKAGE DIMENSIONS

H-PSOF8L 9.90x11.68, 1.20P  
CASE 100DC  
ISSUE O



NOTE 3



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.36	0.46	0.56
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D1	3.30		
E	9.80	9.90	10.80
E1	7.40	7.50	7.60
E4	8.30		
E5	9.49		
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H1	6.55	6.65	6.75
H2	7.05	7.15	7.25
H3	3.60		
H4	3.26		
K	2.70	2.80	2.90
K1	4.18		
L	1.63	1.73	1.83
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	1.10	1.20	1.30
θ	10° REF.		

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