

MOSFET - Power, Single N-Channel, SUPERFET[®], FAST, TOLL-4L

600 V, 100 mΩ, 27 A

NTBL100N60S5H

Description

The SUPERFET V MOSFET FAST series helps maximize system efficiency by the extremely low switching losses in hard switching application. The TOLL package offers improved thermal performance and excellent switching performance by providing a Kelvin Source configuration and lower parasitic source inductance.

Features

- 650 V @ $T_J = 150^\circ\text{C}$ / Typ. $R_{DS(on)} = 80\text{ m}\Omega$
- 100% Avalanche Tested
- Pb-Free, Halogen Free / BFR Free and RoHS Compliant

Applications

- Telecom / Server Power Supplies
- EV Charger / UPS / Solar / Industrial Power Supplies

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

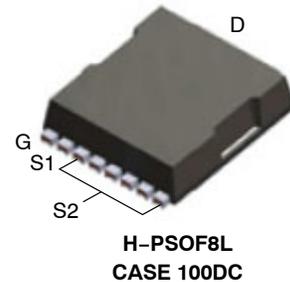
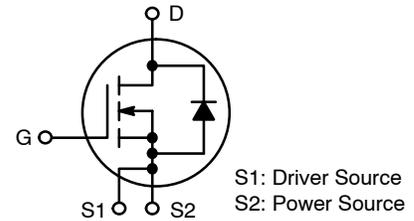
Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	600	V
Gate-to-Source Voltage	V_{GS}	DC	± 30
		AC ($f > 1\text{ Hz}$)	± 30
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	27
		$T_C = 100^\circ\text{C}$	17
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	179
Pulsed Drain Current (Note 1)	$T_C = 25^\circ\text{C}$	I_{DM}	95
Pulsed Source Current (Body Diode) (Note 1)		I_{SM}	95
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)	I_S	27	A
Single Pulse Avalanche Energy	$I_L = 5.1\text{ A}$ $R_G = 25\ \Omega$	E_{AS}	230
Avalanche Current	I_{AS}	5.1	A
Repetitive Avalanche Energy (Note 1)	E_{AR}	1.79	mJ
MOSFET dv/dt	dv/dt	120	V/ns
Peak Diode Recovery dv/dt (Note 2)		20	
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

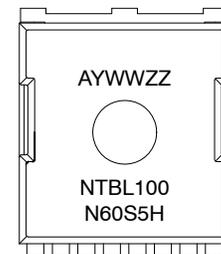
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $I_{SD} \leq 13.5\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq 400\text{ V}$, starting $T_J = 25^\circ\text{C}$.

$V_{(BR)DSS}$	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
600 V	100 mΩ @ $V_{GS} = 10\text{ V}$	27 A

N-CHANNEL MOSFET



MARKING DIAGRAM



- A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
NTBL100N60S5H = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NTBL100N60S5H	H-PSOF8L	2000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	43	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	600	–	–	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 10\text{ mA}$, Referenced to 25°C	–	630	–	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}, T_J = 25^\circ\text{C}$	–	–	1	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	–	–	± 100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 13.5\text{ A}, T_J = 25^\circ\text{C}$	–	80	100	m Ω
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 2.7\text{ mA}, T_J = 25^\circ\text{C}$	2.7	–	4.3	V
Forward Trans-conductance	g_{FS}	$V_{DS} = 20\text{ V}, I_D = 13.5\text{ A}$	–	27.3	–	S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 250\text{ kHz}$	–	2616	–	pF
Output Capacitance	C_{OSS}		–	39	–	
Time Related Output Capacitance	$C_{OSS(tr)}$	$I_D = \text{Constant}, V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	–	609	–	pF
Energy Related Output Capacitance	$C_{OSS(er)}$	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	–	65.5	–	pF
Total Gate Charge	$Q_{G(tot)}$	$V_{DD} = 400\text{ V}, I_D = 13.5\text{ A}, V_{GS} = 10\text{ V}$	–	46.5	–	nC
Gate-to-Source Charge	Q_{GS}		–	12.7	–	
Gate-to-Drain Charge	Q_{GD}		–	12	–	
Gate Resistance	R_G		$f = 1\text{ MHz}$	–	1.16	

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 0/10\text{ V}, V_{DD} = 400\text{ V}, I_D = 13.5\text{ A}, R_G = 4.7\text{ }\Omega$	–	20.8	–	ns
Rise Time	t_r		–	5.35	–	
Turn-Off Delay Time	$t_{d(OFF)}$		–	60	–	
Fall Time	t_f		–	2.61	–	

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_{SD} = 13.5\text{ A}, T_J = 25^\circ\text{C}$	–	–	1.2	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, I_{SD} = 13.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 400\text{ V}$	–	362	–	ns
Reverse Recovery Charge	Q_{RR}		–	5323	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL CHARACTERISTICS

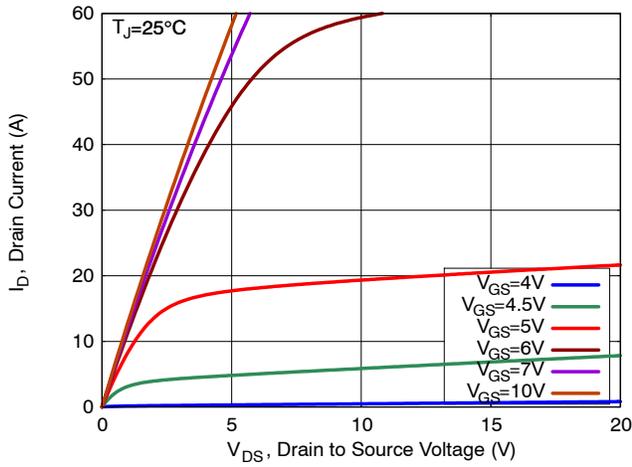


Figure 1. On-Region Characteristics

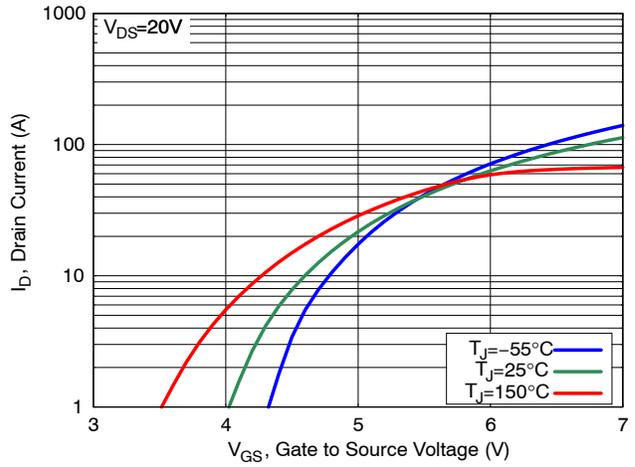


Figure 2. Transfer Characteristics

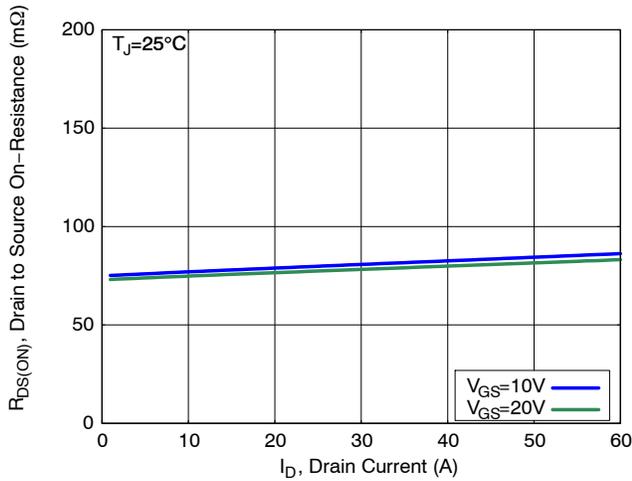


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

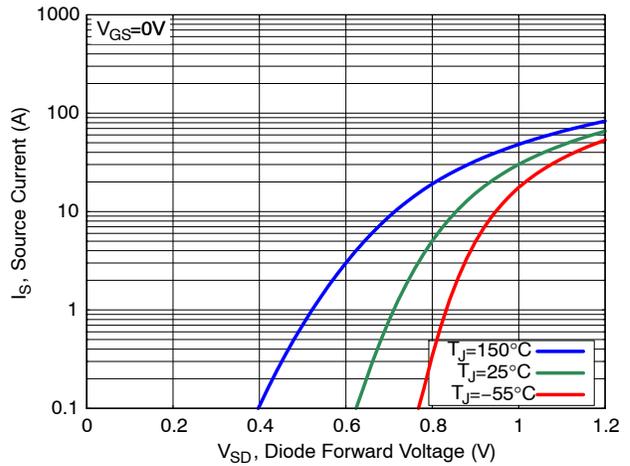


Figure 4. Diode Forward Voltage vs. Source Current

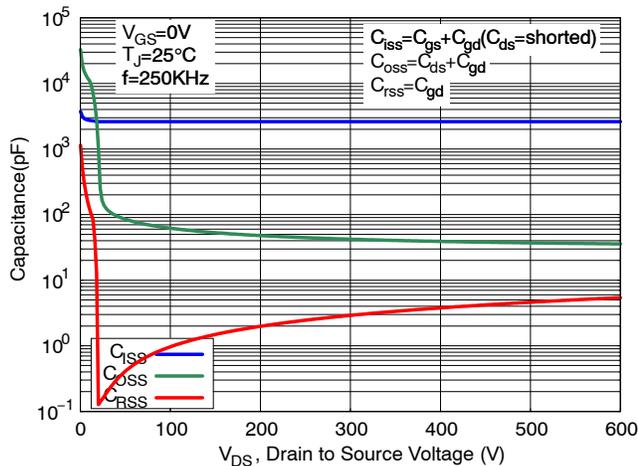


Figure 5. Capacitance Characteristics

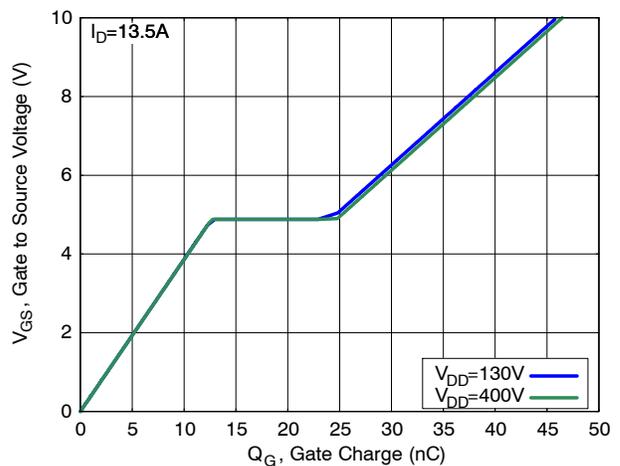


Figure 6. Gate Charge Characteristics

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TYPICAL CHARACTERISTICS

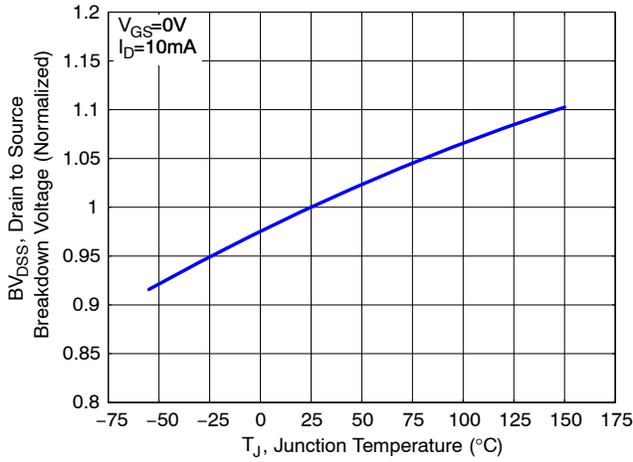


Figure 7. Breakdown Voltage Variation vs. Temperature

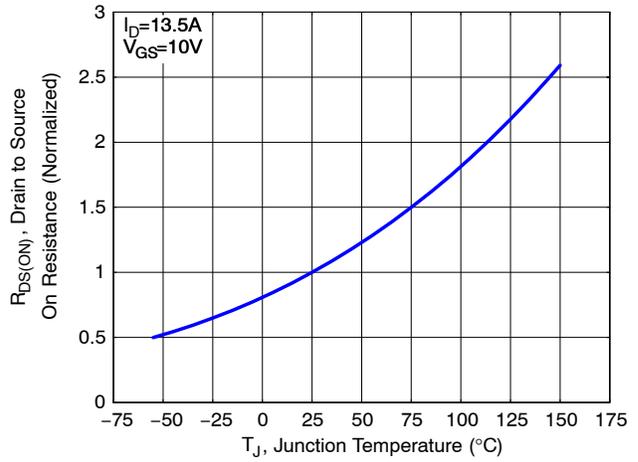


Figure 8. On-Resistance Variation vs. Temperature

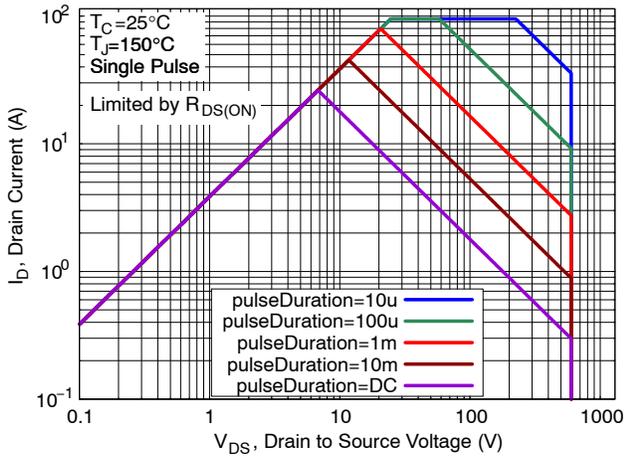


Figure 9. Maximum Safe Operating Area

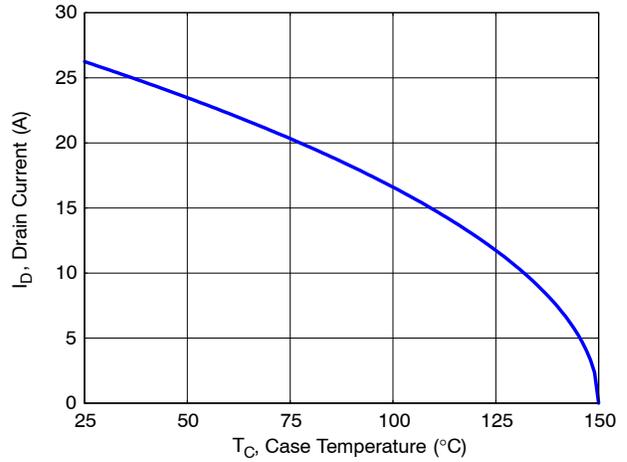


Figure 10. Maximum Drain Current vs. Case Temperature

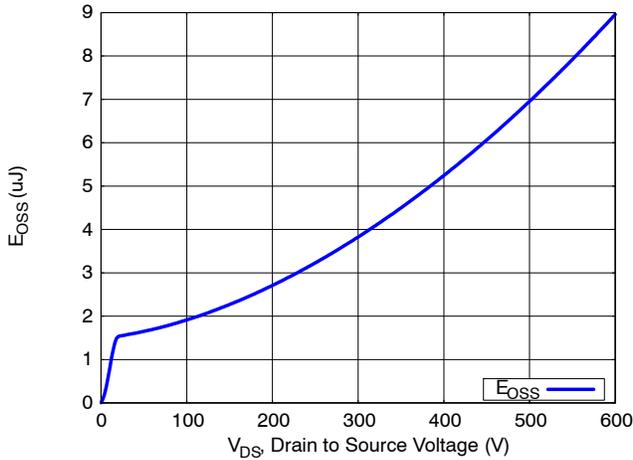


Figure 11. Eoss vs. Drain-to-Source Voltage

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TYPICAL CHARACTERISTICS

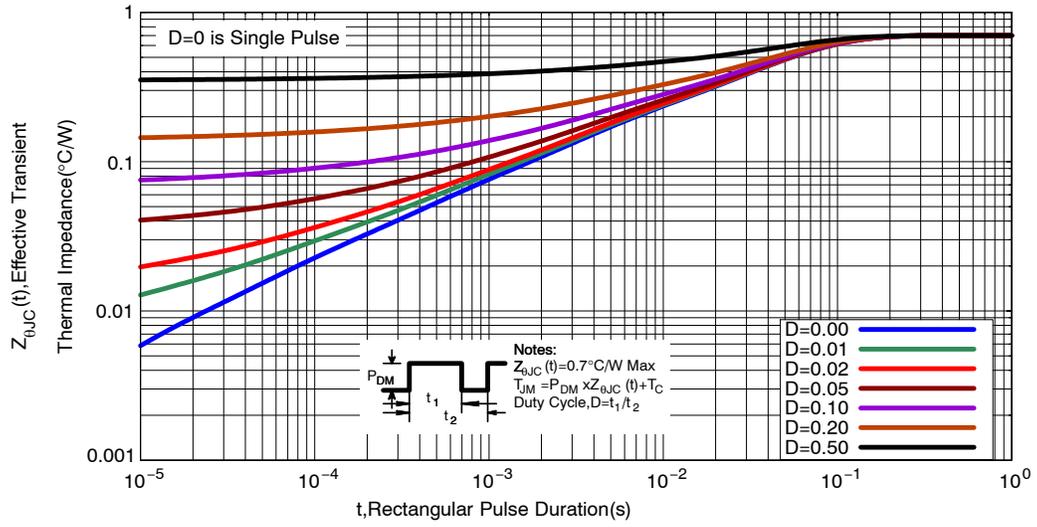
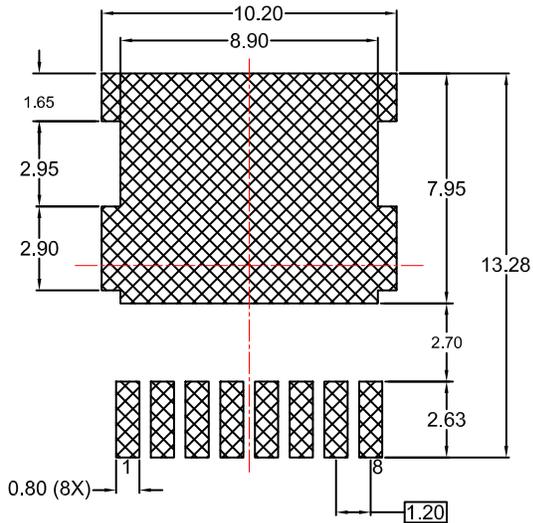
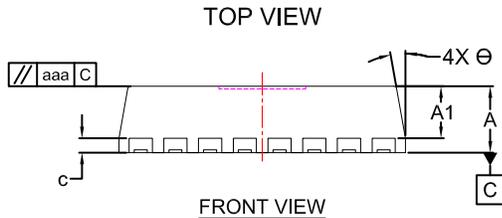
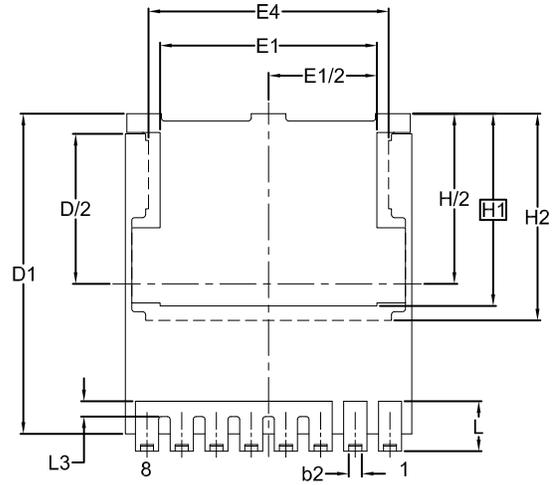
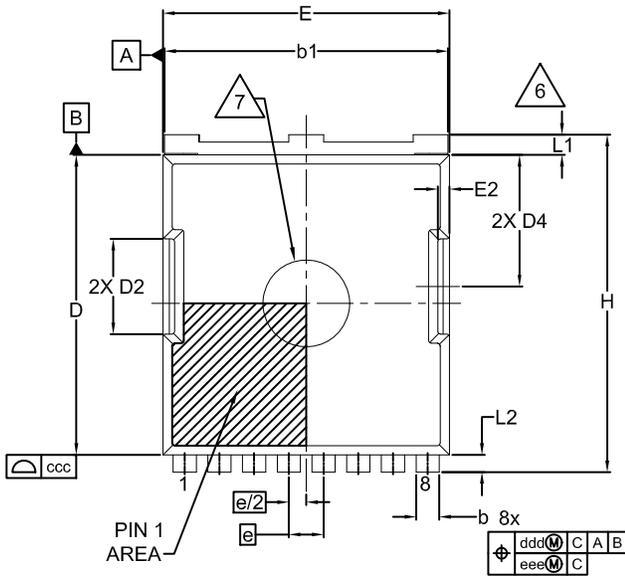


Figure 12. Transient Thermal Impedance

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PACKAGE DIMENSIONS

H-PSOF8L 9.90x11.68, 1.20P
CASE 100DC
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLEMMETERS.
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D/2	5.09	5.19	5.29
D4	4.45	4.55	4.65
E	9.80	9.90	10.00
E1	7.40	7.50	7.60
E2	0.30	0.40	0.50
E4	8.20	8.30	8.40
e	1.20 BSC		
H	11.58	11.68	11.78
H1	6.66 BSC		
H2	7.05	7.15	7.25
H/2	5.79	5.89	5.99
L	1.63	1.73	1.83
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.43	0.53	0.63
Ø	10° REF.		
aaa	0.20		
ccc	0.20		
ddd	0.25		
eee	0.20		

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