MOSFET - Power, Single N-Channel, SUPERFET®, FAST, TOLL-4L

600 V, 125 mΩ, 22 A

NTBL125N60S5H

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
600 V	125 mΩ @ V_{GS}= 10 V	22 A

Description

The SUPERFET V MOSFET FAST series helps maximize system efficiency by the extremely low switching losses in hard switching application. The TOLL package offers improved thermal performance and excellent switching performance by providing a Kelvin Source configuration and lower parasitic source inductance.

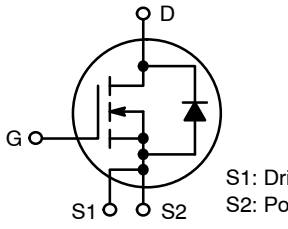
Features

- 650 V @ T_J = 150°C / Typ. $R_{DS(on)}$ = 100 mΩ
- 100% Avalanche Tested
- Pb−Free, Halogen Free / BFR Free and RoHS Compliant

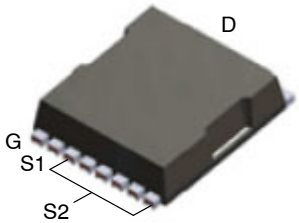
Applications

- Telecom / Server Power Supplies
- EV Charger / UPS / Solar / Industrial Power Supplies

N−CHANNEL MOSFET



S1: Driver Source
S2: Power Source



H−PSOF8L
CASE 100DC

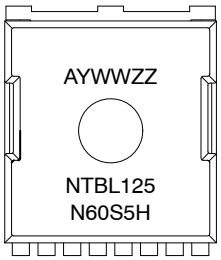
MAXIMUM RATINGS (T_J = 25°C, unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DSS}	600	V
Gate−to−Source Voltage	DC	V_{GS}	±30	V
	AC (f > 1 Hz)		±30	
Continuous Drain Current	T_C = 25°C	I_D	22	A
	T_C = 100°C		13	
Power Dissipation	T_C = 25°C	P_D	152	W
Pulsed Drain Current (Note 1)	T_C = 25°C	I_{DM}	77	A
Pulsed Source Current (Body Diode) (Note 1)		I_{SM}	77	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode)		I_S	22	A
Single Pulse Avalanche Energy	I_L = 4.5 A, R_G = 25 Ω	E_{AS}	184	mJ
Avalanche Current		I_{AS}	4.5	A
Repetitive Avalanche Energy (Note 1)		E_{AR}	1.52	mJ
MOSFET dv/dt		dv/dt	120	V/ns
Peak Diode Recovery dv/dt (Note 2)			20	
Lead Temperature for Soldering Purposes (1/8″ from case for 10 seconds)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. I_{SD} ≤ 11 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

MARKING DIAGRAM



A	= Assembly Location
Y	= Year
WW	= Work Week
ZZ	= Assembly Lot Code
NTBL125N60S5H	= Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NTBL125N60S5H	H−PSOF8L	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.82	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	43	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 mA, T_J = 25°C	600	–	–	V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 10 mA, Referenced to 25°C	–	630	–	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 600 V, T_J = 25°C	–	–	1	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 11 A, T_J = 25°C	–	100	125	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2.1 mA, T_J = 25°C	2.7	–	4.3	V
Forward Trans−conductance	g_{FS}	V_{DS} = 20 V, I_D = 11 A	–	21.7	–	S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{DS} = 400 V, V_{GS} = 0 V, f = 250 kHz	–	2036	–	pF
Output Capacitance	C_{OSS}		–	31.2	–	
Time Related Output Capacitance	$C_{OSS(tr.)}$	I_D = Constant, V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	485	–	
Energy Related Output Capacitance	$C_{OSS(er.)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	52.2	–	
Total Gate Charge	$Q_{G(tot)}$	V_{DD} = 400 V, I_D = 11 A, V_{GS} = 10 V	–	37.1	–	nC
Gate−to−Source Charge	Q_{GS}		–	9.92	–	
Gate−to−Drain Charge	Q_{GD}		–	10.2	–	
Gate Resistance	R_G	f = 1 MHz	–	1.08	–	Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(ON)}$	V_{GS} = 0/10 V, V_{DD} = 400 V, I_D = 11 A, R_G = 7.5 Ω	–	18.5	–	ns
Rise Time	t_r		–	5.15	–	
Turn-Off Delay Time	$t_{d(OFF)}$		–	56.4	–	
Fall Time	t_f		–	2.7	–	
SOURCE−TO−DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_{SD} = 11 A, T_J = 25°C	–	–	1.2	V
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_{SD} = 11 A, dI/dt = 100 A/μs, V_{DD} = 400 V	–	336	–	ns
Reverse Recovery Charge	Q_{RR}		–	4513	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

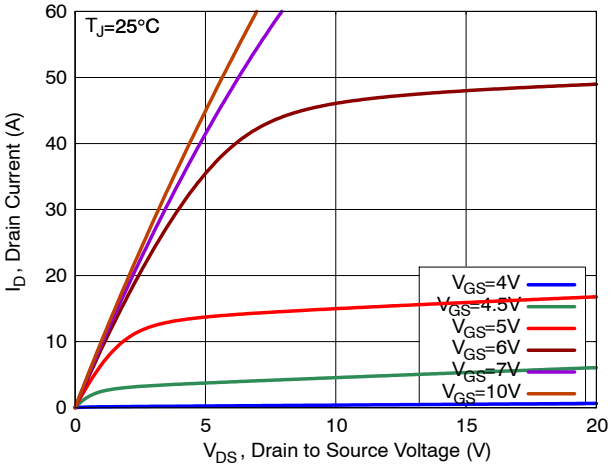


Figure 1. On−Region Characteristics

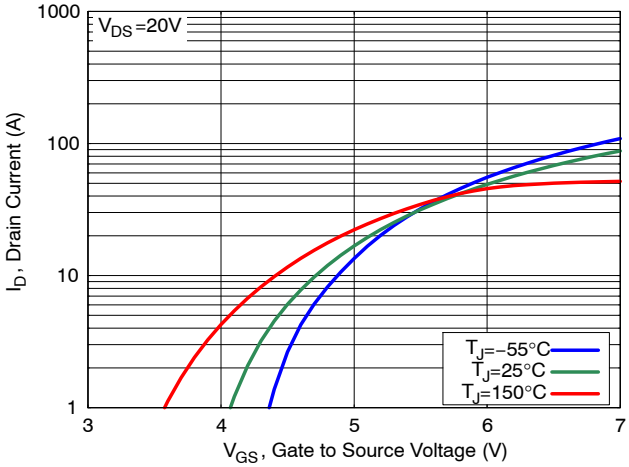


Figure 2. Transfer Characteristics

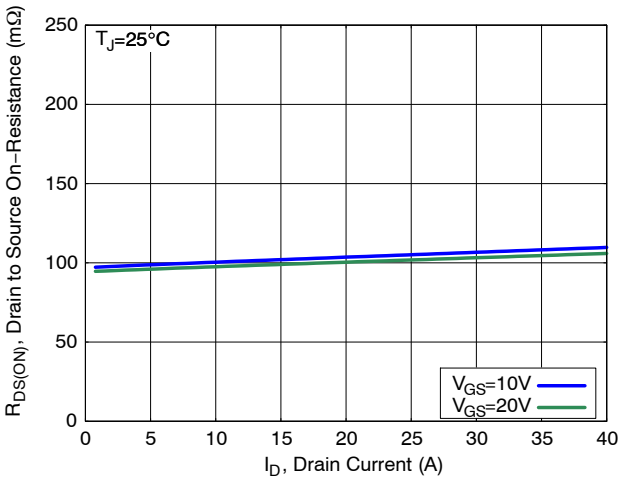


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

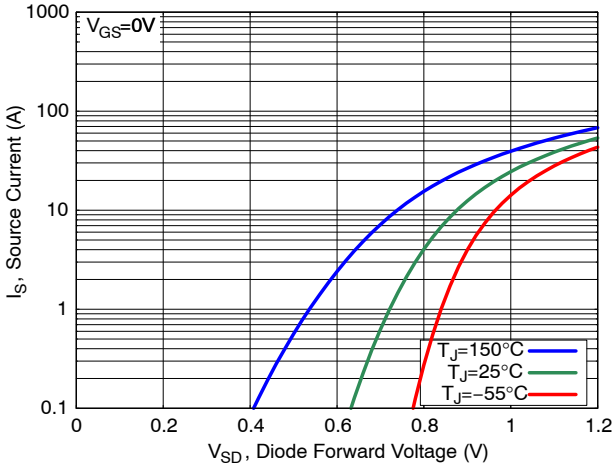


Figure 4. Diode Forward Voltage vs. Source Current

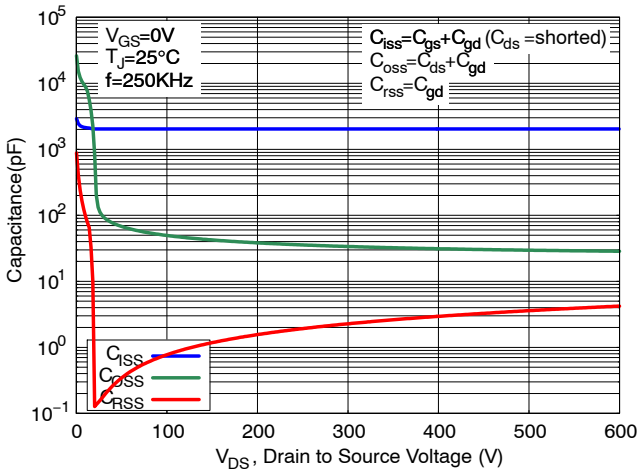


Figure 5. Capacitance Characteristics

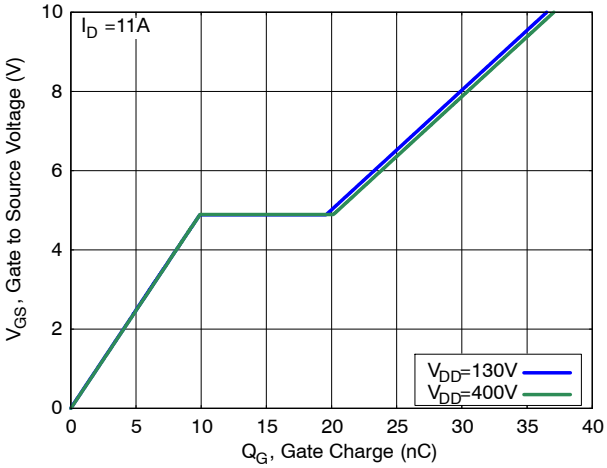


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

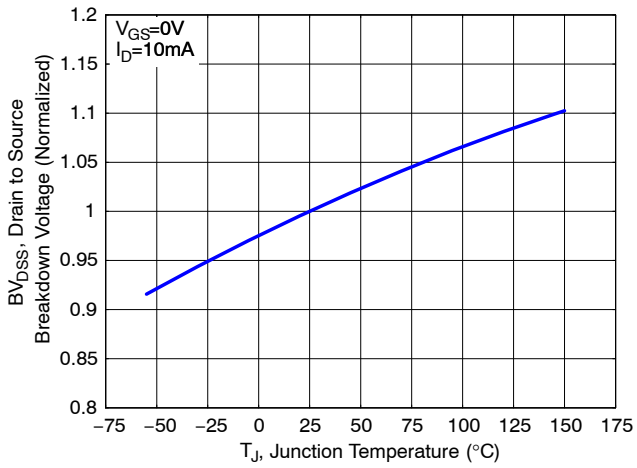


Figure 7. Breakdown Voltage Variation vs. Temperature

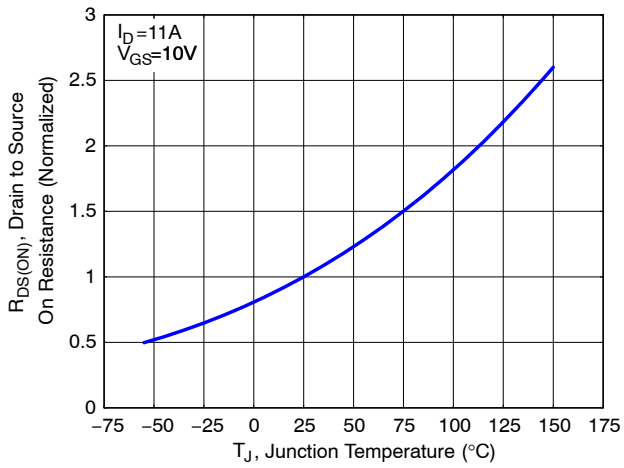


Figure 8. On−Resistance Variation vs. Temperature

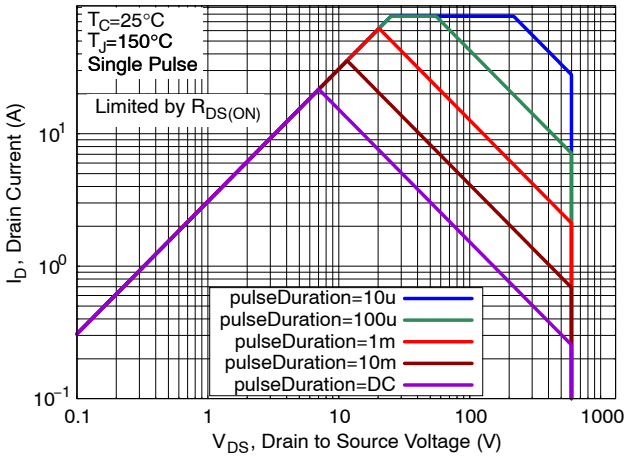


Figure 9. Maximum Safe Operating Area

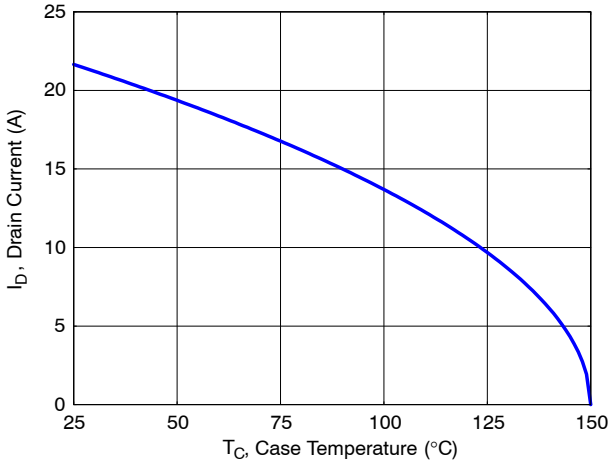


Figure 10. Maximum Drain Current vs. Case Temperature

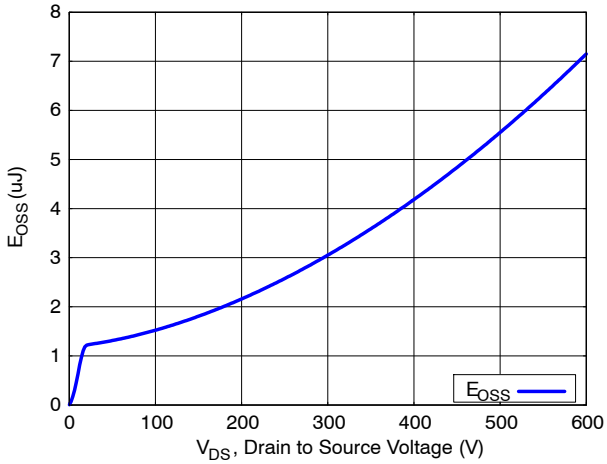


Figure 11. Eoss vs. Drain−to−Source Voltage

TYPICAL CHARACTERISTICS

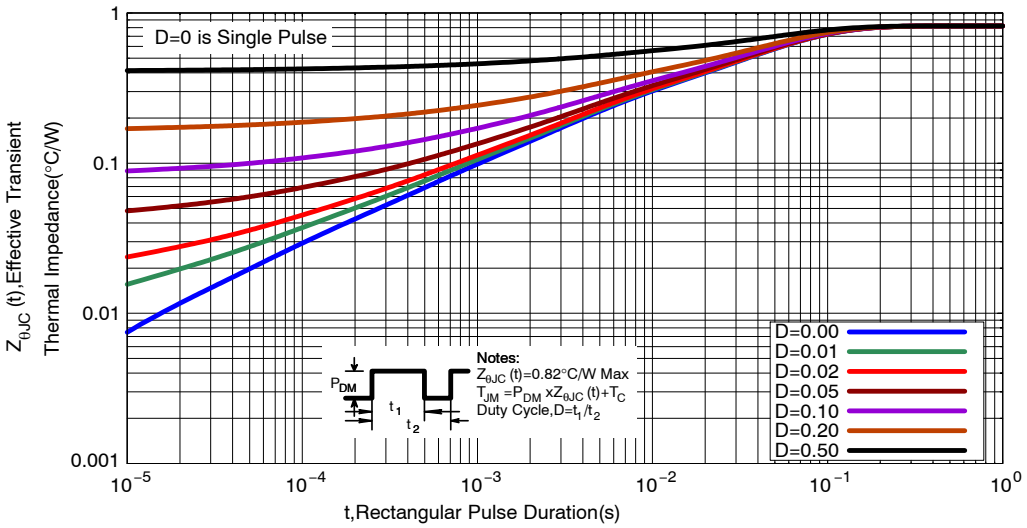
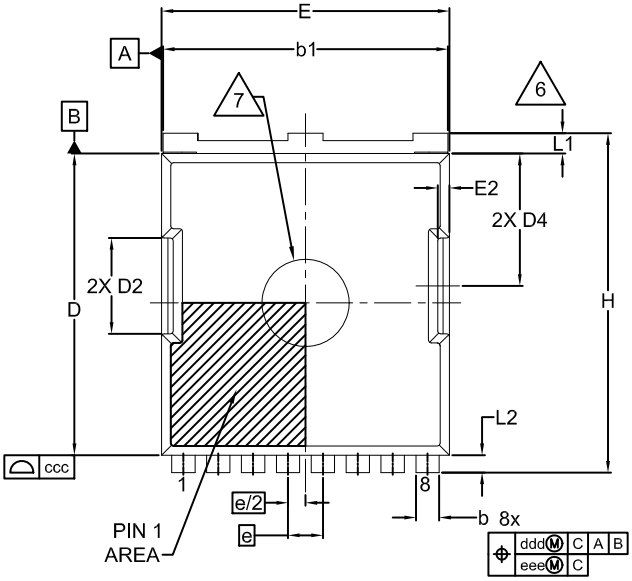


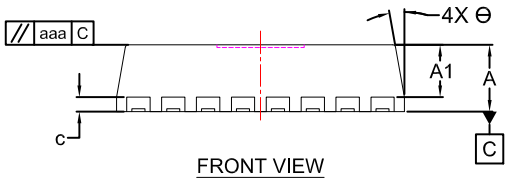
Figure 12. Transient Thermal Impedance

PACKAGE DIMENSIONS

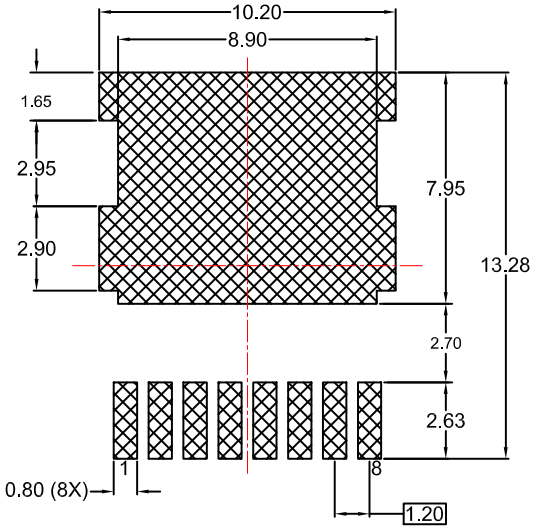
H−PSOF8L 9.90x11.68, 1.20P
CASE 100DC
ISSUE O



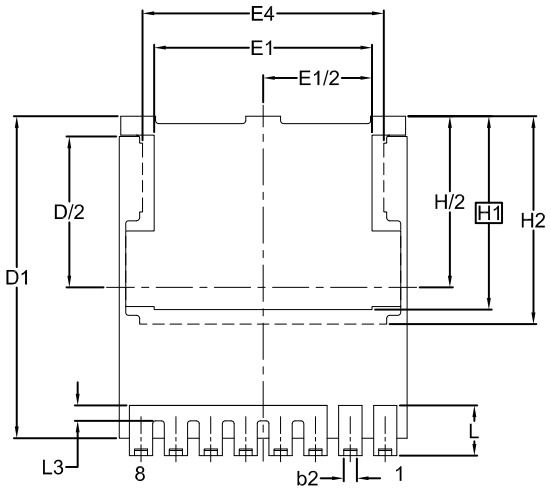
TOP VIEW



FRONT VIEW



RECOMMENDED LAND PATTERN



BOTTOM VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D/2	5.09	5.19	5.29
D4	4.45	4.55	4.65
E	9.80	9.90	10.00
E1	7.40	7.50	7.60
E2	0.30	0.40	0.50
E4	8.20	8.30	8.40
e	1.20 BSC		
H	11.58	11.68	11.78
H1	6.66 BSC		
H2	7.05	7.15	7.25
H/2	5.79	5.89	5.99
L	1.63	1.73	1.83
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.43	0.53	0.63
Θ	10° REF.		
aaa	0.20		
ccc	0.20		
ddd	0.25		
eee	0.20		

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLEMETERS.
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

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