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MOSFET - Power, Single P-Channel, SO8-FL -30 V, 1.8 mΩ, -234 A



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NTMFS003P03P8Z

Features

- Ultra Low $R_{DS(on)}$ to Improve System Efficiency
- Advanced Package Technology in 5x6mm for Space Saving and Excellent Thermal Conduction
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Load Switch
- Protection: Reverse Current, Over Voltage, and Reverse Negative Voltage
- Battery Management

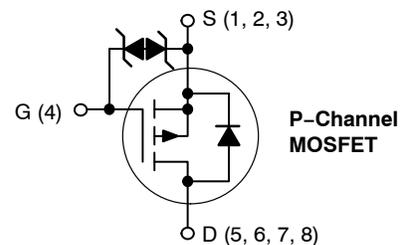
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	-30	V
Gate-to-Source Voltage		V_{GS}	± 25	V
Continuous Drain Current $R_{\theta JC}$ (Note 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D	-234
		$T_C = 85^\circ\text{C}$		-169
		$T_C = 25^\circ\text{C}$	P_D	139
Power Dissipation $R_{\theta JA}$ (Note 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D	-35.7
		$T_A = 85^\circ\text{C}$		-25.7
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)	Steady State	$T_A = 25^\circ\text{C}$	P_D	3.2
		$T_A = 25^\circ\text{C}$		
Continuous Drain Current $R_{\theta JA}$ (Notes 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D	-19.1
		$T_A = 85^\circ\text{C}$		-13.8
Power Dissipation $R_{\theta JA}$ (Notes 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	P_D	0.9
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	-604	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{Lpk} = 58.04 \text{ A}$)		E_{AS}	168.4	mJ
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$

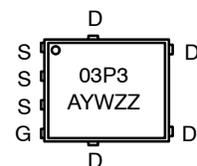
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using a 1 in² pad size, 2 oz. Cu pad.
2. Surface-mounted on FR4 board using a minimum pad size, 2 oz. Cu pad.
3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
-30 V	1.8 mΩ @ -10 V	-234 A
	2.9 mΩ @ -4.5 V	



MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS003P03P8ZT1G	SO8-FL (Pb-Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Drain) (Note 1)	$R_{\theta JC}$	0.9	$^{\circ}C/W$
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	39	$^{\circ}C/W$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	135	$^{\circ}C/W$

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0 V, I_D = -250 \mu A$	-30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250 \mu A, \text{ref to } 25^{\circ}C$		-5		$mV/^{\circ}C$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0 V, V_{DS} = -24 V, T_J = 25^{\circ}C$			-1.0	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 25 V$			± 10	μA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250 \mu A$	-1.0		-3.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = -250 \mu A, \text{ref to } 25^{\circ}C$		5.5		$mV/^{\circ}C$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -10 V, I_D = -23 A$		1.2	1.8	$m\Omega$
		$V_{GS} = -4.5 V, I_D = -20 A$		1.9	2.9	
Forward Transconductance	g_{FS}	$V_{DS} = -5 V, I_D = -20 A$		110		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{iss}	$V_{GS} = 0 V, V_{DS} = -15 V, f = 1.0 \text{ MHz}$		12120		pF
Output Capacitance	C_{oss}			4020		
Reverse Transfer Capacitance	C_{rss}			4100		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5 V, V_{DS} = -15 V, I_D = -23 A$		167		nC
Threshold Gate Charge	$Q_{G(TH)}$			7		
Gate-to-Source Charge	Q_{GS}			21		
Gate-to-Drain Charge	Q_{GD}			116		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -10 V, V_{DS} = -15 V, I_D = -23 A$		277		

SWITCHING CHARACTERISTICS, $V_{GS} = 4.5 V$ (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -4.5 V, V_{DS} = -15 V, I_D = -23 A, R_G = 6 \Omega$		81		ns
Rise Time	t_r			440		
Turn-Off Delay Time	$t_{d(off)}$			180		
Fall Time	t_f			400		

SWITCHING CHARACTERISTICS, $V_{GS} = 10 V$ (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -10 V, V_{DS} = -15 V, I_D = -23 A, R_G = 6 \Omega$		28		ns
Rise Time	t_r			116		
Turn-Off Delay Time	$t_{d(off)}$			325		
Fall Time	t_f			380		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0 V, I_S = -23 A$	$T_J = 25^{\circ}C$		-0.75	-1.3	V
			$T_J = 125^{\circ}C$		-0.6		

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = -23 A		70		ns
Charge Time	t _a			43		
Discharge Time	t _b			28		
Reverse Recovery Charge	Q _{RR}			116		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

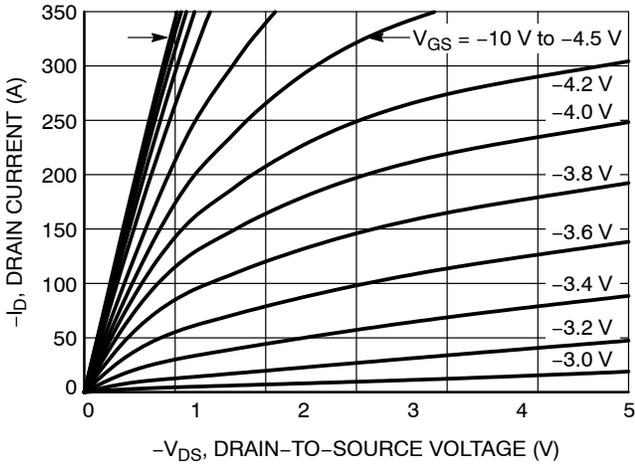


Figure 1. On-Region Characteristics

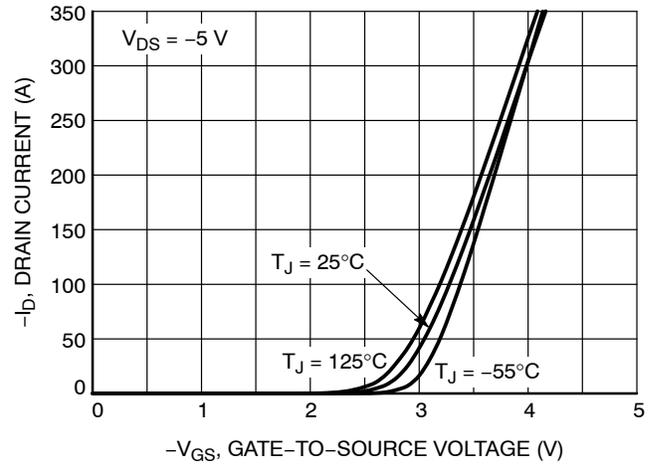


Figure 2. Transfer Characteristics

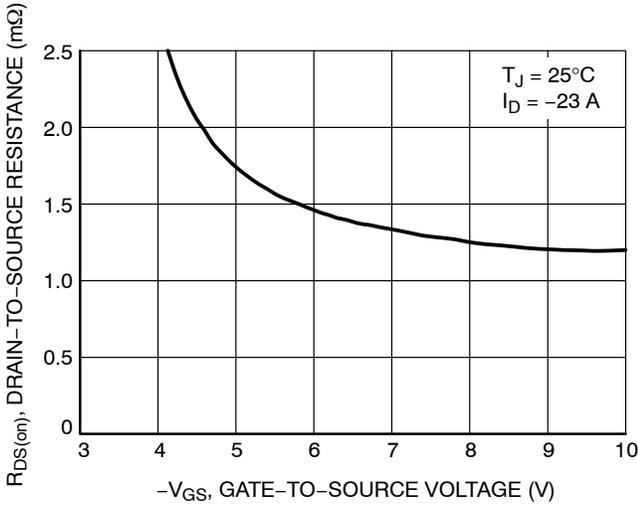


Figure 3. On-Resistance vs. Gate-to-Source Voltage

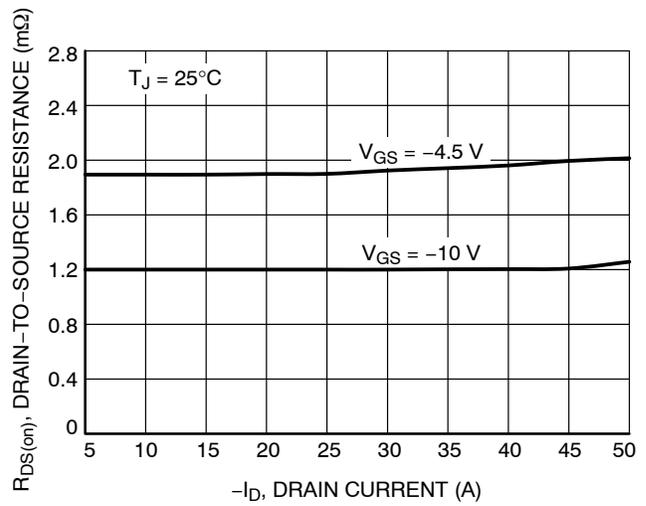


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

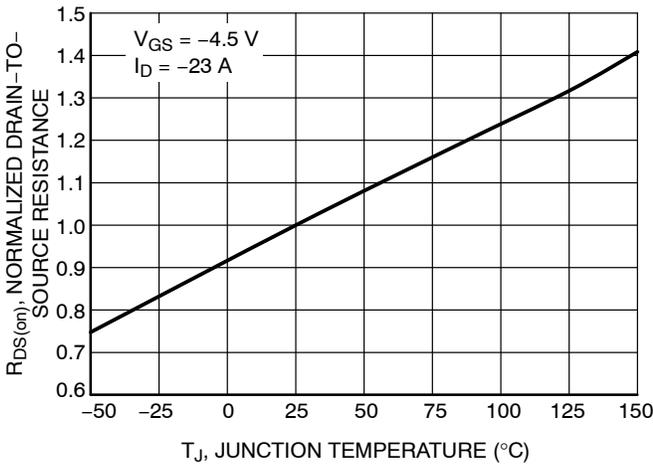


Figure 5. On-Resistance Variation with Temperature

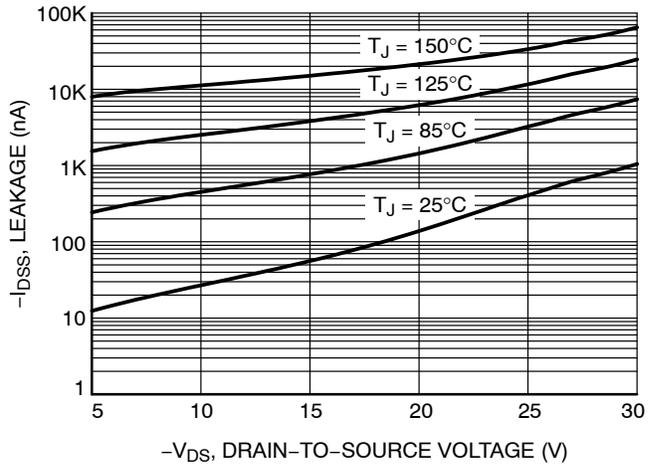


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

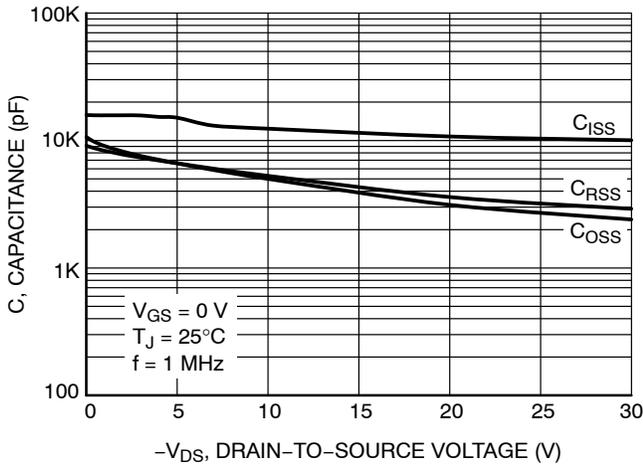


Figure 7. Capacitance Variation

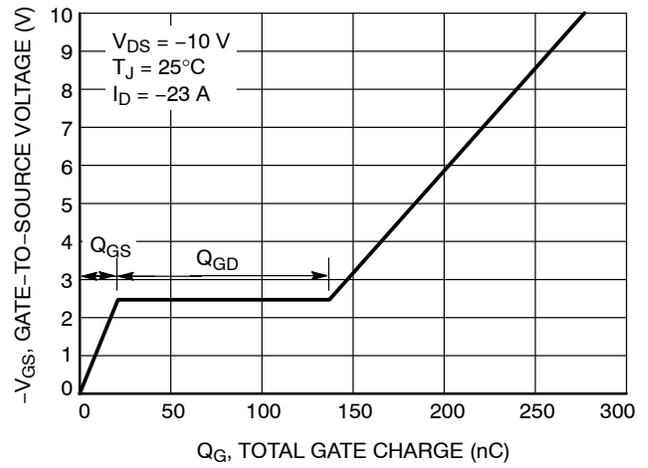


Figure 8. Gate-to-Source Voltage vs. Total Charge

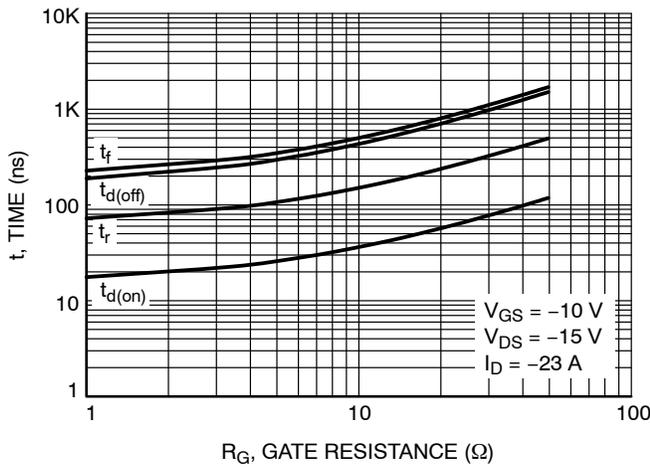


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

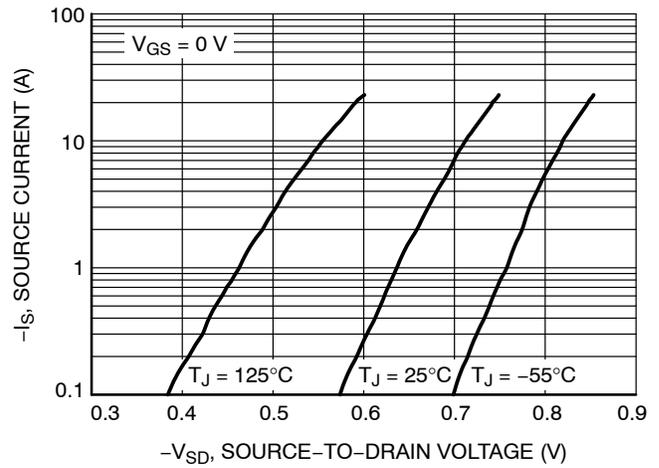


Figure 10. Diode Forward Voltage vs. Current

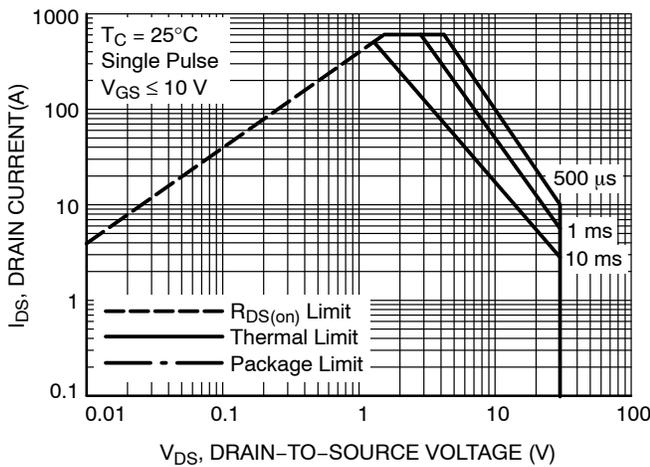


Figure 11. Maximum Rated Forward Biased Safe Operating Area

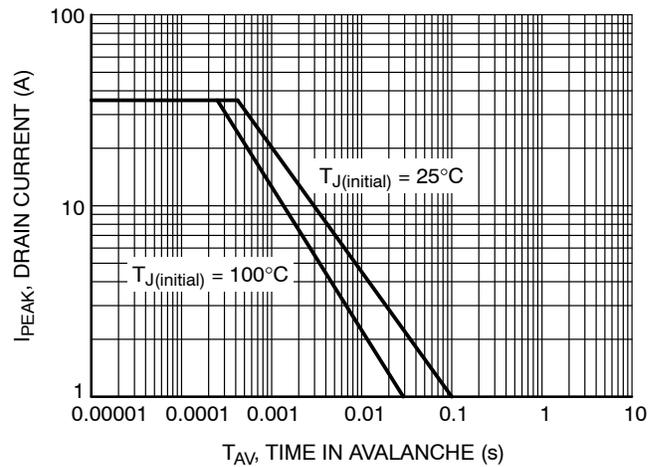


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

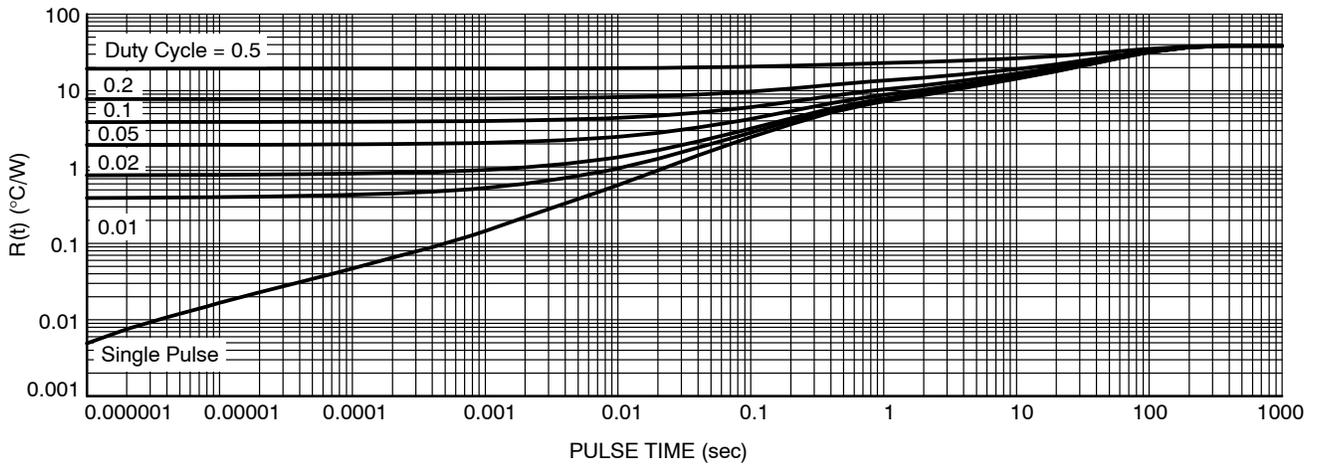


Figure 13. Thermal Characteristics

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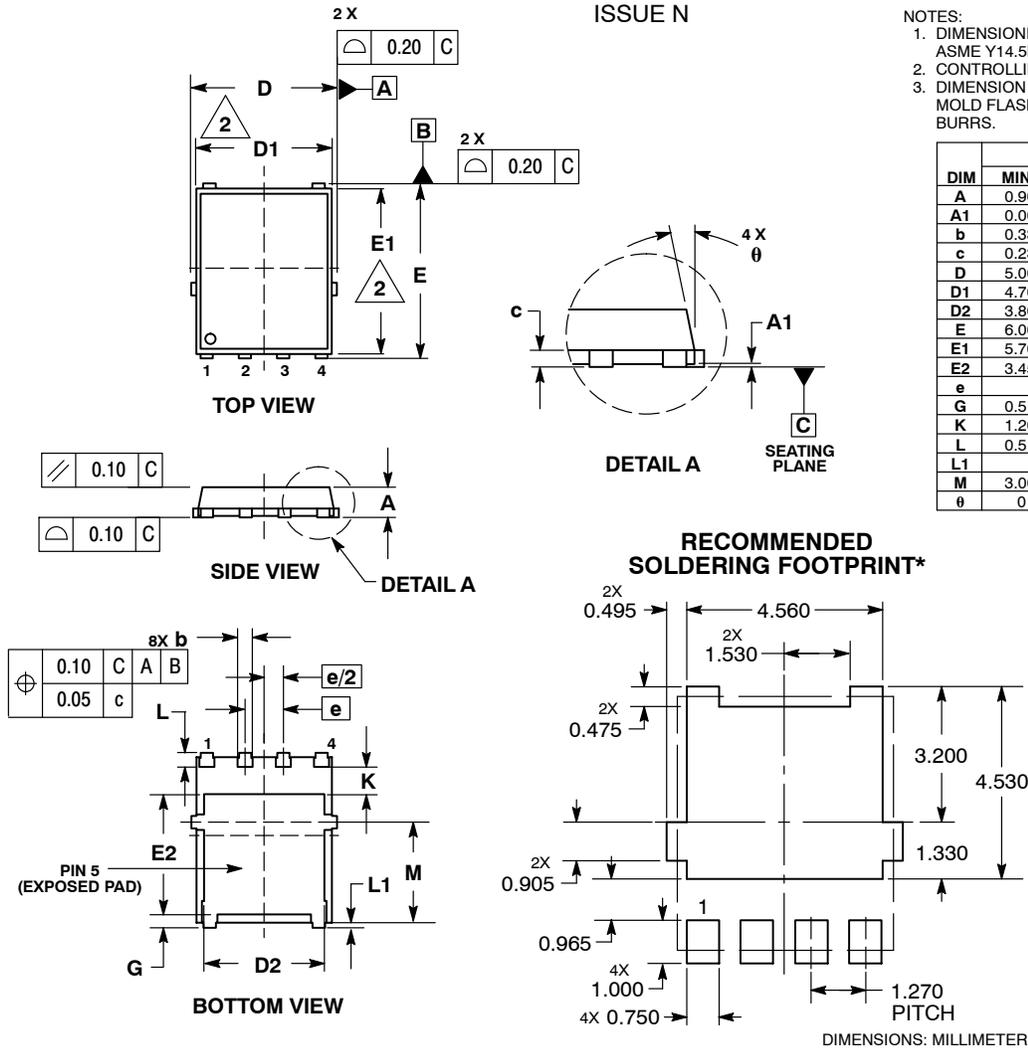
PACKAGE DIMENSIONS

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



- STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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