

MOSFET - Power, Single N-Channel, STD Gate, DUAL COOL® DFN8 5x6 60 V, 1.5 mΩ, 238 A

Product Preview

NTMFSC1D6N06C

Features

- Advanced Dual-sided Cooled Packaging
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

- Synchronous Rectifier
- DC-DC Conversion
- Oring FET and Load Switching

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	60	V
Gate-to-Source Voltage	e		V _{GS}	±20	V
Continuous Drain		T _C = 25°C	I _D	238	Α
Current $R_{\theta JC}$ (Notes 1, 3)	Steady	T _C = 100°C	1	168	
Power Dissipation	State	T _C = 25°C	P_{D}	170	W
R _{θJC} (Note 1)		T _C = 100°C		84	
Continuous Drain		T _A = 25°C	I _D	35	Α
Current R _{θJA} (Notes 1, 2, 3)	Steady	T _A = 100°C	1	25	
Power Dissipation	State	T _A = 25°C	P_{D}	3.8	W
R _{θJA} (Notes 1, 2)		T _A = 100°C		1.9	
Pulsed Drain Current	T _A = 25	°C, t _p = 10 μs	I _{DM}	900	Α
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +175	°C
Source Current (Body Diode)			Is	190	Α
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 17 A)			E _{AS}	451	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

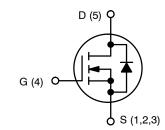
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface–mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
- Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

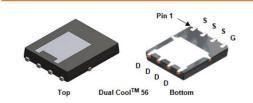
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This document contains information on a product under development. **onsemi** reserves the right to change or discontinue this product without notice.

V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
60 V	1.5 mΩ @ 10 V	238 A

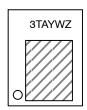


N-CHANNEL MOSFET



DFN8 5x6 CASE TBD

MARKING DIAGRAM



3T = Specific Device Code

A = Assembly Location

Y = Year

W = Work Week

Z = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Bottom)	$R_{ heta JC}$	0.9	°C/W
Thermal Resistance, Junction-to-Case (Top)	$R_{ heta JC}$	1.4	
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	39	

ELECTRICAL CHARACTERISTICS (T_{.1} = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
OFF CHARACTERISTICS	•			<u>.</u>		
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu A$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/$ ΔT_J	I _D = 250 μA, Referenced to 25°C		12.8		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, T _J = 25°C			10	10 μΑ
		V _{DS} = 60 V, T _J = 125°C			250	
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = 20 \text{ V}$			100	nA
ON CHARACTERISTICS (Note 4)						
Drain-to-Source On Resistance	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 50 \text{ A}$		1.27	1.5	mΩ
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2.0		4.0	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/ \Delta T_J$	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$		-9.4		mV/°C
Forward Transconductance	9FS	V _{DS} = 5 V, I _D = 50 A		157		S
CHARGES, CAPACITANCES & GATE RE	SISTANCE					
Input Capacitance	C _{ISS}	V _{GS} = 0 V, V _{DS} = 30 V, f = 1 MHz		4860		pF
Output Capacitance	C _{OSS}			2800		
Reverse Transfer Capacitance	C _{RSS}			40		
Output Charge	Q _{OSS}			128		nC
Total Gate Charge	Q _{G(TOT)}	$V_{GS} = 10 \text{ V}, V_{DD} = 30 \text{ V}, I_D = 50 \text{ A}$		65		
Threshold Gate Charge	Q _{G(TH)}			13		
Gate-to-Source Charge	Q _{GS}			22		
Gate-to-Drain Charge	Q _{GD}			11		
Gate Resistance	R _G	f = 1 MHz		2		Ω
Gate Voltage Plateau	V _{GP}			4.6		V
SWITCHING CHARACTERISTICS (Note 5)					
Turn-On Delay Time	t _{d(ON)}	Resistive Load, V _{GS} = 0/10 V,		26		ns
Rise Time	t _r	$V_{DD} = 30 \text{ V}, I_D = 50 \text{ A}, R_G = 2.5 \Omega$		8		
Turn-Off Delay Time	t _{d(OFF)}			50		
Fall Time	t _f			9		

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise specified)

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Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	$V_{GS} = 0 \text{ V, } I_S = 50 \text{ A, } T_J = 25^{\circ}\text{C}$		0.81	1.2	V
		V _{GS} = 0 V, I _S = 50 A, T _J = 125°C		0.67		
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V}, I_{S} = 50 \text{ A}$		82		ns
Charge Time	t _a	dI/dt = 100 A/μs		41		
Discharge Time	t _b			41		
Reverse Recovery Charge	Q_{RR}			139		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

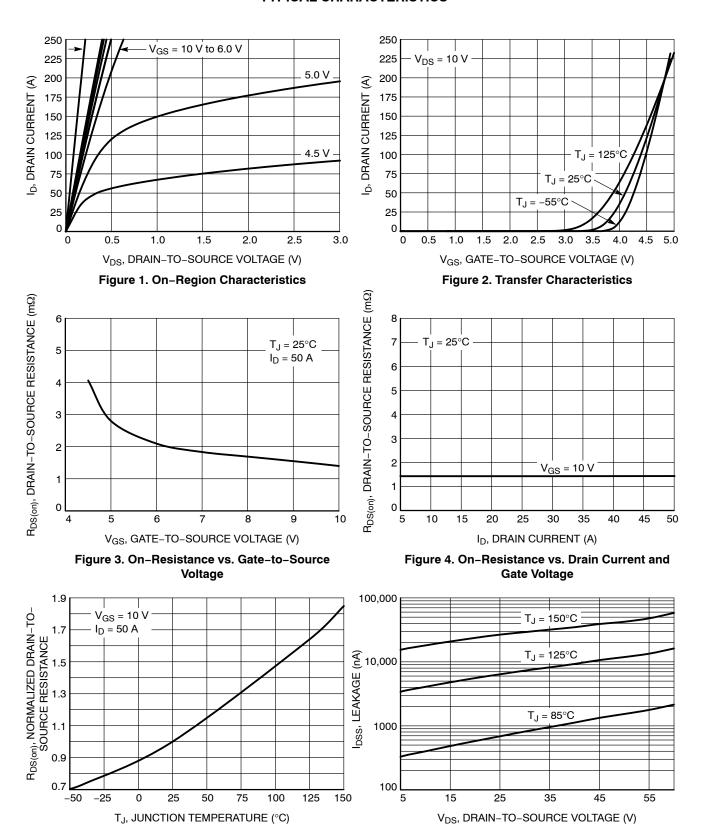


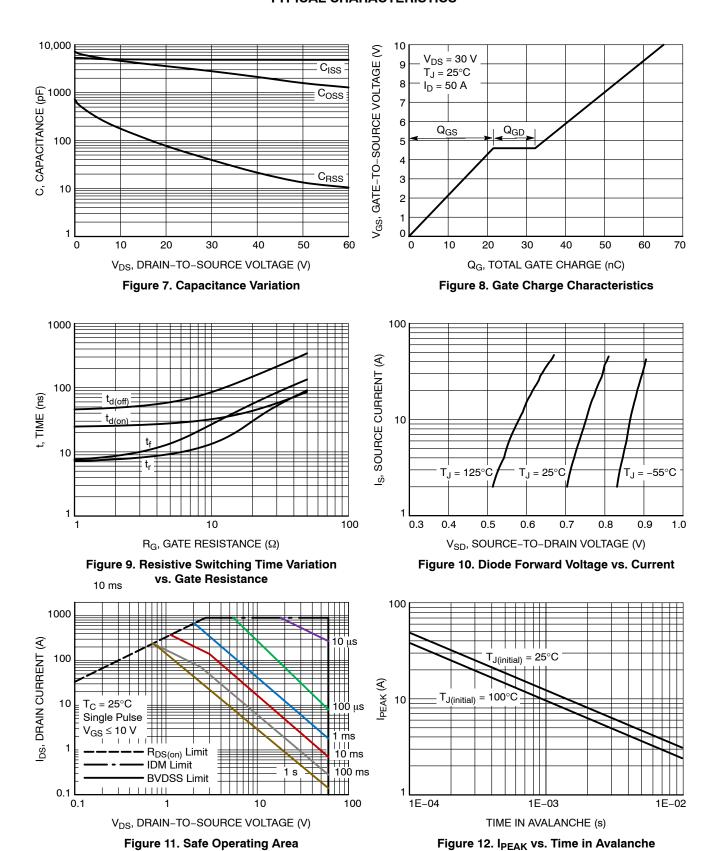
Figure 6. Drain-to-Source Leakage Current

vs. Voltage

Figure 5. On-Resistance Variation with

Temperature

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

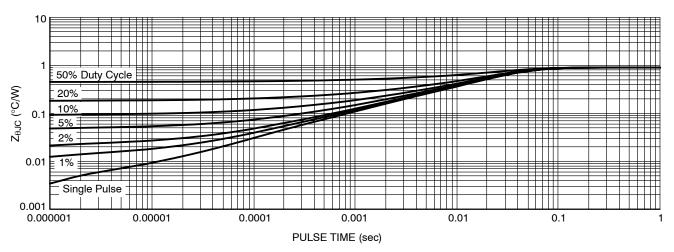


Figure 13. Thermal Characteristics

ORDERING INFORMATION

Device	Device Marking	Package	Shipping [†]
NTMFSC1D6N06CTWG	ЗТ	DFN8 5x6 (Pb-Free/Halogen Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

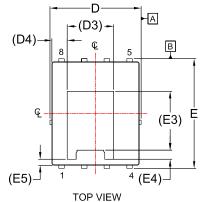
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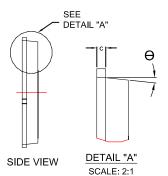


DFN8 5x6.15, 1.27P, DUAL COOL

CASE 506EG ISSUE D

DATE 25 AUG 2020





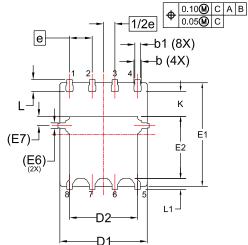
NOTES:

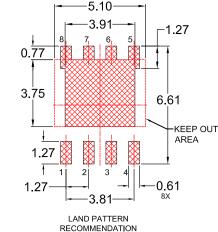
- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.

SEATING PLANE

- 4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
- 5. SEATING PLANE IS DEFINED BY THE TERMINALS.
 "A1" IS DEFINED AS THE DISTANCE FROM THE
 SEATING PLANE TO THE LOWEST POINT ON THE
 PACKAGE BODY.

	// 0.10 C	Θ
FRONT VIEW SEE	8X A	A1 ,
DETAIL "B"	O.10 C DETAIL "B"	C





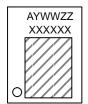
SCALE: 2:1

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRMD.

DIM	MILLIMETERS		
Divi	MIN.	NOM.	MAX.
Α	0.85	0.90	0.95
A1	-	-	0.05
A2	ı	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
С	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	•	3.30 REF	
E4	Ī	0.50 REF	
E5	Û	0.34 REF	:
E6	(0.30 REF	:
E7	-	0.52 REF	:
е	1	1.27 BSC	;
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
θ	0°		12°

GENERIC MARKING DIAGRAM*

BOTTOM VIEW



XXXX = Specific Device Code

A = Assembly Location

Y = Year

WW = Work Week

ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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