

MOSFET - Power, Single N-Channel, Source Down, WDFN9 40 V, 1.3 mΩ, 207 A

NTTFSSH1D3N04XL

Features

- Advanced Source-Down Package Technology (3.3x3.3mm) with Excellent Thermal Conduction
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low QRR with Soft Recovery to Minimize ERR Loss and Voltage Spike
- Low Q_G and Capacitance to Minimize Driving and Switching Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- High Switching Frequency DC-DC Conversion
- Synchronous Rectifier

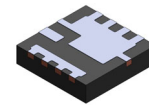
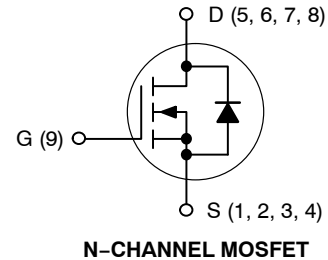
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	40	V
Gate-to-Source Voltage	DC V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	W
Pulsed Drain Current	I_{DM}	$T_C = 25^\circ\text{C}$, $t_p = 100 \mu\text{s}$	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Continuous Source-Drain Current (Body Diode)	I_S	184	A
Single Pulse Avalanche Energy ($I_{PK} = 52 \text{ A}$)	E_{AS}	135	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- The entire application environment impacts the thermal resistance values shown, they are not constants and are valid for the particular conditions noted.
- Surface-mounted on FR4 board using a 1 in² pad size, 1 oz Cu pad.
- E_{AS} of 135 mJ is based on started $T_J = 25^\circ\text{C}$, $I_{AS} = 52 \text{ A}$, $V_{DD} = 32 \text{ V}$, $V_{GS} = 10 \text{ V}$, 100% avalanche tested.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
40 V	1.3 mΩ @ 10 V	207 A
	1.7 mΩ @ 4.5 V	



WDFN9
CASE 511EB

MARKING DIAGRAM

1D3N04
AWLYWW

1D3N04 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

NTTFSSH1D3N04XL

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Bottom)	$R_{\theta JCB}$	1.4	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	60	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$, Referenced to 25°C		17		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{ V}, T_J = 25^\circ\text{C}$			10	μA
		$V_{DS} = 40\text{ V}, T_J = 125^\circ\text{C}$			100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 24\text{ A}$		1.0	1.3	m Ω
		$V_{GS} = 6\text{ V}, I_D = 24\text{ A}$		1.1	1.4	
		$V_{GS} = 4.5\text{ V}, I_D = 19\text{ A}$		1.4	1.7	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 120\text{ }\mu\text{A}$	1.3		2.2	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 120\text{ }\mu\text{A}$		-5		mV/°C
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 24\text{ A}$		123		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}, f = 1\text{ MHz}$		3480		pF
Output Capacitance	C_{OSS}			920		
Reverse Transfer Capacitance	C_{RSS}			32		
Output Charge	Q_{OSS}			35		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 20\text{ V}; I_D = 24\text{ A}$		21		nC
		$V_{GS} = 6\text{ V}, V_{DD} = 20\text{ V}; I_D = 24\text{ A}$		28		
				47		
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 10\text{ V}, V_{DD} = 20\text{ V}; I_D = 24\text{ A}$		5.7		
Gate-to-Source Charge	Q_{GS}			10		
Gate-to-Drain Charge	Q_{GD}			3.4		
Gate Plateau Voltage	V_{GP}			2.9		
Gate Resistance	R_G	$f = 1\text{ MHz}$		0.6		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}, V_{DD} = 20\text{ V},$ $I_D = 24\text{ A}, R_G = 2.5\text{ }\Omega$		18		ns
Rise Time	t_r			5		
Turn-Off Delay Time	$t_{d(OFF)}$			43		
Fall Time	t_f			4		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 24\text{ A}, T_J = 25^\circ\text{C}$		0.79	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 24\text{ A}, T_J = 125^\circ\text{C}$		0.65		

NTTFSSH1D3N04XL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, I _S = 24 A, dI/dt = 1000 A/μs, V _{DD} = 20 V		17		ns
Charge Time	t _a			10		
Discharge Time	t _b			7		
Reverse Recovery Charge	Q _{RR}			84		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NTTFSSH1D3N04XL	1D3N04	WDFN9 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

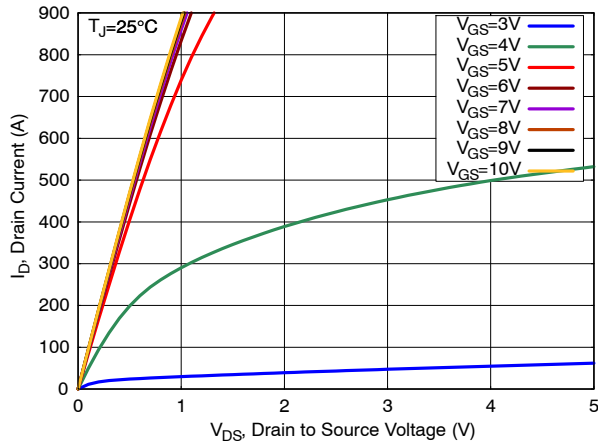


Figure 1. On-Region Characteristics

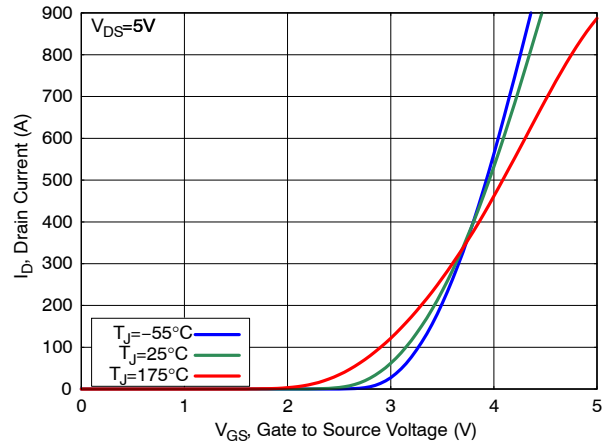


Figure 2. Transfer Characteristics

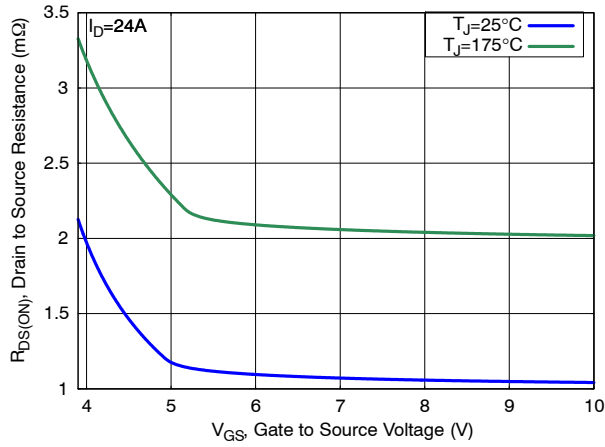


Figure 3. On-Resistance vs. Gate Voltage

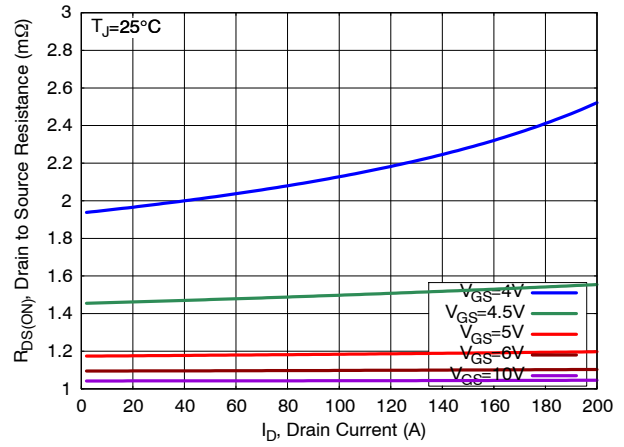


Figure 4. On-Resistance vs. Drain Current

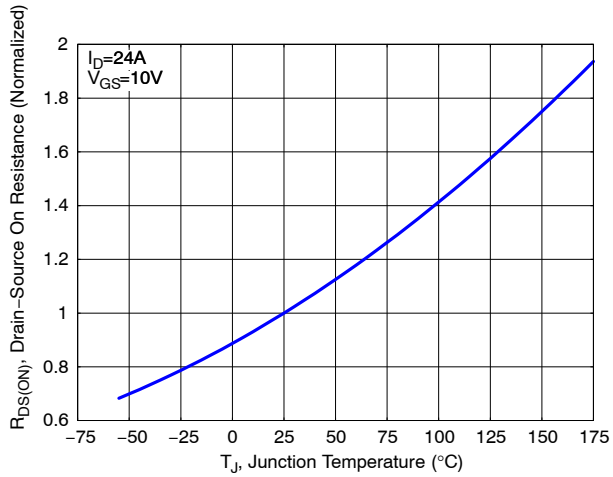


Figure 5. Normalized ON Resistance vs. Junction Temperature

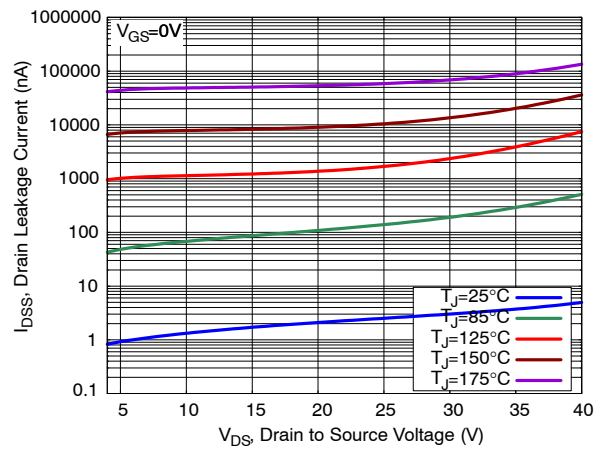


Figure 6. Drain Leakage Current vs. Drain Voltage

NTTFSSH1D3N04XL

TYPICAL CHARACTERISTICS

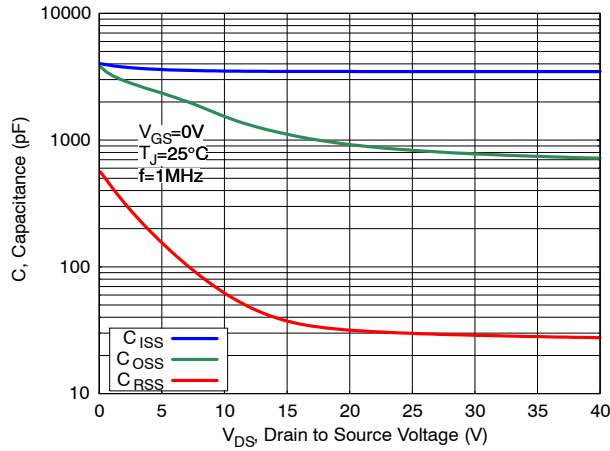


Figure 7. Capacitance Characteristics

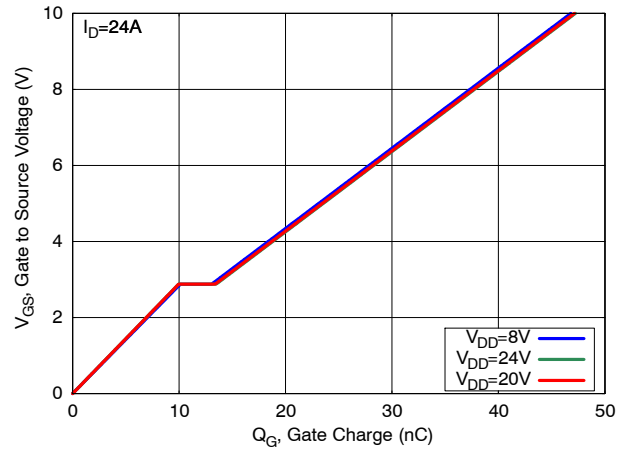


Figure 8. Gate Charge Characteristics

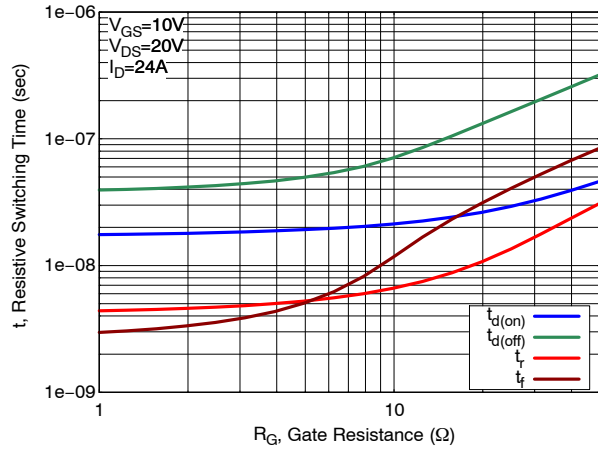


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

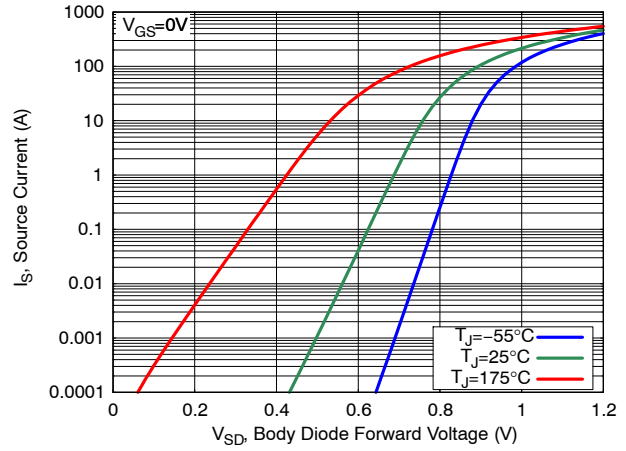


Figure 10. Diode Forward Characteristics

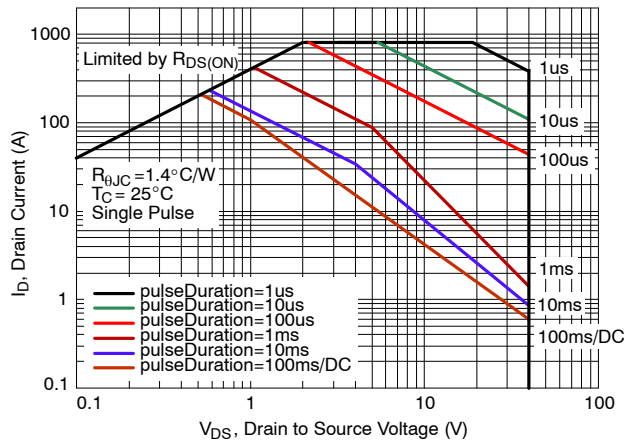


Figure 11. Safe Operating Area (SOA)

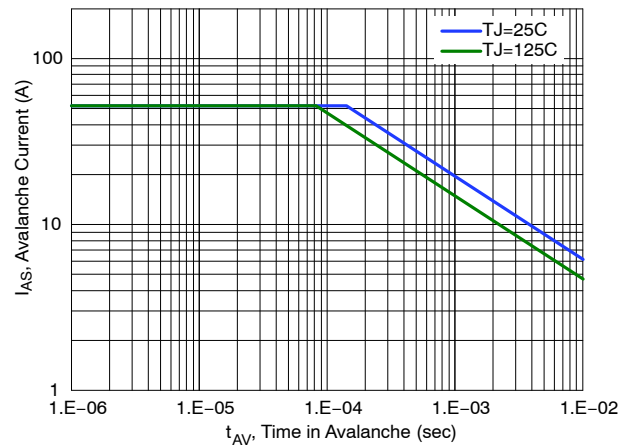


Figure 12. Avalanche Current vs. Pulse Time (UIS)

TYPICAL CHARACTERISTICS

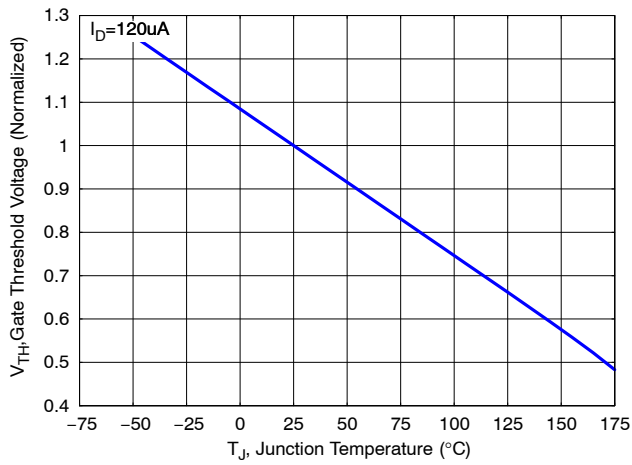


Figure 13. Gate Threshold Voltage vs. Junction Temperature

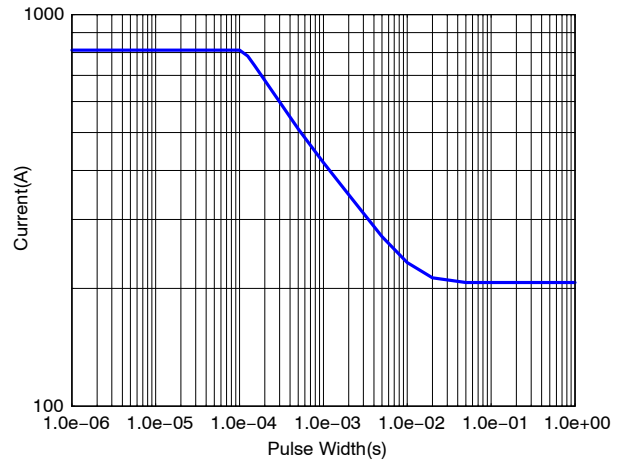


Figure 14. IDM vs. Pulse Width

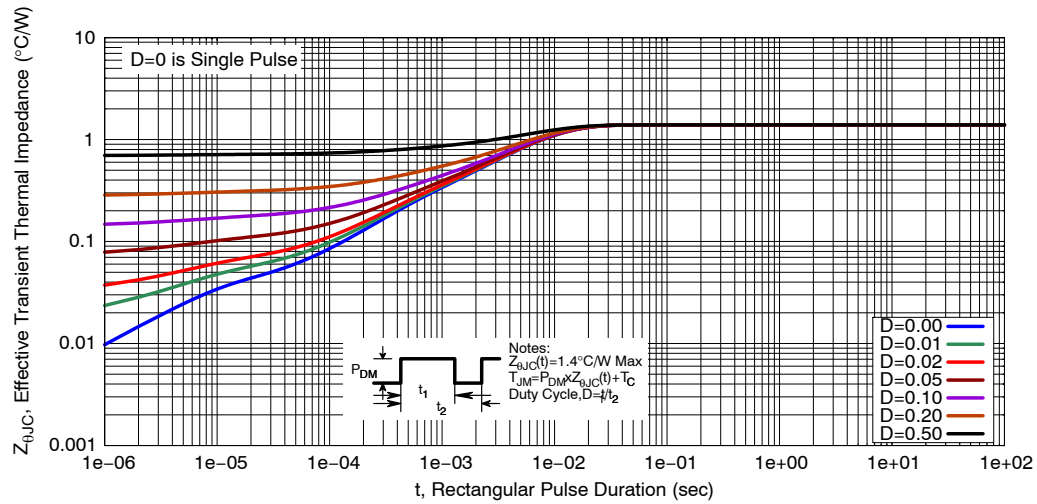
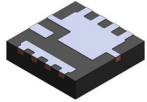
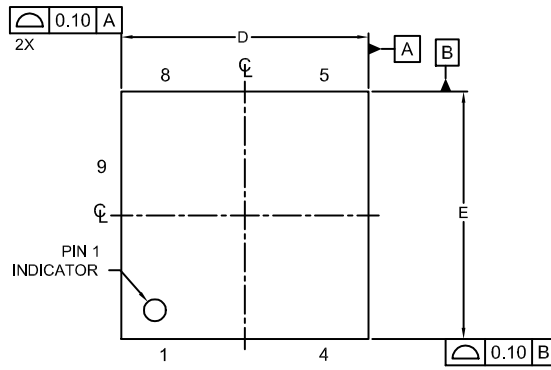
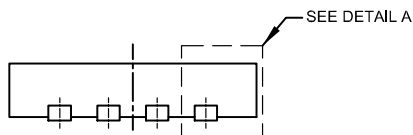
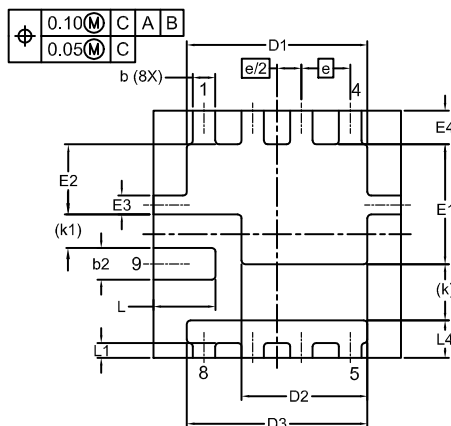
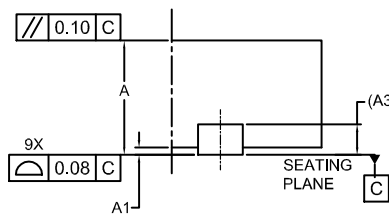


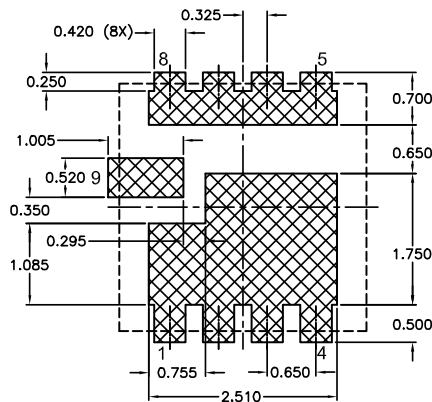
Figure 15. Transient Thermal Response


WDFN9 3.3x3.3, 0.65P
CASE 511EB
ISSUE B

DATE 21 JUL 2021


TOP VIEW

FRONT VIEW

BOTTOM VIEW

DETAIL A

SCALE: 2:1

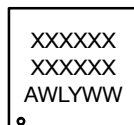

**LAND PATTERN
RECOMMENDATION**

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D1, D2, E1 AND E2 DO NOT INCLUDE MOLD FLASH.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

UNIT IN MILLIMETER			
DIM	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.25	0.30	0.35
b2	0.37	0.42	0.47
D	3.20	3.30	3.40
D1	2.31	2.41	2.51
D2	1.58	1.68	1.78
D3	2.31	2.41	2.51
E	3.20	3.30	3.40
E1	1.50	1.60	1.70
E2	0.84	0.94	1.04
E3	0.20	0.25	0.30
E4	0.35	0.45	0.55
e	0.650 BSC		
e/2	0.325 BSC		
k	0.75 REF		
k1	0.45 REF		
L	0.73	0.83	0.93
L1	0.10	0.20	0.30
L4	0.40	0.50	0.60

**GENERIC
MARKING DIAGRAM***


XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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