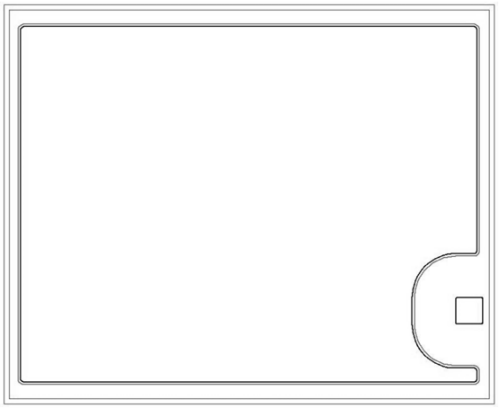
# MOSFET – Power, Single N-Channel
## 30 V, 0.52 mΩ

# NVCW3SS0D5N03CLA



### Features

- Typical RDS(on) = 0.43 mΩ at VGS = 10 V
- Typical Qg(tot) = 139 nC at VGS = 10 V
- AEC−Q101 Qualified
- RoHS Compliant

### DIMENSION (μm)

| | |
|---|---|
| Die Size | 3683 x 3000 |
| Scribe Width | 80 |
| Source Attach Area | 3462 x 2708 |
| Gate Attach Area | 200 x 200 |
| Die Thickness | 76.2 |

Gate: AlCu
Source: Ti−NiV−Ag
Drain: Ti−Ni−Ag (back side of die)
Passivation: Polyimide
Wafer Diameter: 8 inch
Bad dice identified in Inking
Gross Die Count: 2458

### ORDERING INFORMATION

| Device | Package |
|---|---|
| NVCW3SS0D5N03CLA | Unsawn wafer on ring frame |

### RECOMMENDED STORAGE CONDITIONS

| | |
|---|---|
| Temperature | 22 to 28°C |
| RH | 44% to 66% |

The Chip is 100% Probed to Meet the Conditions and Limits Specified at $T_J$ = 25°C

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 30 | – | – | V |
| $I_{DSS}$ | Drain to Source Leakage Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | – | – | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | – | – | 100 | nA |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 1.3 | – | 2.2 | V |
| $R_{DS(on)}$* | Bare Die Drain to Source On Resistance | $I_D$ = 30 A, $V_{GS}$ = 10 V | – | 0.43 | 0.52 | mΩ |
| | | $I_D$ = 30 A, $V_{GS}$ = 4.5 V | – | 0.68 | 0.85 | mΩ |

*Accurate $R_{DS(on)}$ test at die level is not feasible for this thin die as limited by the test contact precision attainable in a die form. The max $R_{DS(on)}$ specification is defined from the historical performance of the die in package but is not guaranteed by test in production. The die $R_{DS(on)}$ performance depends on the Source wire/ribbon bonding layout.

**ABSOLUTE MAXIMUM RATINGS** in Reference to the NVMFS4C01N electrical data in SO−8FL ($T_J$ = 25°C unless otherwise noted)

| Symbol | Parameter | | Ratings | Unit |
|---|---|---|---|---|
| $V_{DSS}$ | Drain to Source Voltage | | 30 | V |
| $V_{GS}$ | Gate to Source Voltage | | ±20 | V |
| $I_D$ | Continuous Drain Current $R_{\theta JC}$ (Note 1,3) | $T_C$ = 25°C | 370 | A |
| $P_D$ | Power Dissipation $R_{\theta JC}$ (Note 1,3) | $T_C$ = 25°C | 161 | W |
| $E_{AS}$ | Single Pulse Avalanche Energy ($I_{L(pk)}$ = 35 A) | | 862 | mJ |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature | | −55 to +175 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**THERMAL CHARACTERISTICS** in Reference to the NVMFS4C01N electrical data in SO−8FL (Note 1)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case, Max | 0.93 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient, Max (Note 2) | 39 | °C/W |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 $mm^2$, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

**ELECTRICAL CHARACTERISTICS** in Reference to the NVMFS4C01N electrical data in SO−8FL ($T_J$ = 25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 30 | – | – | V |
| $I_{DSS}$ | Drain to Source Leakage Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | – | – | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | – | – | 100 | nA |
| **ON CHARACTERISTICS** (Note 4) | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 1.3 | | 2.2 | V |
| $R_{DS(on)}$ | Drain to Source On−Resistance | $V_{GS}$ = 10 V, $I_D$ = 30 A | – | 0.56 | 0.67 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 30 A | – | 0.76 | 0.95 | mΩ |
| **CHARGES AND CAPACITANCES** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1 MHz | – | 10144 | – | pF |
| $C_{oss}$ | Output Capacitance | | – | 5073 | – | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 148 | – | pF |
| $Q_{g(ToT)}$ | Total Gate Charge | $V_{GS}$ = 4.5 V, $V_{DS}$ = 15 V, $I_D$ = 30 A | – | 63 | – | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | – | 29 | – | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | – | 13 | – | nC |
| $Q_{g(ToT)}$ | Total Gate Charge | $V_{GS}$ = 10 V, $V_{DS}$ = 15 V, $I_D$ = 30 A | | 139 | | nC |
| **SWITCHING CHARACTERISTICS** (Note 5) | | | | | | |
| $t_{d(on)}$ | Turn−On Delay Time | $V_{GS}$ = 4.5 V, $V_{DS}$ = 15 V, $I_D$ = 15 A, $R_G$ = 3.0 Ω | – | 29 | – | ns |
| $t_r$ | Rise Time | | – | 68 | – | ns |
| $t_{d(off)}$ | Turn−Off Delay Time | | – | 53 | – | ns |
| $t_f$ | Fall Time | | – | 36 | – | ns |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Voltage | $I_S$ = 10 A, $V_{GS}$ = 0 V | – | – | 1.1 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $dI_S/dt$ = 100 A/μA, $I_S$ = 30 A | – | 87 | – | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | – | 147 | – | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

## TYPICAL CHARACTERISTICS

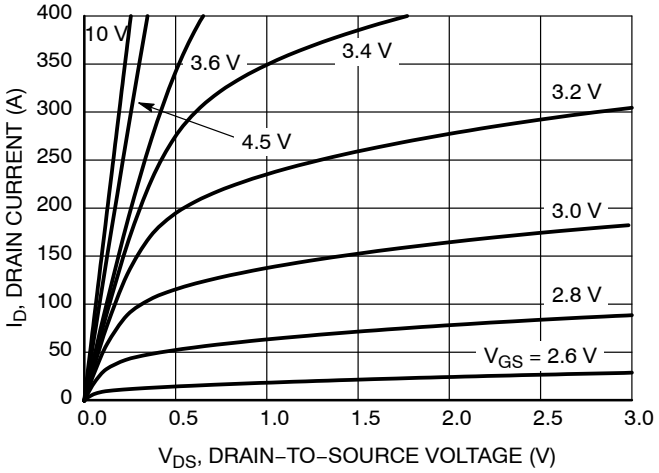



**Figure 1. On−Region Characteristics**

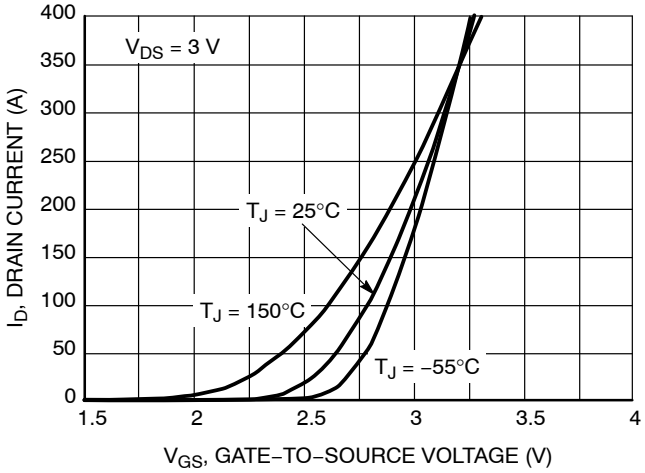



**Figure 2. Transfer Characteristics**

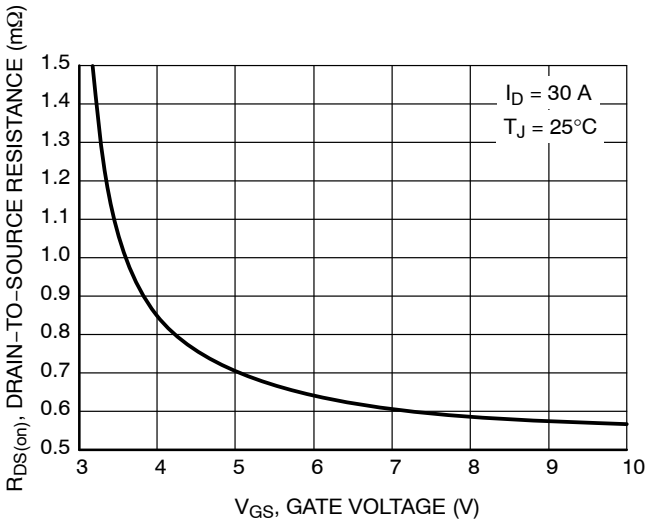



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

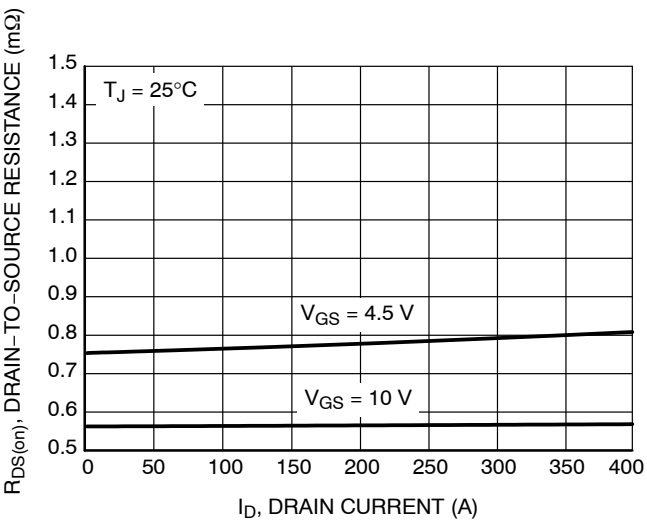



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

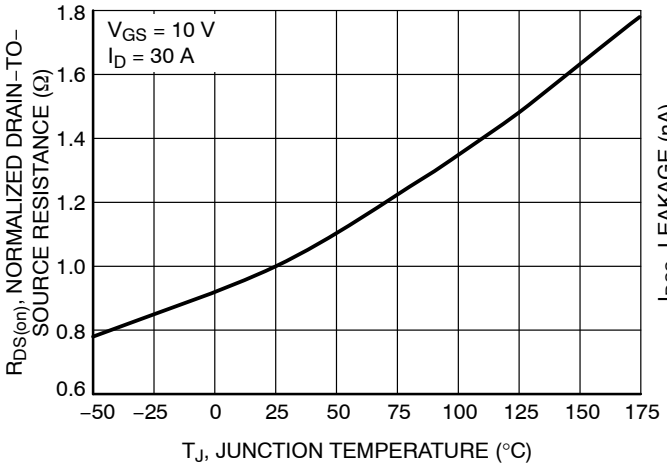



**Figure 5. On−Resistance Variation with Temperature**

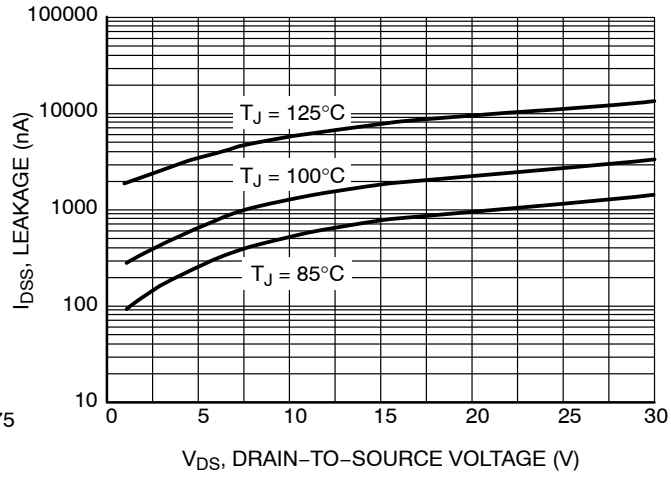



**Figure 6. Drain−to−Source Leakage Current vs. Voltage**

## TYPICAL CHARACTERISTICS

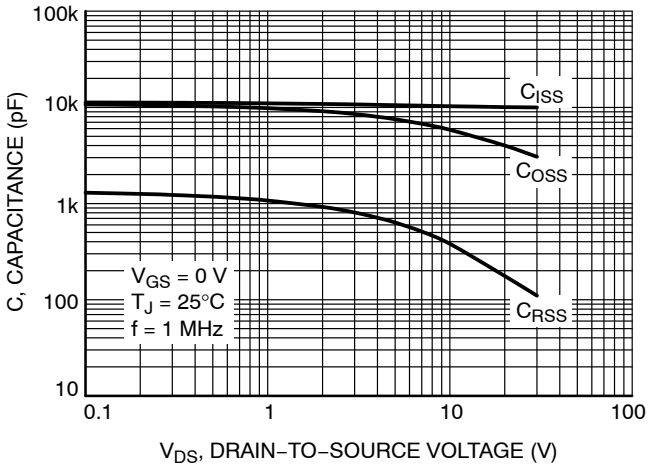



**Figure 7. Capacitance Variation**

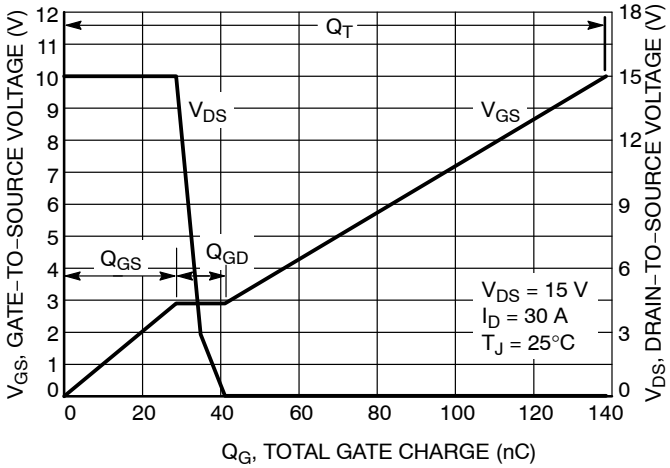



**Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge**

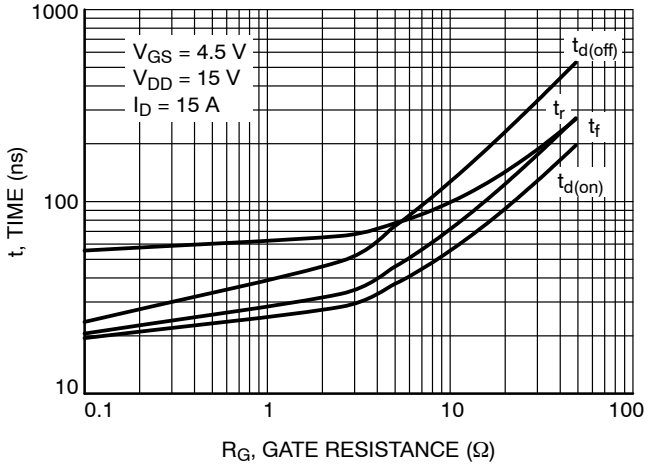



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

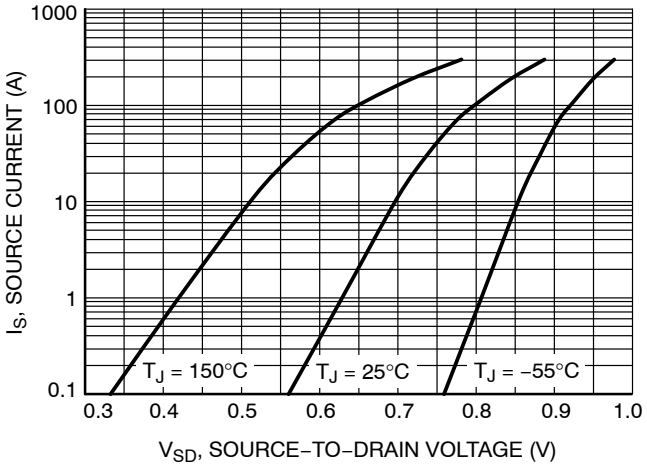



**Figure 10. Diode Forward Voltage vs. Current**

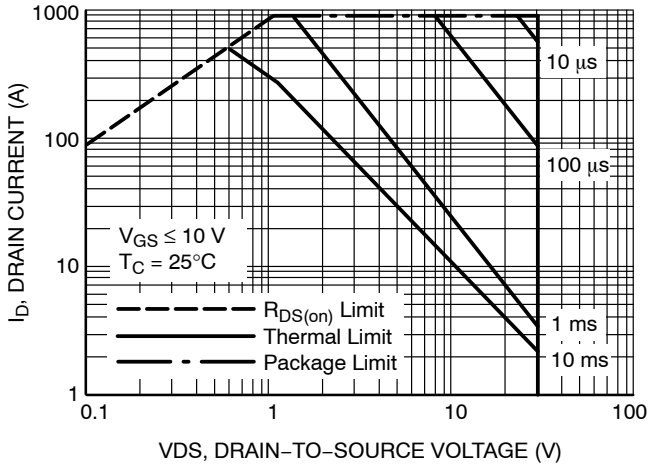



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

## TYPICAL CHARACTERISTICS

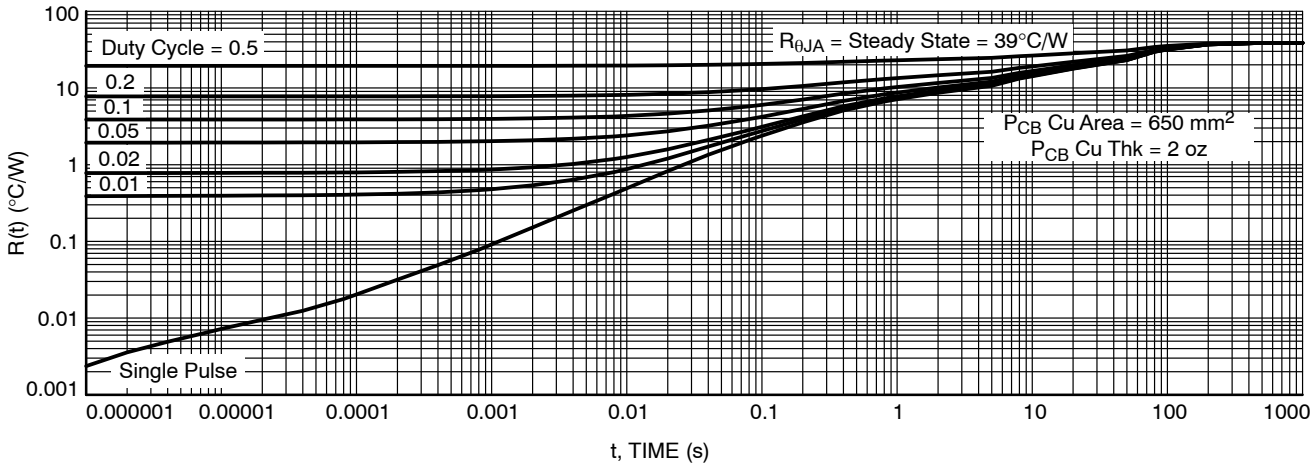



**Figure 12. Thermal Impedance (Junction−to−Ambient)**

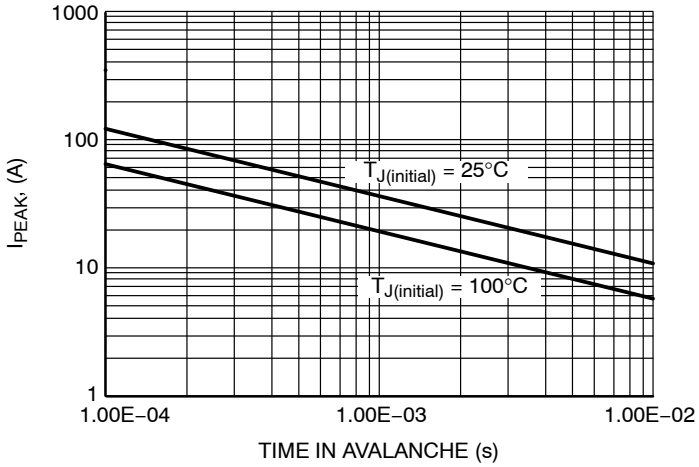



**Figure 13. Avalanche Characteristics**



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