

MOSFET – Power, N-Channel

100 V, 1.8 mΩ

PCFA86062WA



ON Semiconductor®

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Features

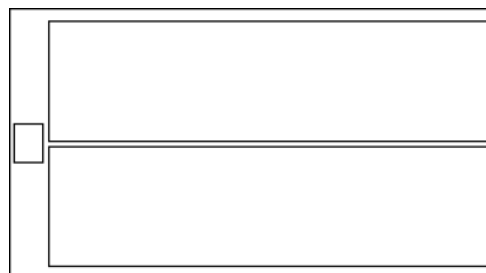
- Typical $R_{DS(on)}$ = 1.4 mΩ at V_{GS} = 10 V
- Typical $Q_{g(tot)}$ = 95 nC at V_{GS} = 10 V
- AEC-Q101 Qualified and PPAP Capable
- RoHS Compliant

DIMENSION (μm)

Die Size	6604 × 3683
Saw Street Width	60
Source Attach Area	(5971.4 × 1639.6) × 2
Gate Attach Area	390 × 540
Die Thickness	101.6 ±19.1

Gate and Source: AlSiCu
Drain: Ti-NiV-Ag (back side of die)
Passivation: Polyimide
Wafer Diameter: 8 inch
Wafer Unsawn on UV Tape
Bad dice identified in inking
Gross Die Counts: 1006

The Chip is 100% Probed to Meet the Conditions and Limits Specified at $T_J = 25^\circ\text{C}$.



ORDERING INFORMATION

Device	Package
PCFA86062WA	Wafer Unsawn on Foil

RECOMMENDED STORAGE CONDITIONS

Temperature	22 to 28°C
RH	40 to 66%

Symbol	Parameter	Condition	Min	Typ	Max	Unit
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$	100	–	–	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0 \text{ V}$	–	–	5	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0 \text{ V}$	–	–	±100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu\text{A}$	2.0	–	4.0	V
* $R_{DS(on)}$	Bare Die Drain to Source On Resistance	$I_D = 5 \text{ A}$, $V_{GS} = 10 \text{ V}$	–	1.4	1.8	mΩ
V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 5 \text{ A}$, $V_{GS} = 0 \text{ V}$	–	–	1.25	V

*Accurate $R_{DS(on)}$ test at die level is not feasible as limited by the test contact precision attainable in a die form. The max $R_{DS(on)}$ specification is defined from the historical performance of the die in package but is not guaranteed by test in production. The die $R_{DS(on)}$ performance depends on the Source wire/ribbon bonding layout.

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MOSFET MAXIMUM RATINGS in Reference to the FDBL86062–F085 electrical data in TOLL
($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Continuous Drain Current $R_{\theta JC}$ ($V_{GS} = 10$) (Note 1) $T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	315.7 223.2	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	352	mJ
P_D	Power Dissipation $R_{\theta JC}$	429	W
	Derate Above 25°C	2.86	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to $+175$	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.35	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 3)	43	$^\circ\text{C}/\text{W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by silicon.
2. Starting $T_J = 25^\circ\text{C}$, $L = 0.1$ mH, $I_{AS} = 84$ A
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

ELECTRICAL CHARACTERISTICS in Reference to the FDBL86062–F085 electrical data in TOLL
($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0$ V		100	–	–	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS} = 100$ V, $V_{GS} = 0$ V	$T_J = 25^\circ\text{C}$	–	–	5	μA
			$T_J = 175^\circ\text{C}$ (Note 4)	–	–	2	mA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20$ V		–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu\text{A}$		2.0	3.1	4.0	V
$R_{DS(on)}$	Drain to Source On-Resistance	$I_D = 80$ A, $V_{GS} = 10$ V	$T_J = 25^\circ\text{C}$	–	1.5	2.0	m Ω
			$T_J = 175^\circ\text{C}$ (Note 4)	–	3.3	4.3	m Ω

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz	–	6970	–	pF
C _{oss}	Output Capacitance		–	3950	–	pF
C _{rss}	Reverse Transfer Capacitance		–	29	–	pF
R _g	Gate Resistance	f = 1 MHz	–	0.4	–	Ω
Q _{g(ToT)}	Total Gate Charge	V _{GS} = 0 to 10 V, V _{DD} = 80 V, I _D = 80 A	–	95	–	nC
Q _{g(th)}	Threshold Gate Charge	V _{GS} = 0 to 2 V, V _{DD} = 80 V, I _D = 80 A	–	13	–	nC
Q _{gs}	Gate to Source Gate Charge	V _{DD} = 75 V, I _D = 80 A	–	31	–	nC
Q _{gd}	Gate to Drain “Miller” Charge		–	20	–	nC

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay	$V_{DD} = 50$ V, $I_D = 80$ A, $V_{GS} = 10$ V, $R_{GEN} = 6 \Omega$	–	31	–	ns
t_r	Rise Time		–	25	–	ns
$t_{d(off)}$	Turn-Off Delay		–	36	–	ns
t_f	Fall Time		–	9	–	ns

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ELECTRICAL CHARACTERISTICS in Reference to the FDBL86062–F085 electrical data in TOLL
($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DRAIN–SOURCE DIODE CHARACTERISTIC						
V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 80\text{ A}, V_{GS} = 0\text{ V}$	–	–	1.25	V
		$I_{SD} = 40\text{ A}, V_{GS} = 0\text{ V}$	–	–	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 80\text{ A}, dI_{SD}/dt = 100\text{ A}/\mu\text{s},$ $V_{DD} = 80\text{ V}$	–	115	–	ns
Q_{rr}	Reverse Recovery Charge		–	172	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at $T_J = 175^\circ\text{C}$. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

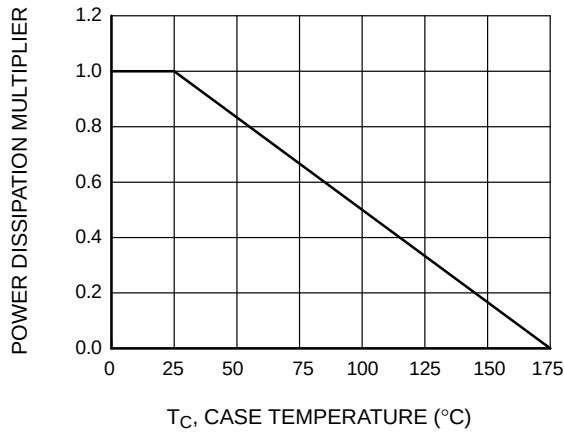


Figure 1. Normalized Power Dissipation vs. Case Temperature

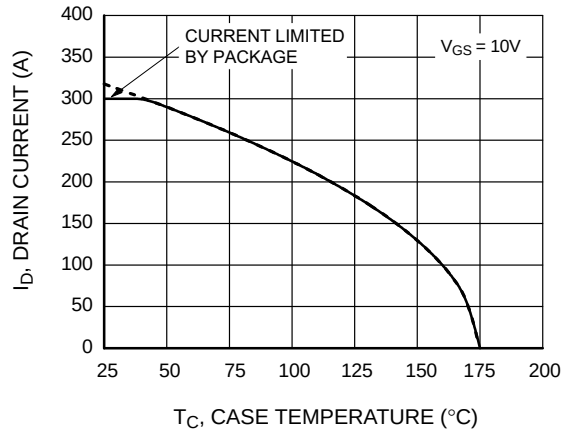


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

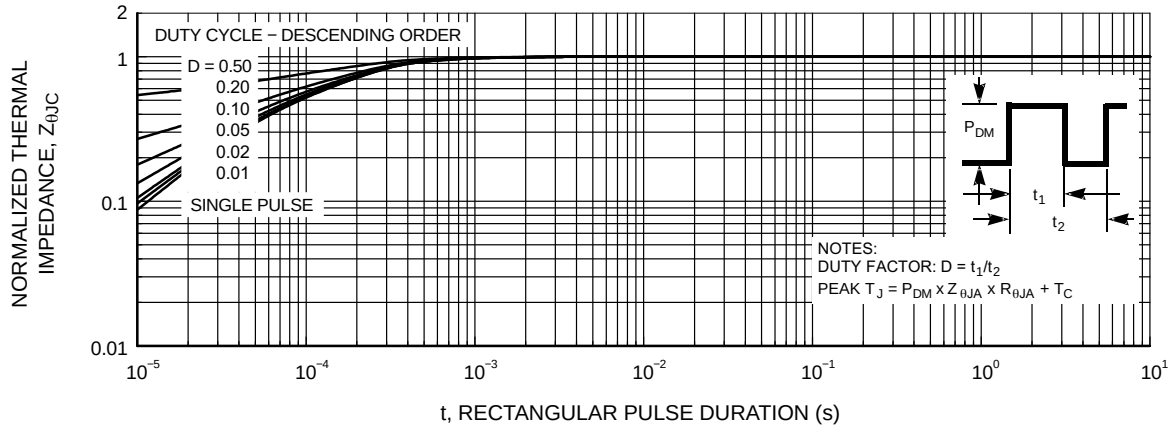


Figure 3. Normalized Maximum Transient Thermal Impedance

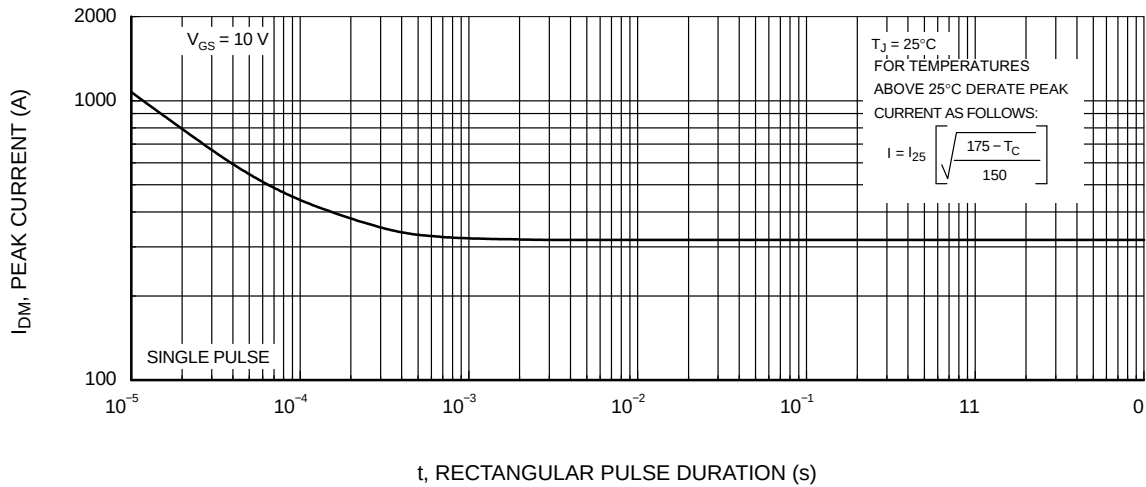


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

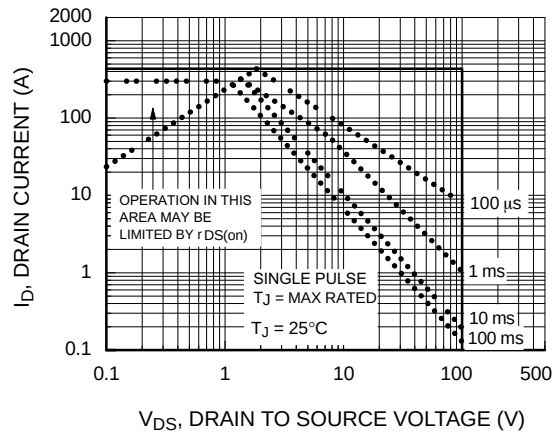


Figure 5. Forward Bias Safe Operating Area

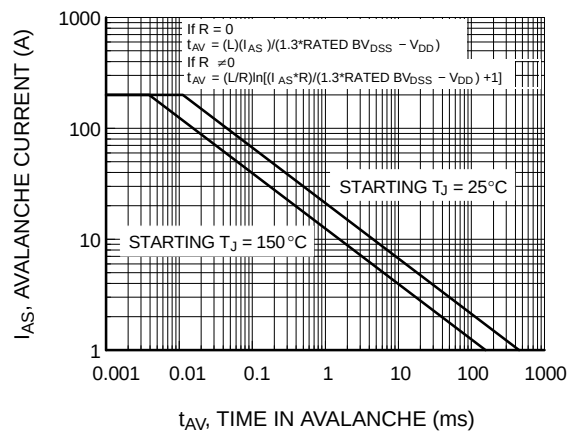


Figure 6. Unclamped Inductive Switching Capability

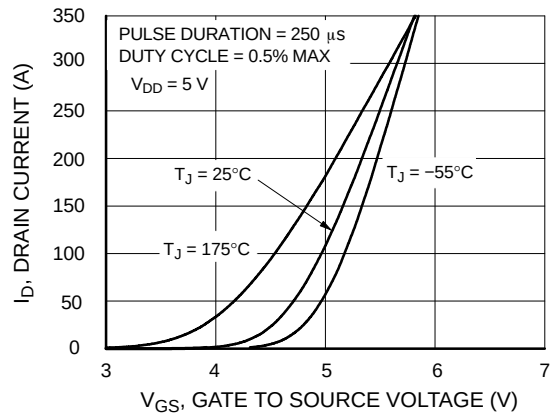


Figure 7. Transfer Characteristics

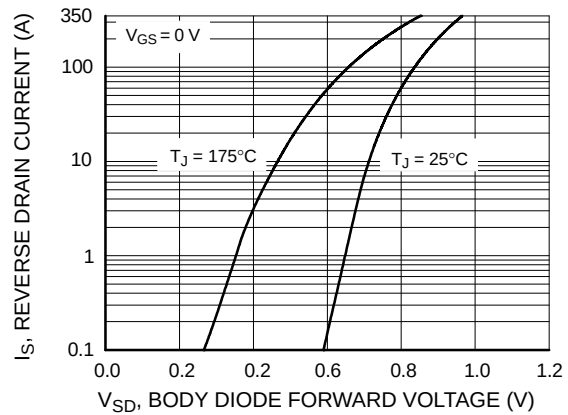


Figure 8. Forward Diode Characteristics

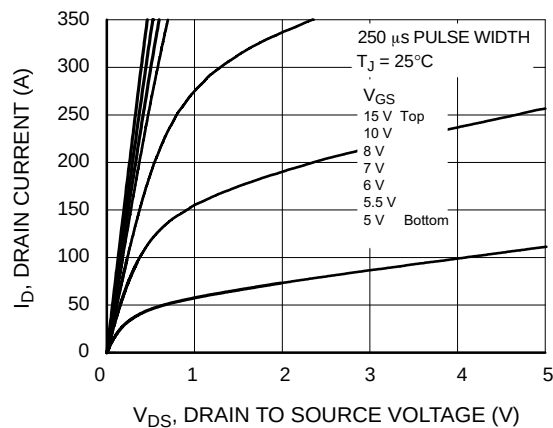


Figure 9. Saturation Characteristics

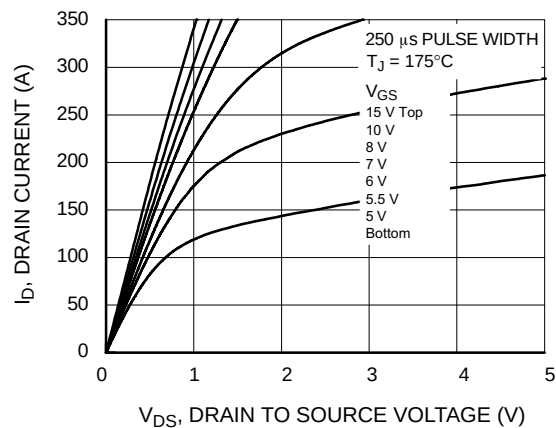


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)

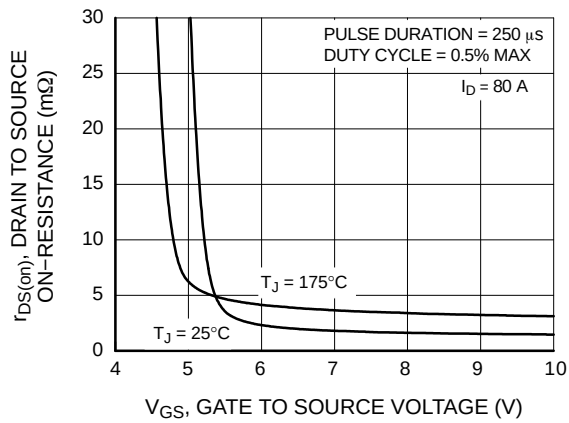
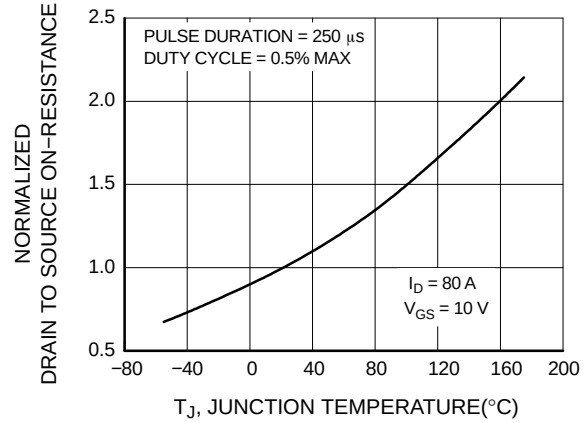
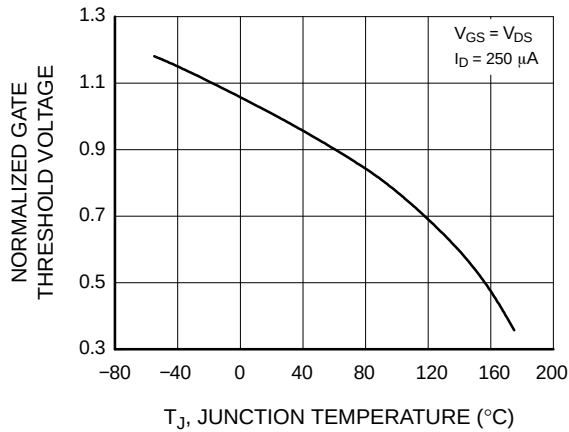
Figure 11. $R_{DS(on)}$ vs. Gate VoltageFigure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

Figure 13. Normalized Gate Threshold Voltage vs. Temperature

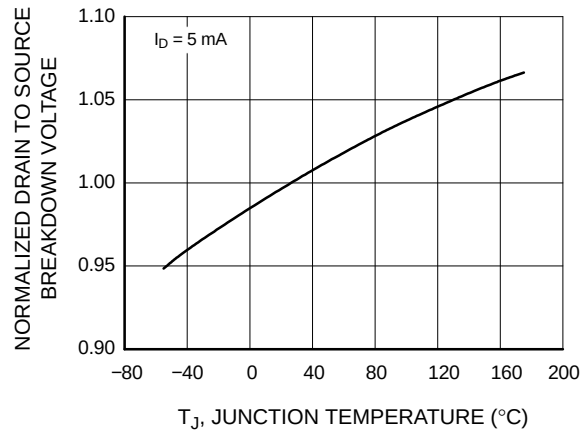


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

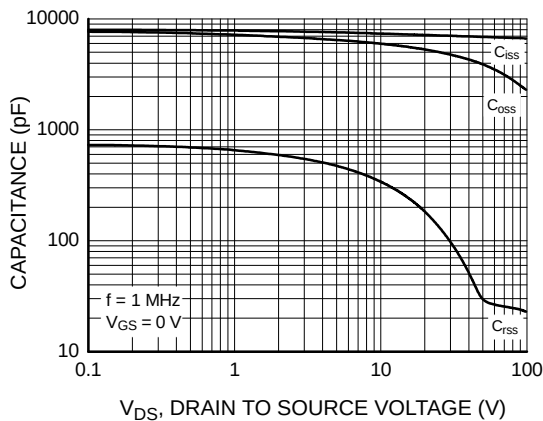


Figure 15. Capacitance vs. Drain to Source Voltage

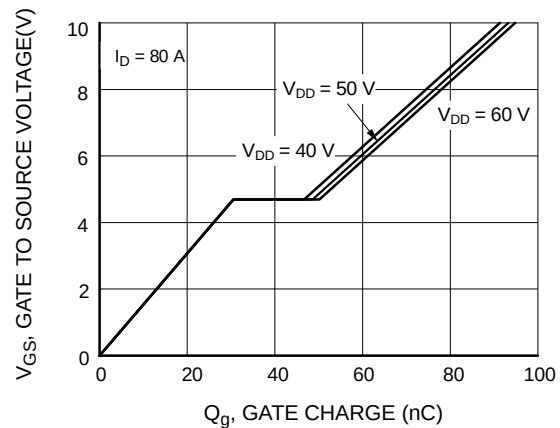


Figure 16. Gate Charge vs. Gate to Source Voltage

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