NCN7200

Data Switch, Gigabit Ethernet LAN, with 2:1 Mux/ DeMux and Power-Down Feature

The NCN7200 is pin−compatible to the PI3L720ZHE and comes in a 42−pin WQFN package (3.5 mm x 9 mm x 0.5 mm Pitch). The NCN7200 is an 8−channel, bidirectional switch with a power shutdown feature that puts all outputs in a high−impedance state. The switch is compatible with 10/100/1000 Base−T Ethernet standards. The device has 3 additional lines for status indicator LEDs which are switched together with the Ethernet pairs.

Features

- 2:1 Mux/ DeMux LAN Switch
- Three Extra Channels Facilitate LED Switching
- Fully Specified for Power Supply Range: 3 V to 3.6 V
- Powerdown Feature Conserves Energy
- ESD Protection
  - 8 kV HBM (Human Body Model, I/O to GND)
  - 10 kV Contact Discharge (IEC61000−4−2)
- Low Crosstalk: −70 dB
- Pin−to−Pin Replacement for PI3L720ZHE
- This is a Pb−Free Device

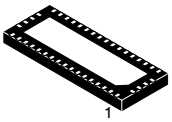
Typical Applications

- Routes signals for 10/100/1000 Mbps Ethernet
- Facilitates Docking System by Interfacing One Controller to Dual Connectors

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM



WQFN42
CASE 510AP

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

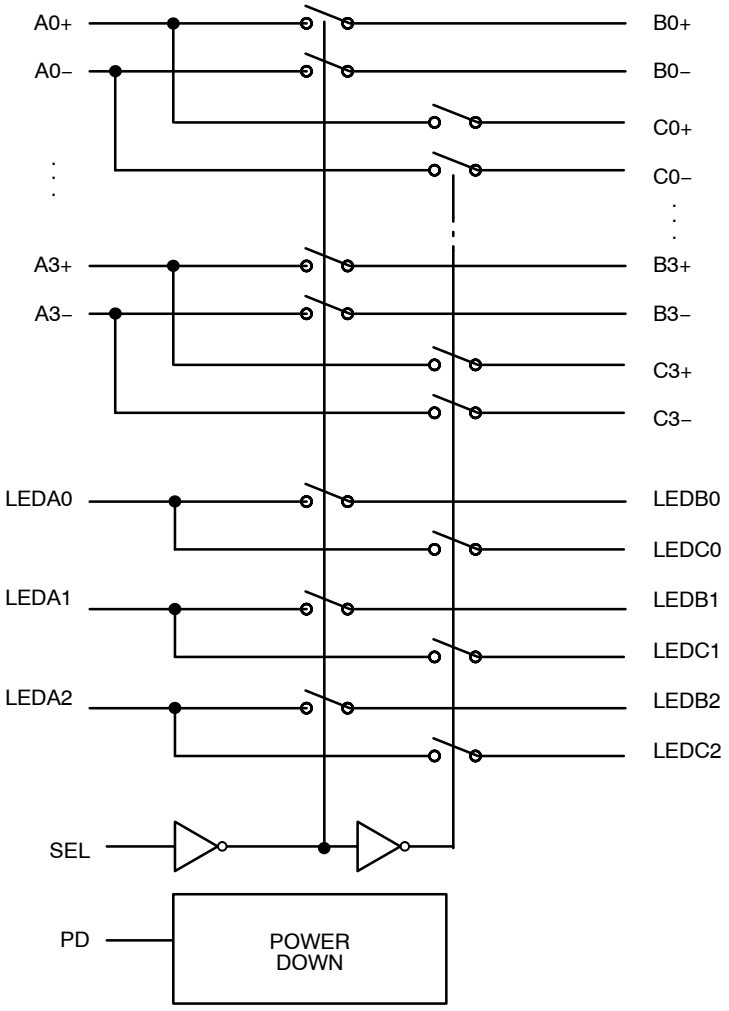


Figure 1. Detailed Block Diagram

TRUTH TABLE

PD	SEL	Function
L	L	AX to BX; LEDAX to LEDBX
L	H	AX to CX; LEDAX to LEDCX
H	X	Hi−Z

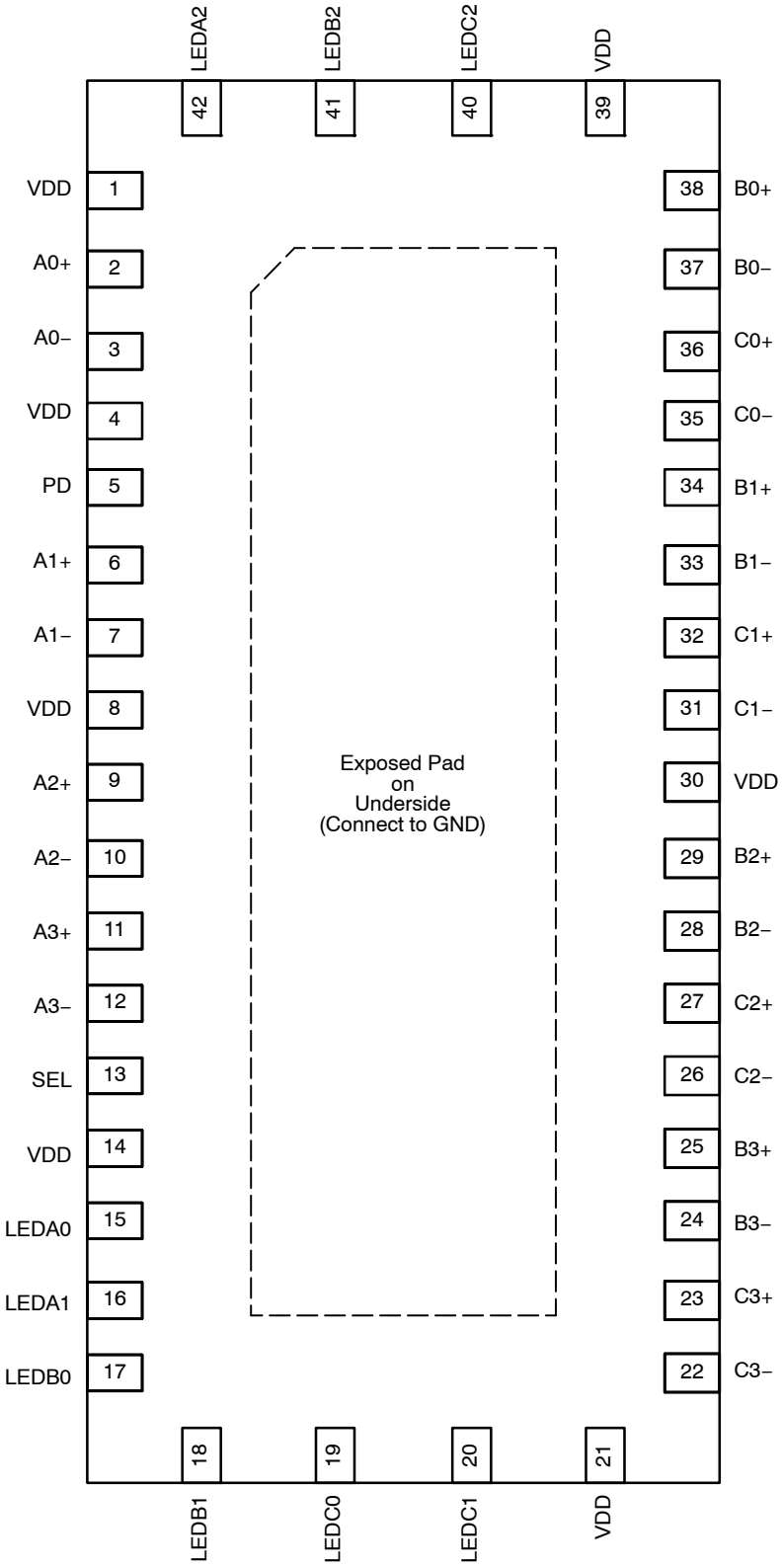


Figure 2. Pin Description
(Top View)

PIN DESCRIPTION

Pin Name	Description
AX+, AX−	Port A DeMux I/O
BX+, BX−	Port B Mux I/O
CX+, CX−	Port C LED Mux I/O
GND	Ground
LEDZX	LED I/O
PD	Powerdown, Active high, with internal pulldown resistor
SEL	Select
V_{DD}	Power

MAXIMUM RATINGS

Description	Value	Unit
Storage Temperature	−65 to +150	°C
Supply Voltage to Ground Potential	−0.5 to +4.0	V
DC Input Voltage	−0.5 to +5.5	V
DC Output Current (Note 1)	120	mA
Power Dissipation (Note 1)	0.5	W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Continuous short−circuit operation to ground at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability. Shorting output to either V+ or V− will adversely affect reliability.

GIGABIT ETHERNET LAN SWITCH WITH 2:1 MUX/ DEMUX AND POWER DOWN FEATURE

(Min / Max values are at V_{DD} = 3.3 V ±10%, T_A = −40°C to +85°C. Typ values are at V_{DD} = 3.3 V and T_A = 25°C)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
POWER SUPPLY CHARACTERISTICS (Note 2)						
V_{DD}	Power DC Supply Voltage		3.0	3.3	3.6	V
$I_{DD-Standby}$	Quiescent Power Supply Current	V_{DD} = 3.6 V, V_{IN} = GND or V_{DD}		0.38	0.45	mA
$I_{DD-Active}$	Active Power Supply Current	V_{DD} = 3.6 V, V_{IN} = V_{DD} or GND		1.0	1.5	mA
I_{DD-PD}	Power Down Current	P_D = 1, V_{DD} = 3.6 V, V_{IN} = V_{DD} or GND		0.13	0.16	mA

2. Active power represents normal data communication. Standby power is when the device is enabled for operation but there is no LAN traffic (cable not connected). Power down current is the minimum power state used when not connected and mobile.
3. Measured by the voltage drop between A and B pins at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A & B) pins.
4. Guaranteed by design and/or characterization.
5. The bus switch contributes no propagational delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

GIGABIT ETHERNET LAN SWITCH WITH 2:1 MUX/ DEMUX AND POWER DOWN FEATURE

(Min / Max values are at V_{DD} = 3.3 V ±10%, T_A = −40°C to +85°C. Typ values are at V_{DD} = 3.3 V and T_A = 25°C)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
CONTROL LOGIC (SEL AND PD PINS) DC ELECTRICAL CHARACTERISTICS FOR 1000 BASE−T ETHERNET SWITCHING						
V_{IH}	Input HIGH Voltage	Guaranteed HIGH level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed LOW level	−0.5		0.8	
V_{IK}	Clamp Diode Voltage	V_{DD} = Max, I_{IN} = −18 mA		−0.7	−1.0	
I_{IHSEL}	Input HIGH Current (SEL)	V_{DD} = Max, V_{IN} = V_{DD}			±0.1	μA
I_{IHPD}	Input High Current (PD)	V_{DD} = Max, V_{IN} = V_{DD}			±1.2	
I_{IL}	Input LOW Current	V_{DD} = Max, V_{IN} = GND			±0.1	
I_{OFF}	Off−Leakage Current (SEL)	V_{DD} = 0 V, V_{IN} = 0 V to V_{DD}			±0.1	
DATA PATH (AX TO BX, CX PINS) DC ELECTRICAL CHARACTERISTICS FOR 1000 BASE−T ETHERNET SWITCHING						
R_{ON}	Switch On−Resistance (Note 3)	V_{DD} = Min, 1.5 V < V_{IN} < V_{DD}, I_{TN} = −40 mA		2.0	6.0	Ω
$R_{FLAT(ON)}$	On−Resistance Flatness (Note 3)	V_{DD} = Min, V_{IN} @ 1.5 V and V_{DD}, I_{TN} = −40 mA		0.3		
ΔR_{ON}	On−Resistance match from center ports to any other port (Note 3)	V_{DD} = Min, 1.5 V < V_{IN} < V_{DD}, I_{TN} = −40 mA		0.5	1.0	
I_{ON}	On Leakage Current (AX)	V_{DD} = 3.6 V, V_{AX} = 0 V or V_{DD}, V_{OUT} = Float	−0.1		+0.1	μA
I_{OFF}	Off Leakage Current (AX/BX/CX)	V_{DD} = 3.6 V, V_{IN} = 0 V or V_{DD}, V_{OUT} = V_{DD} or 0 V	−0.1		+0.1	μA
DATA PATH (LEDAX TO LEDBX, LEDCX PINS) DC ELECTRICAL CHARACTERISTICS FOR 1000 BASE−T ETHERNET SWITCHING						
R_{ON}	Switch On−Resistance (Note 3)	V_{DD} = Min, 1.5 V < V_{IN} < V_{DD}, I_{TN} = −40 mA		7.0	16	Ω
$R_{FLAT(ON)}$	On−Resistance Flatness (Note 3)	V_{DD} = Min, V_{IN} @ 1.5 V and V_{DD}, I_{TN} = −40 mA		0.3		
ΔR_{ON}	On−Resistance match from center ports to any other port (Note 3)	V_{DD} = Min, 1.5 V < V_{IN} < V_{DD}, I_{TN} = −40 mA		0.8	1.25	
I_{ON}	On Leakage Current (LEDAX)	V_{DD} = 3.6 V, V_{AX} = 0 V or V_{DD}, V_{OUT} = Float	−0.1		+0.1	μA
I_{OFF}	Off Leakage Current (LEDAX/LEDBX/LEDCX)	V_{DD} = 3.6 V, V_{IN} = 0 V or V_{DD}, V_{OUT} = V_{DD} or 0 V	−0.1		+0.1	μA
CONTROL LOGIC (SEL AND PD PINS) DC ELECTRICAL CHARACTERISTICS FOR 10/100 BASE−T ETHERNET SWITCHING						
V_{IH}	Input HIGH Voltage	Guaranteed HIGH level (Control Pins)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed LOW level (Control Pins)	−0.5		0.8	
V_{IK}	Clamp Diode Voltage	V_{DD} = Max, IN = −18 mA		−0.7	−1.0	
I_{IHSEL}	Input HIGH Current (SEL)	V_{DD} = Max, V_{IN} = V_{DD}			±0.1	μA
I_{IHPD}	Input HIGH Current (PD)	V_{DD} = Max, V_{IN} = V_{DD}			±1.2	
I_{IL}	Input LOW Current	V_{DD} = Max, V_{IN} = GND			±0.1	
I_{OFF}	Off−Leakage Current (SEL)	V_{DD} = 0 V, V_{IN} = 0 V to V_{DD}			±0.1	

2. Active power represents normal data communication. Standby power is when the device is enabled for operation but there is no LAN traffic (cable not connected). Power down current is the minimum power state used when not connected and mobile.
3. Measured by the voltage drop between A and B pins at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A & B) pins.
4. Guaranteed by design and/or characterization.
5. The bus switch contributes no propagational delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

GIGABIT ETHERNET LAN SWITCH WITH 2:1 MUX/ DEMUX AND POWER DOWN FEATURE

(Min / Max values are at V_{DD} = 3.3 V ±10%, T_A = −40°C to +85°C. Typ values are at V_{DD} = 3.3 V and T_A = 25°C)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
DATA PATH (AX TO BX, CX PINS) DC ELECTRICAL CHARACTERISTICS FOR 10/100 BASE−T ETHERNET SWITCHING						
R_{ON}	Switch On−Resistance (Note 3)	V_{DD} = Min, 1.25 V < V_{IN} < V_{DD}, I_{TN} = −10 mA to −30 mA		2.0	6.0	Ω
$R_{FLAT(ON)}$	On−Resistance Flatness (Note 3)	V_{DD} = Min, 1.25 V < V_{IN} < V_{DD}, I_{TN} = −10 mA to −30 mA		0.8		
ΔR_{ON}	On−Resistance match from center ports to any other port (Note 3)	V_{DD} = Min, 1.25 V < V_{IN} < V_{DD}, I_{TN} = −10 mA to −30 mA		0.8	1.3	
I_{ON}	On Leakage Current (AX)	V_{DD} = 3.6 V, V_{AX} = 0 V or V_{DD}, V_{OUT} = Float	−0.1		+0.1	μA
I_{OFF}	Off Leakage Current (AX/BX/CX)	V_{DD} = 3.6 V, V_{IN} = 0 V or V_{DD}, V_{OUT} = V_{DD} or 0 V	−0.1		+0.1	μA
DATA PATH (LEDAX TO LEDBX, LEDCX PINS) DC ELECTRICAL CHARACTERISTICS FOR 10/100 BASE−T ETHERNET SWITCHING						
R_{ON}	Switch On−Resistance (Note 3)	V_{DD} = Min, 1.25 V < V_{IN} < V_{DD}, I_{TN} = −10 mA to −30 mA		7.0	16	Ω
$R_{FLAT(ON)}$	On−Resistance Flatness (Note 3)	V_{DD} = Min, 1.25 V < V_{IN} < V_{DD}, I_{TN} = −10 mA to −30 mA		0.3		
ΔR_{ON}	On−Resistance match from center ports to any other port (Note 3)	V_{DD} = Min, 1.25 V < V_{IN} < V_{DD}, I_{TN} = −10 mA to −30 mA		0.8	1.25	
I_{ON}	On Leakage Current (LEDAX)	V_{DD} = 3.6 V, V_{AX} = 0 V or V_{DD}, V_{OUT} = Float	−0.1		+0.1	μA
I_{OFF}	Off Leakage Current (LEDAX/LEDBX/LEDCX)	V_{DD} = 3.6 V, V_{IN} = 0 V or V_{DD}, V_{OUT} = V_{DD} or 0 V	−0.1		+0.1	μA
CAPACITANCE (AX TO BX, CX AND LEDAX TO LEDBX, LEDCX PINS) (Note 4)						
C_{IN}	Input Capacitance	V_{IN} = 0 V, f = 1 MHz		3.0	4.0	pF
$C_{OFF(B1, B2)}$	Port B Capacitance, Switch OFF			5.0	7.0	
$C_{ON(A/B)}$	A/B Capacitance, Switch ON			10.5	12	
DYNAMIC ELECTRICAL CHARACTERISTICS (AX TO BX AND LEDAX TO LEDBX PINS) (Note 5)						
BW	Bandwidth −3 dB	R_L = 100 Ω (Figure 3)		750		MHz
O_{IRR}	OFF Isolation	R_L = 100 Ω, f = 250 MHz (Figure 7)		−30		dB
XTALK	Crosstalk	R_L = 100 Ω, f = 250 MHz (Figure 8)		−70		
SWITCHING CHARACTERISTICS (AX TO BX AND LEDAX TO LEDBX PINS) (Notes 4 and 5)						
t_{PD}	Propagation Delay (Figure 4)			0.3		ns
t_{PZH}, t_{PZL}	Line Enable Time − SEL to AN, BN (Figure 4)		0.5		15	
t_{PHZ}, t_{PLZ}	Line Disable Time − SEL to AN, BN (Figure 4)		0.5		25	
$t_{SK(o)}$	Output Skew between center port to any other port			0.1	0.2	
$t_{SK(p)}$	Skew between opposite transitions of the same output (t_{Hil}, − t_{PLH})			0.1	0.2	

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3. Measured by the voltage drop between A and B pins at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A & B) pins.
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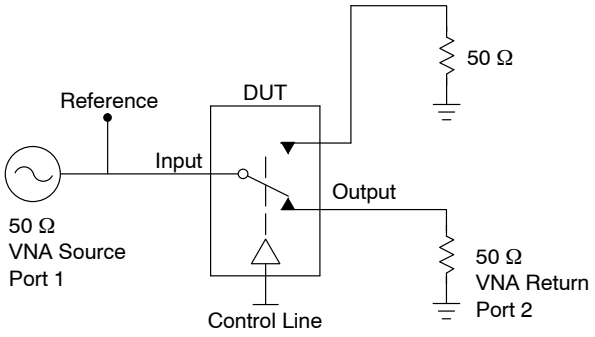


Figure 3. Bandwidth

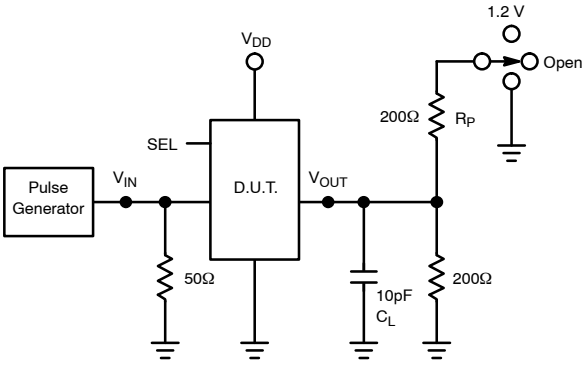


Figure 4. Three−State and t_{pd} Test Setup

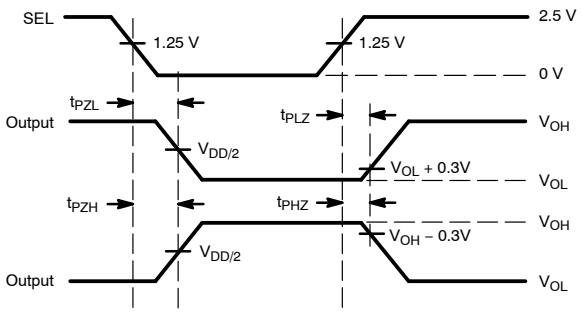


Figure 5. Three−State Timing Diagram

SWITCH POSITIONS

Test	Switch
t_{PLZ}, t_{PZL} (Output on B−Side)	1.2 V
t_{PHZ}, t_{PZH} (Output on B−Side)	GND
t_{PD}	OPEN

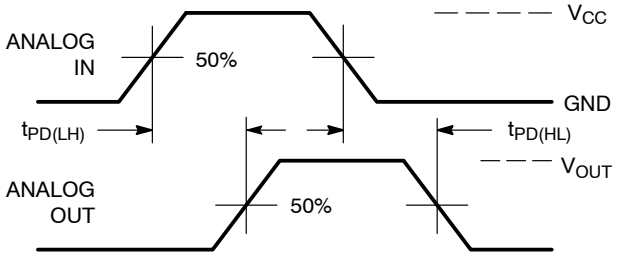


Figure 6. Propagation Delay

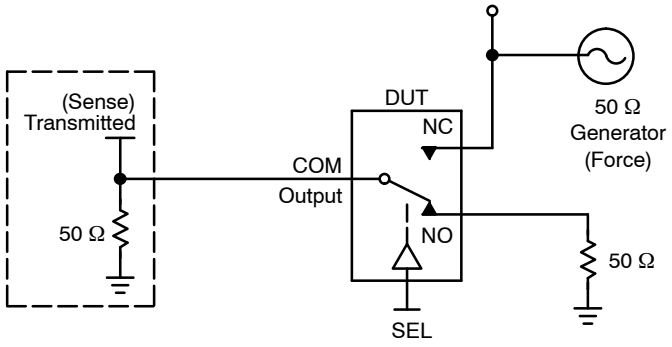
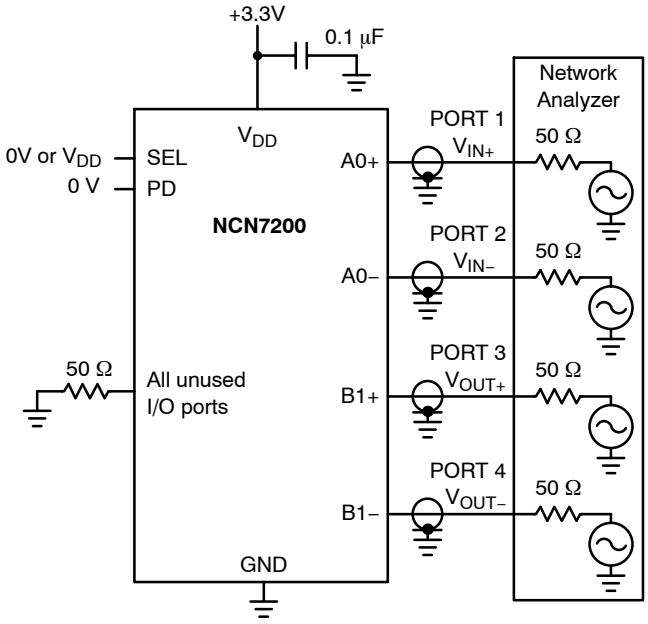


Figure 7. Off−Isolation



$$\text{Differential Crosstalk} = 20\log\left(\frac{V_{OUT+} - V_{OUT-}}{V_{IN+} - V_{IN-}}\right)$$

Measurements are standardized against shorts at IC terminals.
Differential Crosstalk is measured between any two non−adjacent pairs.

Figure 8. Differential Crosstalk

APPLICATION INFORMATION

Logic Inputs

The logic control inputs can be driven up to +3.6 V regardless of the supply voltage. For example, given a +3.3 V supply, the output enables or select pins may be driven low to 0 V and high to 3.6 V: driving the control pins to the rails minimizes power consumption.

Power−Supply Sequencing

Proper power−supply sequencing is advised for all CMOS devices. It is recommended to always apply V_{DD} before applying signals to the input/output or control pins.

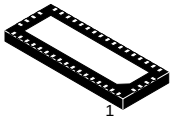
ORDERING INFORMATION

Device	Package	Shipping†
NCN7200MTTWG	WQFN42 (Pb−Free)	2000 / Tape & Reel

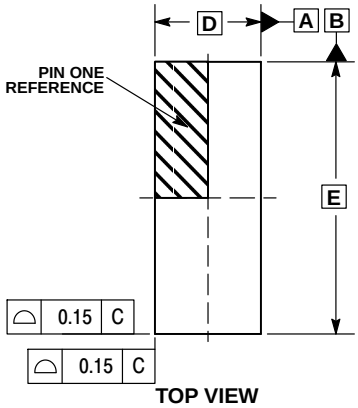
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

WQFN42 3.5x9, 0.5P
CASE 510AP
ISSUE O

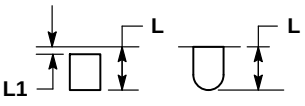
DATE 15 FEB 2010



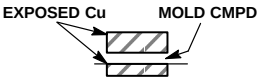
SCALE 2:1



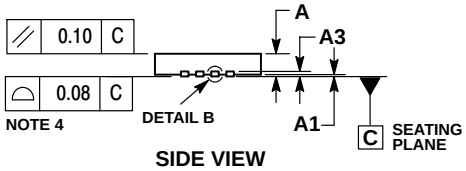
TOP VIEW



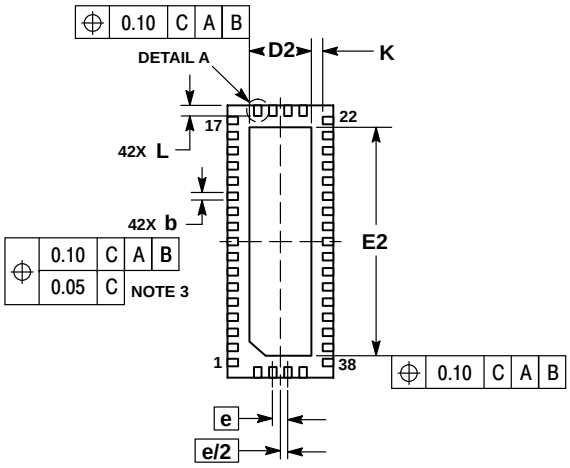
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION



SIDE VIEW

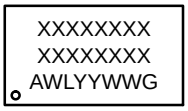


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	3.50 BSC	
D2	1.95	2.15
E	9.00 BSC	
E2	7.45	7.65
e	0.50 BSC	
K	0.20	–––
L	0.30	0.50
L1	0.00	0.15

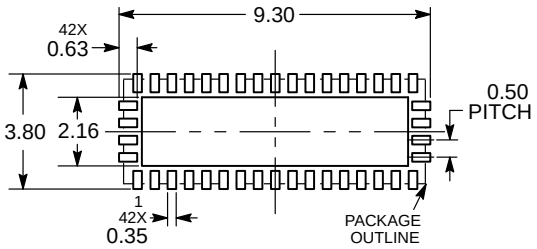
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

DOCUMENT NUMBER:	**98AON48316E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**WQFN42 3.5X9, 0.5P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales