NCP1593A, NCP1593B

Synchronous Buck Regulator

1 MHz, 3 A

The NCP1593 is a fixed 1 MHz, high−output−current, synchronous PWM converter that integrates a low−resistance, high−side P−channel MOSFET and a low−side N−channel MOSFET. The NCP1593 utilizes internally compensated current mode control to provide good transient response, ease of implementation and excellent loop stability. It regulates input voltages from 4.0 V to 5.5 V down to an output voltage as low as 0.6 V and is able to supply up to 3 A of load current.

The NCP1593 includes an internally fixed switching frequency (Fsw), and an internal soft−start to limit inrush current. Other features include cycle−by−cycle current limiting, 100% duty cycle operation, short− circuit protection, power saving mode and thermal shutdown.

Features

- Wide Input Voltage Range: from 4.0 V to 5.5 V
- Internal 90 mΩ High−Side P−Channel MOSFET and 60 mΩ Low−Side N−Channel MOSFET
- Fixed 1 MHz Switching Frequency
- Cycle−by−Cycle Current Limiting
- Hiccup Mode Short−Circuit Protection
- Overtemperature Protection
- Internal Soft−Start
- Start−up with Pre−Biased Output Load
- Adjustable Output Voltage Down to 0.6 V
- Diode Emulation During Light Load
- 100% Duty Cycle Operation to Extend the Battery Life
- These are Pb−Free Devices

Applications

- Set−Top Boxes
- DVD Drives and HDD
- LCD Monitors and TVs
- Cable Modems
- USB Modems
- Telecom/Networking/Datacom Equipment

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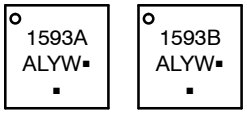
MARKING DIAGRAMS

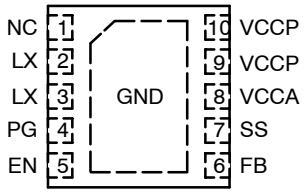
DFN10
CASE 485C



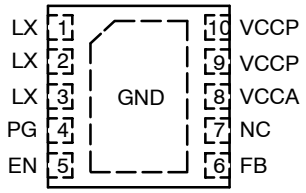
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



NCP1593A
(Top View)



NCP1593B
(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1593AMNTWG	DFN10 (Pb−Free)	3000 / Tape & Reel
NCP1593BMNTWG	DFN10 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

BLOCK DIAGRAM

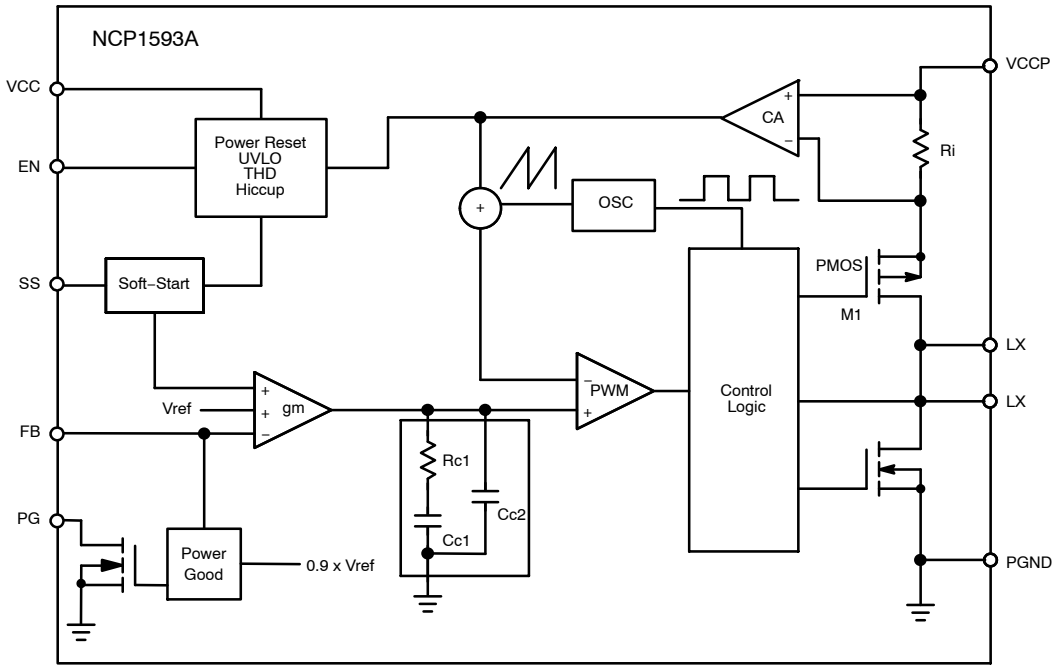


Figure 1. Block Diagram

PIN DESCRIPTIONS

Pin No	Symbol	Description
1	NC / LX	No connect pin for NCP1593A. The user may ground this pin or leave it floating. / LX pin for NCP1593B
2, 3	LX	The drains of the internal MOSFETs. The output inductor should be connected to these pins.
4	PG	Open drain output from the Power Good logic. When the FB voltage is within regulation, this is a high impedance pin. Otherwise it is pulled low.
5	EN	Logic input to enable the part. Logic high to turn on the part and a logic low to shut off the part. An internal pullup forces the part into an enable state when no external bias is present on the pin.
6	FB	Feedback input pin of the Error Amplifier. Connect a resistor divider from the converter's output voltage to this pin to set the converter's regulated voltage.
7	SS / NC	An external capacitor on this pin sets the soft−start ramp time. Leaving this pin open sets the soft−start time at 500 μs. For NCP1593B this pin is a no connect and should be left floating.
8	V_{CC}	Input supply pin for internal bias circuitry. Connect a 0.1 μF ceramic bypass capacitor to this pin. Directly connect the V_{CC} pin to the V_{CCP} pin on the board.
9, 10	V_{CCP}	Input for the power stage
EP	GND	Exposed pad of the package provides both electrical contact to the ground and good thermal contact to the PCB. This pad must be soldered to the PCB for proper operation.

APPLICATION CIRCUIT

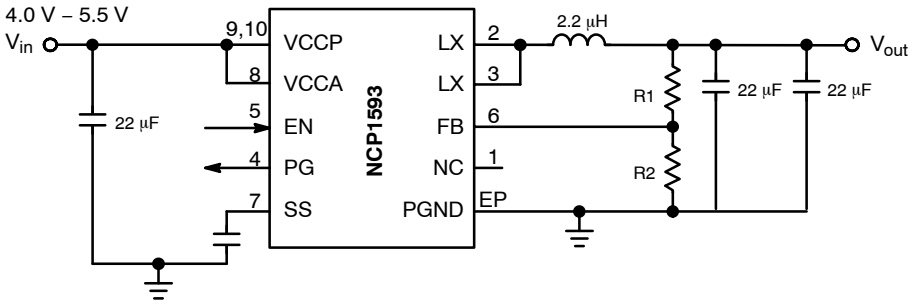


Figure 2. Recommended Application Circuit

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Pin (Pins 8, 9, 10) to GND	V_{in}	6.5 −0.3 (DC) −1.0 (t < 100 ns)	V
LX to GND		V_{in} + 0.7 V_{in} + 1.0 (t < 20 ns) −0.7 (DC) −5.0 (t < 100 ns)	V
All other pins		6.0 −0.3 (DC) −1.0 (t < 100 ns)	V
Operating Ambient Temperature Range (Note 1)	T_A	−40 to +85	°C
Operating Junction Temperature Range (Note 1)	T_J	−40 to +125	°C
Maximum Junction Temperature	$T_{J(MAX)}$	+150	°C
Storage Temperature Range	T_S	−55 to +150	°C
Thermal Resistance Junction−to−Air (Note 2)	$R_{\theta JA}$	68	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

2. $R_{\theta JA}$ measured on approximately 1x1 inch sq. of 1 oz. Copper FR−4 or G−10 board.

ELECTRICAL CHARACTERISTICS (−40°C < T_J < 125°C, V_{CC} = 4.0 V − 5.5 V, for min/max values unless noted otherwise)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.0		5.5	V
V_{CC} UVLO Threshold	V_{UVLO}		2.4	2.5	2.9	V
UVLO Hysteresis	V_{UVLO_hys}			320		mV
V_{CC} Quiescent Current	I_{INVCC}			1.0	1.5	mA
VCCP Quiescent Current	I_{INVCCP}			20	50	μA
Shutdown Supply Current	I_{QSHDN}			1.8	3.0	μA
FEEDBACK VOLTAGE						
Reference Voltage	V_{FB}		0.591	0.6	0.609	V
Reference Voltage	V_{FB}	T_J = 25°C	0.594	0.6	0.606	V
Feedback Input Bias Current	I_{FB}			10	100	nA
Feedback Voltage Line Regulation (Note 3)		V_{CC} = 4.0 V to 5.5 V			−65	dB
PWM						
Maximum Duty Cycle (Regulating)	$d.c._{MAX}$			95		%
Maximum Duty Cycle (LDO mode)	$d.c._{LDO}$	Vout > $d.c._{MAX}$ * V_{IN}			100	%
Minimum Controllable On Time	t_{ONmin}			35		ns
Current Limit						
Cycle-by-cycle Current Limit (Note 3)	I_{LIM}	V_{CC} = 5.0 V, T_J = 25°C		5.1		A
Oscillator						
Switching Frequency	f_{SW}		0.87	1.0	1.13	MHz
MOSFET's						
High-Side MOSFET On Resistance	R_{DSonH}	I_{DS} = 100 mA, V_{IN} = 5.0 V		90	190	mΩ
High-Side MOSFET Leakage	I_{lkgH}	LX = 0 V			10	μA
Low-Side MOSFET On Resistance	R_{DSonL}	I_{DS} = 100 mA, V_{IN} = 5.0 V		60	90	mΩ
Low-Side MOSFET Leakage	I_{lkgL}	LX = 5 V			10	μA
POWER GOOD						
Power Good Rising Threshold	V_{PGH}		0.51	0.54		V
Power Good Falling Threshold	V_{PHL}		0.48	0.51		V
Power Good Hysteresis (High-to-Low)	V_{PGhys}			30		mV
Power Good Pulldown Voltage	V_{RPG}	I_{PG} = 2.5 mA		130	250	mV
ENABLE						
Enable High Threshold	V_{ENHI}		1.4			V
Enable Low Threshold	V_{ENLO}				0.4	V
Enable Hysteresis	V_{ENhys}			200		mV
Enable Pullup Current	I_{EN}			1.4	3.0	μA
Soft-Start						
Default Soft-start Ramp Time	t_{SS}	SS = open; f_{SW} = 1MHz	0.5	0.58	0.65	ms
Maximum Soft-start Ramp time	t_{SS}	SS = max cap; f_{SW} = 1MHz		10		ms
Hiccup Timer				4 * t_{SS}		ms
Soft-start Current	I_{SS}		0.51	0.7	0.87	μA
Thermal Shutdown						
Thermal Shutdown Threshold				185		°C
Thermal Shutdown Hysteresis				30		°C

3. Guaranteed by Characterization.

TYPICAL CHARACTERISTICS

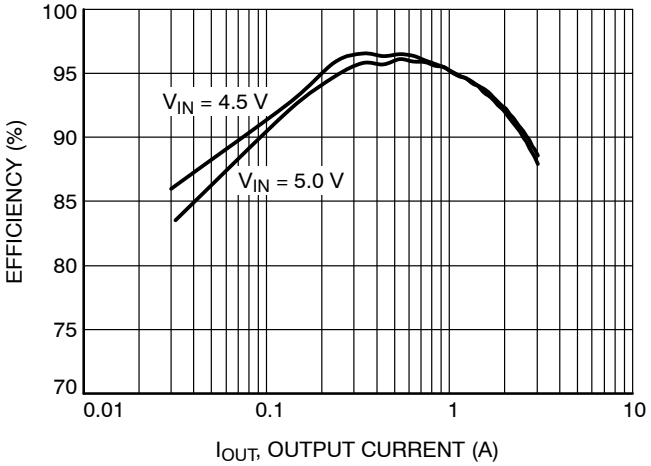


Figure 3. Efficiency vs. Output Current (3.3 V)

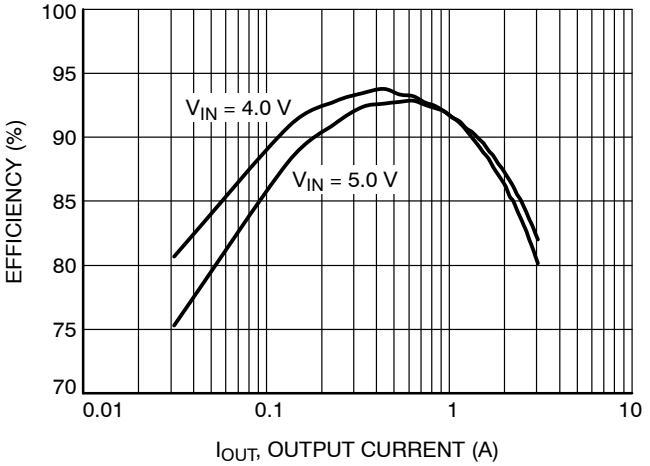


Figure 4. Efficiency vs. Output Current (1.8 V)

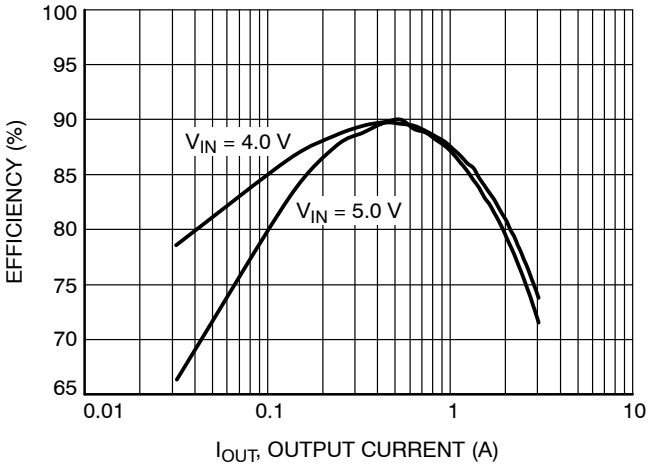


Figure 5. Efficiency vs. Output Current (1.05 V)

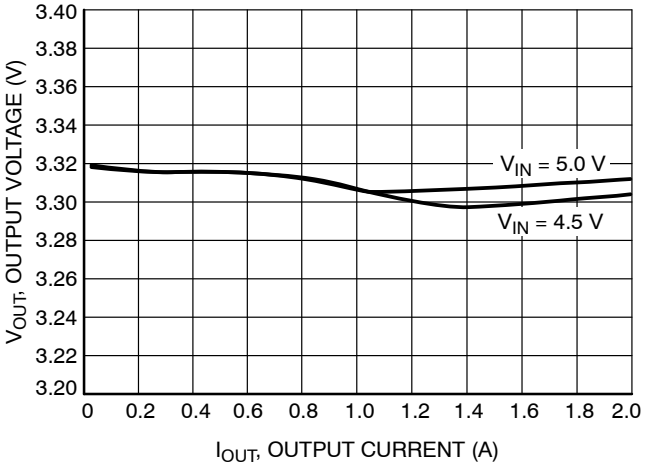


Figure 6. Load Regulation (3.3 V)

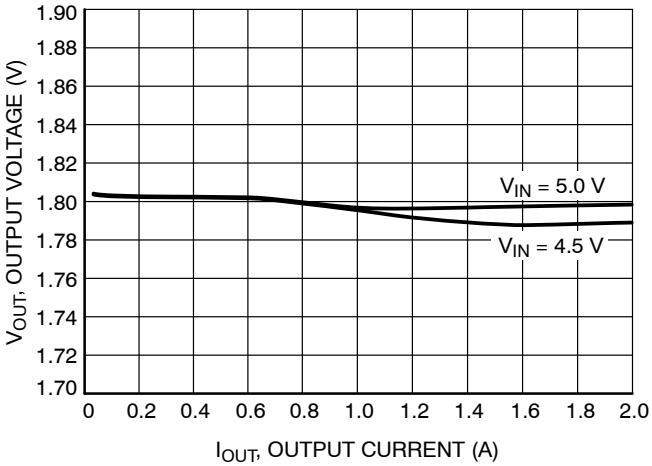


Figure 7. Load Regulation (1.8 V)

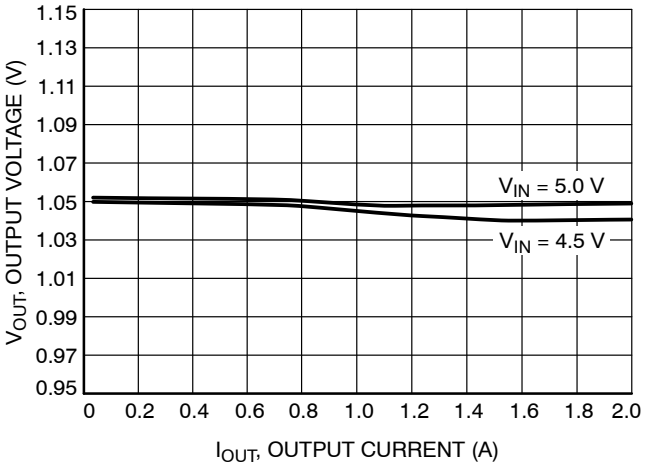


Figure 8. Load Regulation (1.05 V)

TYPICAL CHARACTERISTICS

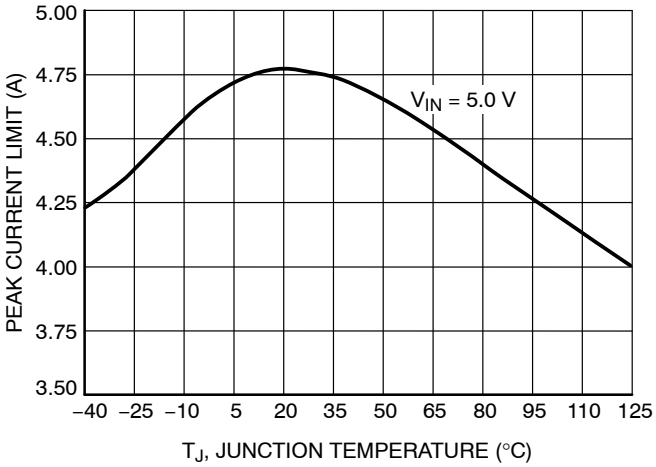


Figure 9. Current Limit vs. Temperature

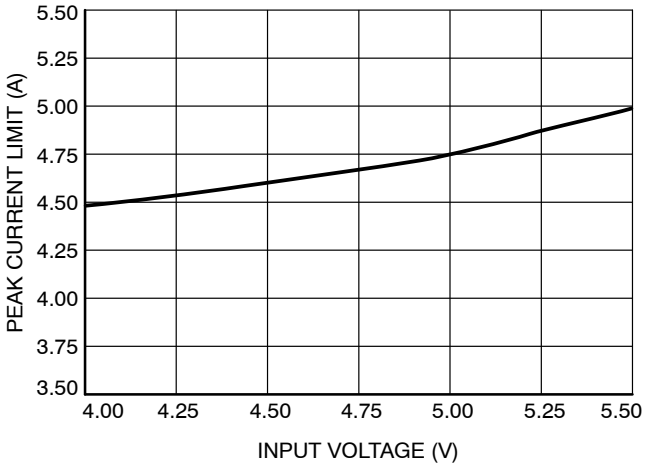


Figure 10. Current Limit vs. Input Voltage

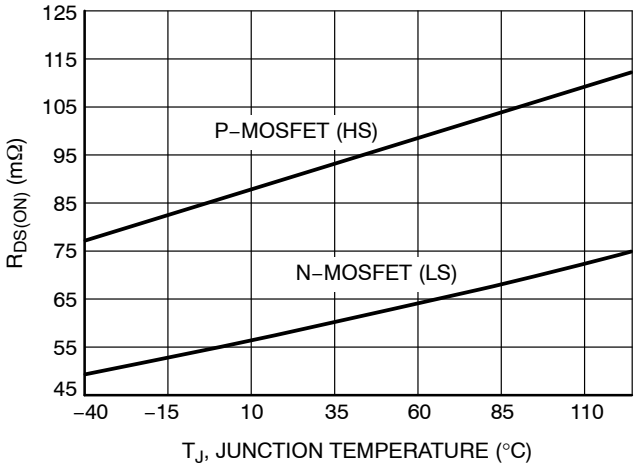
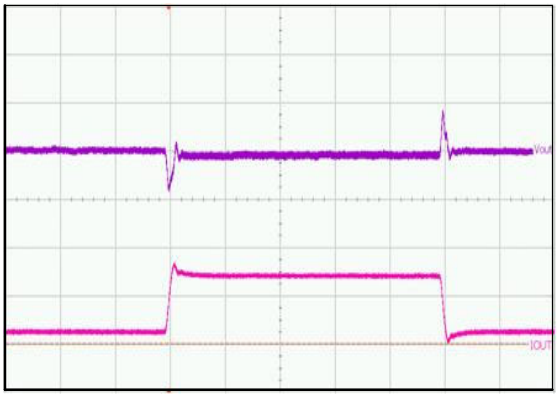
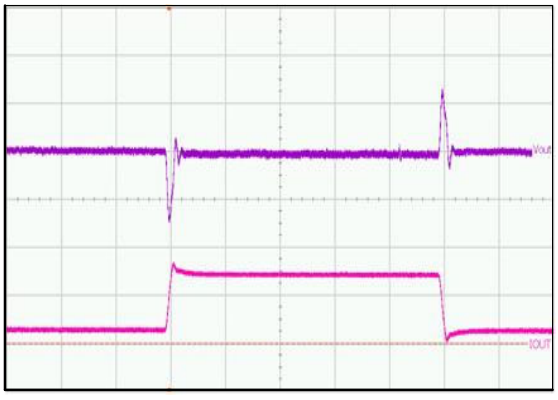


Figure 11. $R_{DS(ON)}$ vs. Temperature



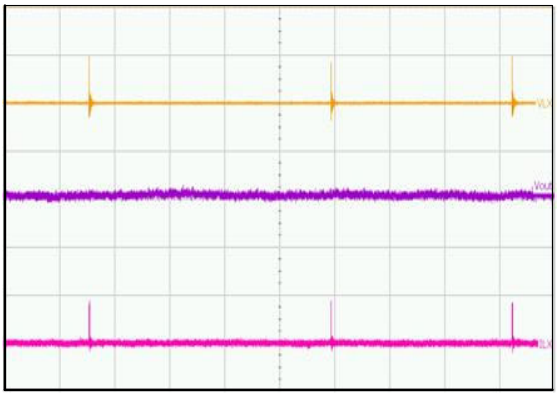
(VIN = 5 V, VOUT = 1.05 V, IOUT = 0.5 A to 3.0 A)
Upper Trace: Output Voltage, 50 mV / div
Lower Trace: Output Current, 2 A / div
Time = 200 μs/div

Figure 12. Load Transient Response



(VIN = 5 V, VOUT = 1.05 V, IOUT = 0.5 A to 3.0 A)
Upper Trace: Output Voltage, 50 mV / div
Lower Trace: Output Current, 2 A / div
Time = 200 μs/div

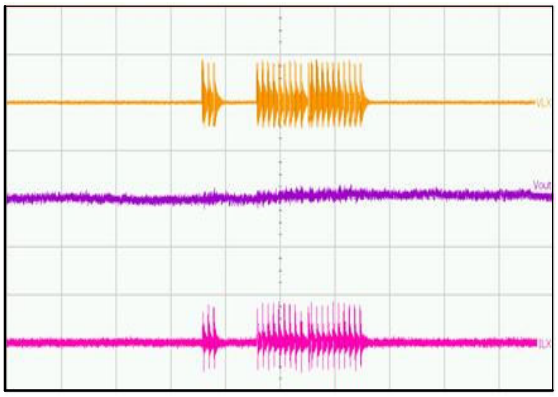
Figure 13. Load Transient Response



(VIN = 5 V, VOUT = 1.05 V, IOUT = 0 A)
Upper Trace: LX Pin Switching Waveforms, 5 V / div
Middle Trace: Output Voltage, 20 mV / div
Lower Trace: Inductor Current, 100 mA / div
Time = 20 μs / div

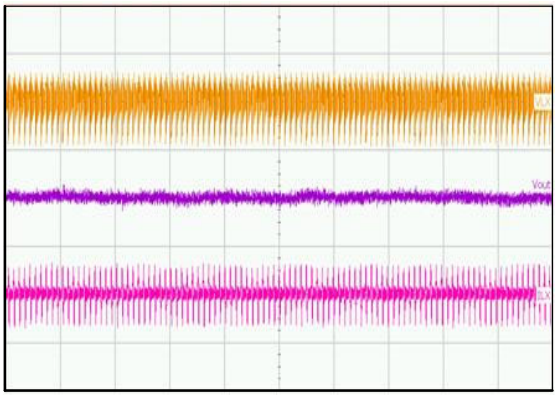
Figure 14. No Load Switching (1.05 V)

TYPICAL CHARACTERISTICS



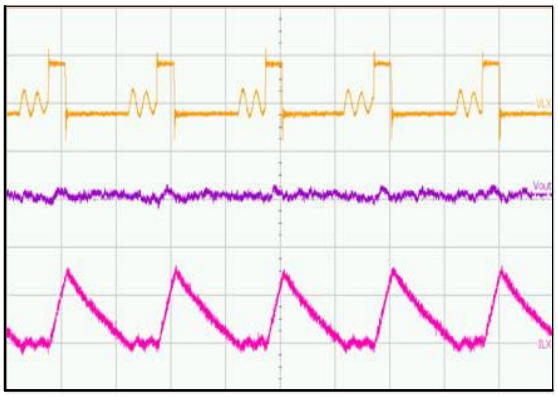
(VIN = 5 V, VOUT = 1.8 V, IOUT = 0 A)
Upper Trace: LX Pin Switching Waveforms, 5 V / div
Middle Trace: Output Voltage, 20 mV / div
Lower Trace: Inductor Current, 100 mA / div
Time = 10 μs / div

Figure 15. No Load Switching (1.8 V)



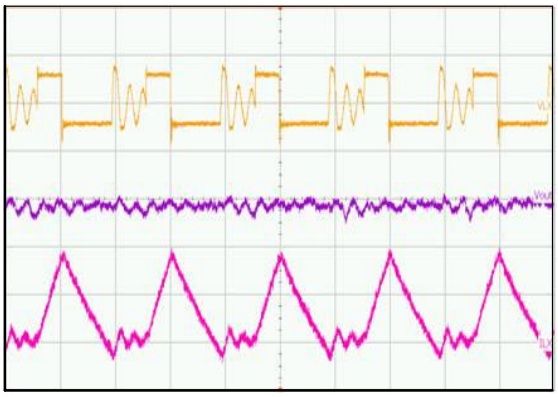
(VIN = 5 V, VOUT = 3.3 V, IOUT = 0 A)
Upper Trace: LX Pin Switching Waveforms, 5 V / div
Middle Trace: Output Voltage, 20 mV / div
Lower Trace: Inductor Current, 200 mA / div
Time = 10 μs / div

Figure 16. No Load Switching (3.3 V)



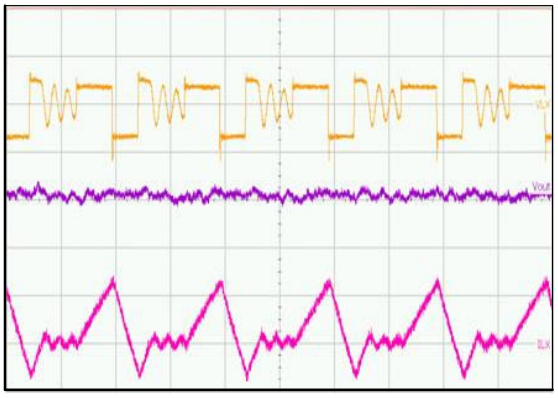
(VIN = 5 V, VOUT = 1.05 V, IOUT = 100 mA)
Upper Trace: LX Pin Switching Waveforms, 5 V / div
Middle Trace: Output Voltage, 20 mV / div
Lower Trace: Inductor Current, 200 mA / div
Time = 500 ns / div

Figure 17. DCM Switching (1.05 V)



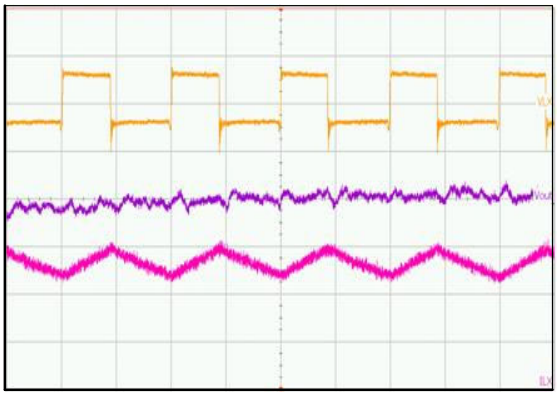
(VIN = 5 V, VOUT = 1.8 V, IOUT = 150 A)
Upper Trace: LX Pin Switching Waveforms, 5 V / div
Middle Trace: Output Voltage, 20 mV / div
Lower Trace: Inductor Current, 200 mA / div
Time = 500 ns / div

Figure 18. DCM Switching (1.8 V)



(VIN = 5 V, VOUT = 3.3 V, IOUT = 100 mA)
Upper Trace: LX Pin Switching Waveforms, 5 V / div
Middle Trace: Output Voltage, 20 mV / div
Lower Trace: Inductor Current, 200 mA / div
Time = 500 ns / div

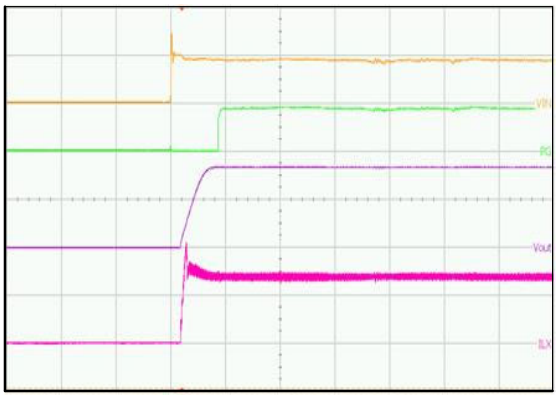
Figure 19. DCM Switching (3.3 V)



(VIN = 5 V, VOUT = 1.8 V, IOUT = 3 A)
Upper Trace: LX Pin Switching Waveforms, 5 V / div
Middle Trace: Output Voltage, 20 mV / div
Lower Trace: Inductor Current, 2 A / div
Time = 500 ns / div

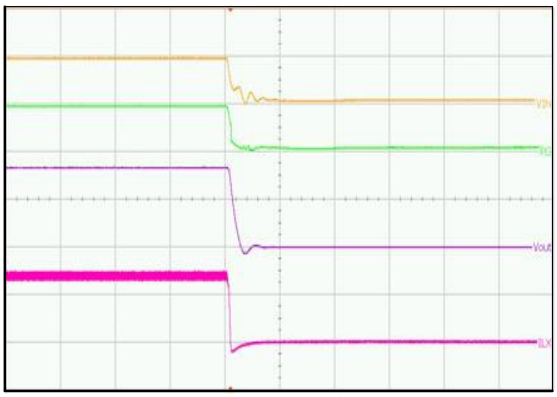
Figure 20. CCM Switching (1.8 V)

TYPICAL CHARACTERISTICS



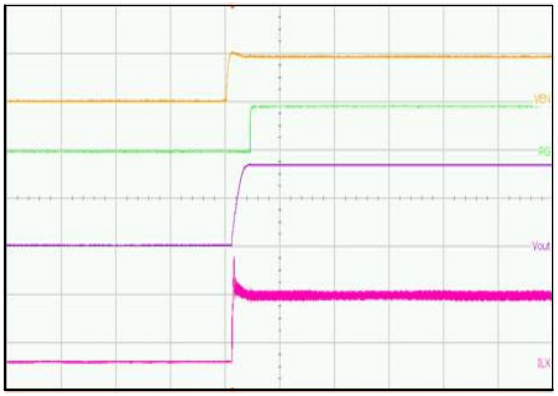
(VIN = 5 V, VOUT = 1.8 V, IOUT = 3 A)
Upper Trace: Input Voltage, 5 V / div
Second Trace: Power Good Pin Voltage, 5 V / div
Third Trace: Output Voltage, 2 V / div
Lower Trace: Inductor Current, 2 A / div
Time = 1 ms / div

Figure 21. Power On from Input Voltage



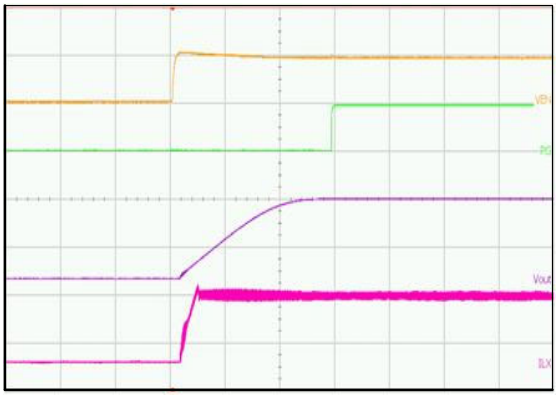
(VIN = 5 V, VOUT = 1.8 V, IOUT = 3 A)
Upper Trace: Input Voltage, 5 V / div
Second Trace: Power Good Pin Voltage, 5 V / div
Third Trace: Output Voltage, 2 V / div
Lower Trace: Inductor Current, 2 A / div
Time = 200 μs / div

Figure 22. Power Off from Input Voltage



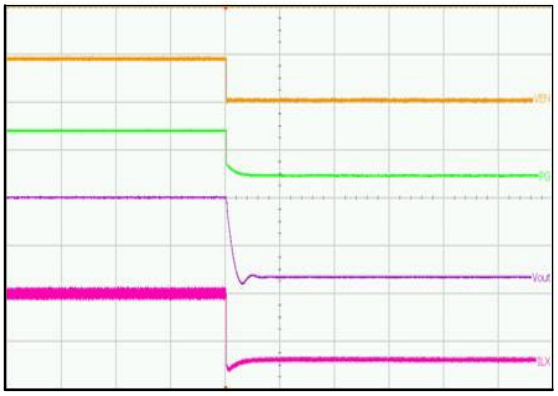
(VIN = 5 V, VOUT = 1.8 V, IOUT = 3 A, no CSS)
Upper Trace: Enable Pin Voltage, 5 V / div
Second Trace: Power Good Pin Voltage, 5 V / div
Third Trace: Output Voltage, 2 V / div
Lower Trace: Inductor Current, 2 A / div
Time = 2 ms / div

Figure 23. Power On from Enable



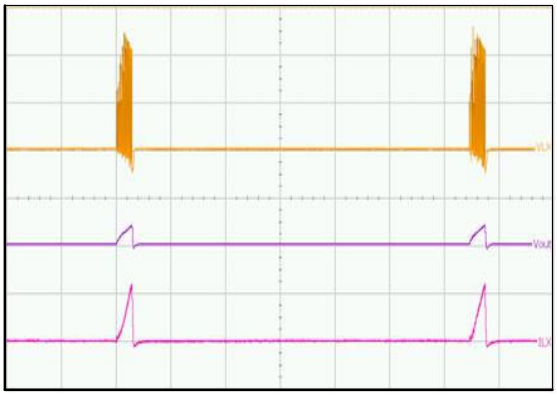
(VIN = 5 V, VOUT = 1.8 V, IOUT = 3 A, CSS = 4.7 nF)
Upper Trace: Enable Pin Voltage, 5 V / div
Second Trace: Power Good Pin Voltage, 5 V / div
Third Trace: Output Voltage, 2 V / div
Lower Trace: Inductor Current, 2 A / div
Time = 2 ms / div

Figure 24. Power On from Enable CSS = 4.7 n



(VIN = 5 V, VOUT = 1.8 V, IOUT = 3 A)
Upper Trace: Enable Pin Voltage, 5 V / div
Second Trace: Power Good Pin Voltage, 5 V / div
Third Trace: Output Voltage, 2 V / div
Lower Trace: Inductor Current, 2 A / div
Time = 200 μs / div

Figure 25. Power Off from Enable



(VIN = 5 V, VOUT = 1.8 V, IOUT = Current Limit, no CSS)
Upper Trace: LX Pin Voltage, 5 V / div
Middle Trace: Output Voltage, 2 V / div
Lower Trace: Inductor Current, 2 A / div
Time = 500 μs / div

Figure 26. Short Circuit Operation

DETAILED DESCRIPTION

Overview

The NCP1593 is a synchronous PWM controller that incorporates all the control and protection circuitry necessary to satisfy a wide range of applications. The NCP1593 employs current mode control to provide fast transient response, simple compensation, and excellent stability. The features of the NCP1593 include a precision reference, fixed 1 MHz switching frequency, a transconductance error amplifier, an integrated high−side P−channel MOSFET and low−side N−Channel MOSFET, internal soft−start, and very low shutdown current. The protection features of the NCP1593 include internal soft−start, pulse−by−pulse current limit, and thermal shutdown.

Reference Voltage

The NCP1593 incorporates an internal reference that allows output voltages as low as 0.6 V. The tolerance of the internal reference is guaranteed over the entire operating temperature range of the controller. The reference voltage is trimmed using a test configuration that accounts for error amplifier offset and bias currents.

Oscillator Frequency

A fixed precision oscillator is provided. The oscillator frequency range is 1 MHz with $\pm$13% variation.

Transconductance Error Amplifier

The transconductance error amplifier's primary function is to regulate the converter's output voltage using a resistor divider connected from the converter's output to the FB pin of the controller, as shown in the applications schematic. If a Fault occurs, the amplifier's output is immediately pulled to GND and PWM switching is inhibited.

Soft−Start

To limit the startup inrush current, a soft−start circuit is used to ramp up the reference voltage from 0 V to its final value linearly. This soft−start time is internally set to a typical value of 500 μs, or it can be externally adjusted by adding a capacitor (C_{SS}) from the SS pin to GND. The following formulas show how to set the externally adjustable soft-start time. The maximum allowable C_{SS} is 10 nF.

$$t_{SS} = \frac{\left(C_{SS} \times V_{FB}\right)}{I_{SS}} \quad \text{(eq. 1)}$$

Where:

V_{FB}: Reference voltage, typically 0.6 V

I_{SS}: Soft−start current, typically 0.7 μA

Output MOSFETs

The NCP1593 includes low $R_{DS(on)}$, both high−side P−channel and low−side N−channel MOSFETs capable of delivering up to 3.0 A of current. When the controller is disabled or during a Fault condition, the controller's output stage is tri−stated by turning OFF both the upper and lower MOSFETs.

Pulse Width Modulation

A high−speed PWM comparator, capable of pulse widths as low as 35 ns, is included in the NCP1593. The inverting input of the comparator is connected to the output of the error amplifier. The non−inverting input is connected to the the current sense signal. At the beginning of each PWM cycle, the CLK signal sets the PWM flip−flop and the upper MOSFET is turned ON. When the current sense signal rises above the error amplifier's voltage then the comparator will reset the PWM flip−flop and the upper MOSFET will be turned OFF.

Current Sense

The NCP1593 monitors the current in the upper MOSFET. The current signal is required by the PWM comparator and the pulse−by−pulse current limiter.

PROTECTIONS

Undervoltage Lockout (UVLO)

The under voltage lockout feature prevents the controller from switching when the input voltage is too low to power the internal power supplies and reference. Hysteresis is incorporated in the UVLO comparator to prevent resistive drops in the wiring or PCB traces from causing ON/OFF cycling of the controller during heavy loading at power up or power down.

Overcurrent Protection (OCP)

NCP1593 detects high side switch current and then compares to a voltage level representing the overcurrent threshold limit. If the current through the high side FET exceeds the overcurrent threshold limit for seven consecutive switching cycles, overcurrent protection is triggered.

Once the overcurrent protection occurs, hiccup mode engages. First, hiccup mode, turns off both FETs and discharges the internal compensation network at the output of the OTA. Next, the IC waits typically 4 x t_{SS} ms and then resets the overcurrent counter. After this reset, the circuit attempts another normal soft−start. Hiccup mode reduces input supply current and power dissipation during a short circuit. It also allows for much improved system up−time, allowing auto−restart upon removal of a temporary short−circuit.

Pre−Bias Startup

In some applications the controller will be required to start switching when it's output capacitors are charged anywhere from slightly above 0 V to just below the regulation voltage. This situation occurs for a number of reasons: the converter's output capacitors may have residual charge on them or the converter's output may be held up by a low current standby power supply. NCP1593 supports pre−bias start up by holding off switching off until the soft start ramp reaches the FB Pin voltage.

Power Good

Power Good (PG) is an open-drain output that requires a pull−up resistor. It is actively held low in soft−start, standby, and shutdown. PG releases when the FB voltage and thus the output voltage rises above 90% of nominal regulation point. The PG goes low when the FB voltage falls below 85% of the regulation point.

Thermal Shutdown

The NCP1593 protects itself from over heating with an internal thermal monitoring circuit. If the junction temperature exceeds the thermal shutdown threshold both the upper and lower MOSFETs will be shut OFF.

APPLICATION INFORMATION

Programming the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB pin (see Figure 27). So the output voltage is calculated according to Eq.1.

$$V_{out} = V_{FB} \cdot \frac{R_1 + R_2}{R_2} \quad \text{(eq. 2)}$$

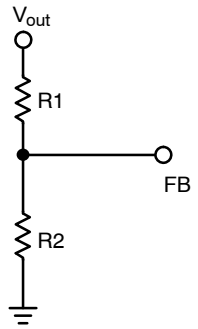


Figure 27. Output divider

Inductor Selection

The inductor is the key component in the switching regulator. The selection of inductor involves trade−offs among size, cost and efficiency. The inductor value is selected according to the equation 2.

$$L = \frac{V_{out}}{f \cdot I_{ripple}} \cdot \left(1 - \frac{V_{out}}{V_{in(max)}}\right) \quad \text{(eq. 3)}$$

Where V_{out} − the output voltage;
f − switching frequency, 1.0 MHz;
I_{ripple} − Ripple current, usually it's 20% − 30% of output current;
$V_{in(max)}$ − maximum input voltage.

Choose a standard value close to the calculated value to maintain a maximum ripple current within 30% of the maximum load current. If the ripple current exceeds this 30% limit, the next larger value should be selected.

The inductor's RMS current rating must be greater than the maximum load current and its saturation current should be about 30% higher. For robust operation in fault conditions (start−up or short circuit), the saturation current should be high enough. To keep the efficiency high, the series resistance (DCR) should be less than 0.1 Ω, and the core material should be intended for high frequency applications.

Output Capacitor Selection

The output capacitor acts to smooth the dc output voltage and also provides energy storage. So the major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is related to capacitance and the ESR. The minimum capacitance required for a certain output ripple can be calculated by Equation 4.

$$C_{OUT(min)} = \frac{I_{ripple}}{8 \cdot f \cdot V_{ripple}} \quad \text{(eq. 4)}$$

Where V_{ripple} is the allowed output voltage ripple.

The required ESR for this amount of ripple can be calculated by equation 5.

$$ESR = \frac{V_{ripple}}{I_{ripple}} \quad \text{(eq. 5)}$$

Based on Equation 3 to choose capacitor and check its ESR according to Equation 4. If ESR exceeds the value from Eq.4, multiple capacitors should be used in parallel.

Ceramic capacitor can be used in most of the applications. In addition, both surface mount tantalum and through−hole aluminum electrolytic capacitors can be used as well.

Input Capacitor Selection

The input capacitor can be calculated by Equation 6.

$$C_{in(min)} = I_{out(max)} \cdot D_{max} \cdot \frac{1}{f \cdot V_{in(ripple)}} \quad \text{(eq. 6)}$$

Where $V_{in(ripple)}$ is the required input ripple voltage.

$$D_{max} = \frac{V_{out}}{V_{in(min)}} \text{ is the maximum duty cycle.} \quad \text{(eq. 7)}$$

Power Dissipation

The NCP1593 is available in a thermally enhanced 10−pin, DFN package. When the die temperature reaches +185°C, the NCP1593 shuts down (see the *Thermal−Overload Protection* section). The power dissipated in the device is the sum of the power dissipated from supply current (PQ), power dissipated due to switching the internal power MOSFET (P_{SW}), and the power dissipated due to the RMS current through the internal power MOSFET (PON). The total power dissipated in the package must be limited so the junction temperature does not exceed its absolute maximum rating of +150°C at maximum ambient temperature. Calculate the power lost in the NCP1593 using the following equations:

1. High side MOSFET

The conduction loss in the top switch is:

$$P_{HSON} = I^2_{RMS\_HSFET} \times R_{DS(on)HS} \quad \text{(eq. 8)}$$

Where:

$$I_{RMS\_FET} = \sqrt{\left(I_{out}^2 + \frac{\Delta I_{PP}^2}{12}\right) \times D} \quad \text{(eq. 9)}$$

ΔI_{PP} is the peak−to−peak inductor current ripple.

The power lost due to switching the internal power high side MOSFET is:

$$P_{HSSW} = \frac{V_{in} \cdot I_{out} \cdot \left(t_r + t_f\right) \cdot f_{SW}}{2} \quad \text{(eq. 10)}$$

t_r and t_f are the rise and fall times of the internal power MOSFET measured at SW node. Typical rise times are 4 ns (rising) and 2 ns (falling).

2. Low side MOSFET

The power dissipated in the top switch is:

$$P_{LSON} = I_{RMS\_LSFET}{}^2 \cdot R_{DS(on)LS} \quad \text{(eq. 11)}$$

Where:

$$I_{RMS\_LSFET} = \sqrt{\left(I_{out}{}^2 + \frac{\Delta I_{PP}{}^2}{12}\right) \cdot (1 - D)} \quad \text{(eq. 12)}$$

ΔI_{PP} is the peak−to−peak inductor current ripple.

The switching loss for the low side MOSFET can be ignored.

The power lost due to the quiescent current (I_Q) of the device is:

$$P_Q = V_{in} \cdot I_Q \quad \text{(eq. 13)}$$

I_Q is the switching quiescent current of the NCP1593.

$$P_{TOTAL} = P_{HSON} + P_{HSSW} + P_{LSON} + P_Q \quad \text{(eq. 14)}$$

Calculate the temperature rise of the die using the following equation:

$$T_J = T_C + \left(P_{TOTAL} \cdot \theta_{JA}\right) \quad \text{(eq. 15)}$$

θ_{JC} is the junction−to−case thermal resistance equal to 68°C/W. T_A is the ambient temperature and TJ is the junction temperature, or die temperature. Solder the underside−exposed pad to a large copper GND plane. If the die temperature reaches the thermal shutdown threshold the NCP1593 shut down and does not restart again until the die temperature cools by 30°C.

Layout Consideration

As with all high frequency switchers, when considering layout, care must be taken in order to achieve optimal electrical, thermal and noise performance. For 1.0MHz switching frequency, switch rise and fall times are typically in few nanosecond range. To prevent noise both radiated and conducted the high speed switching current path must be kept as short as possible. Shortening the current path will also reduce the parasitic trace inductance of approximately 25 nH/inch. At switch off, this parasitic inductance produces a flyback spike across the NCP1593 switch. When operating at higher currents and input voltages, with poor layout, this spike can generate voltages across the NCP1593 that may exceed its absolute maximum rating. A ground plane should always be used under the switcher circuitry to prevent interplane coupling and overall noise.

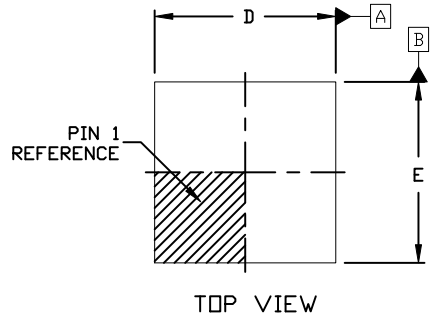
The FB component should be kept as far away as possible from the switch node. The ground for these components should be separated from the switch current path. Failure to do so will result in poor stability or subharmonic like oscillation.

Board layout also has a significant effect on thermal resistance. Reducing the thermal resistance from ground pin and exposed pad onto the board will reduce die temperature and increase the power capability of the NCP1593. This is achieved by providing as much copper area as possible around the exposed pad. Adding multiple thermal vias under and around this pad to an internal ground plane will also help. Similar treatment to the inductor pads will reduce any additional heating effects.

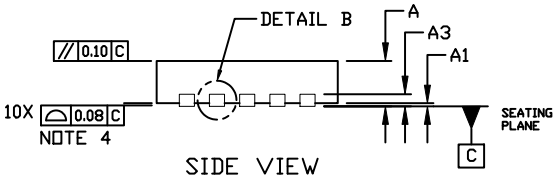
DFN10, 3x3, 0.5P
CASE 485C
ISSUE F

DATE 16 DEC 2021

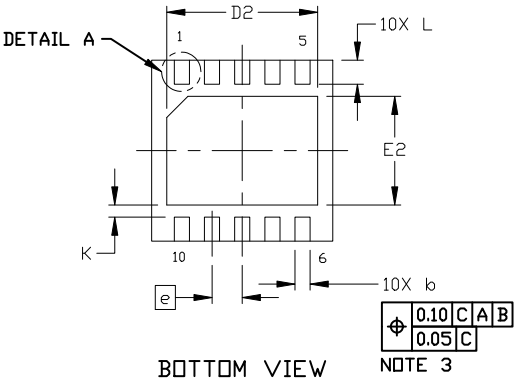
SCALE 2:1



TOP VIEW

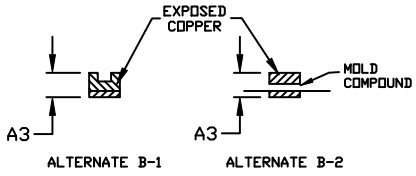


SIDE VIEW

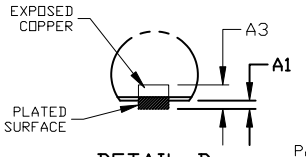


BOTTOM VIEW

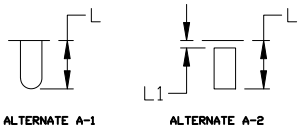
NOTES:
1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.



DETAIL B
ALTERNATE CONSTRUCTION

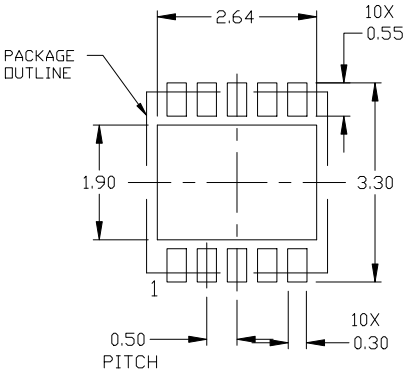


DETAIL B
WETTABLE FLANK
CONSTRUCTION



DETAIL A
ALTERNATE CONSTRUCTION

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3		0.20 REF	
b	0.18	0.23	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e		0.50 BSC	
K		0.20 REF	
L	0.30	0.40	0.50
L1	---	---	0.03



RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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