

# Micro-stepping Motor Driver

## NCV70514

### Description

The NCV70514 is a micro-stepping stepper motor driver for bipolar stepper motors. The chip is connected through I/O pins and an SPI interface with an external microcontroller. The NCV70514 contains a current-translation table and takes the next micro-step depending on the clock signal on the “NXT” input pin and the status of the “DIR” (= direction) register or input pin. The chip provides an error message if stall, an electrical error, an under-voltage or an elevated junction temperature is detected. It is using a proprietary PWM algorithm for reliable current control.

NCV70514 is fully compatible with the automotive voltage requirements and is ideally suited for general-purpose stepper motor applications in the automotive, industrial, medical, and marine environment.

Due to the technology, the device is especially suited for use in applications with fluctuating battery supplies.

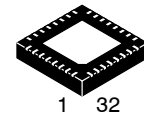
### Features

- Dual H-bridge for 2-phase Stepper Motors
- Programmable Peak-current up to 800 mA
- Low Temperature Boost Current  
(available only for NCV70514MW007 device)
- On-chip Current Translator
- SPI Interface with Daisy Chain Capability
- 7 Step Modes from Full-step up to 32 Micro-steps
- Fully Integrated Current-sensing and Current-regulation
- On Chip Stall Detection
- PWM Current Control with Automatic Selection of Fast and Slow Decay
- Fixed PWM Frequency
- Active Fly-back Diodes
- Full Output Protection and Diagnosis
- Thermal Warning and Shutdown
- Compatible with 3.3 V Microcontrollers, 5 V Tolerant Inputs, 5 V Tolerant Open Drain Outputs

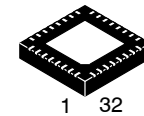
- Reset Function
- Overcurrent Protection
- Enhanced Under Voltage Management
- Step Mode Selection Inputs
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Small Positioning Applications
- Automotive (headlamp alignment, HVAC, idle control, cruise control)
- Industrial Equipment (lighting, fluid control, labeling, process control, XYZ tables, robots)
- Building Automation (HVAC, surveillance, satellite dish, renewable energy systems)

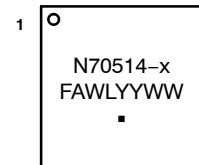


QFN32, 5x5  
CASE 488AM



QFNW32, 5x5  
CASE 484AB

### MARKING DIAGRAM



N70514 = Specific Device Code  
 F = Fab Location  
 A = Assembly Location  
 WL = Wafer Lot  
 YY = Year  
 WW = Work Week  
 ■ = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 32 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 32.

# NCV70514

## TYPICAL APPLICATION SCHEMATIC

The application schematic below shows typical connections for applications with low axis counts and/or with software SPI implementation. For applications with many stepper motor drivers, some “minimal wiring” examples are shown at the last sections of this datasheet.

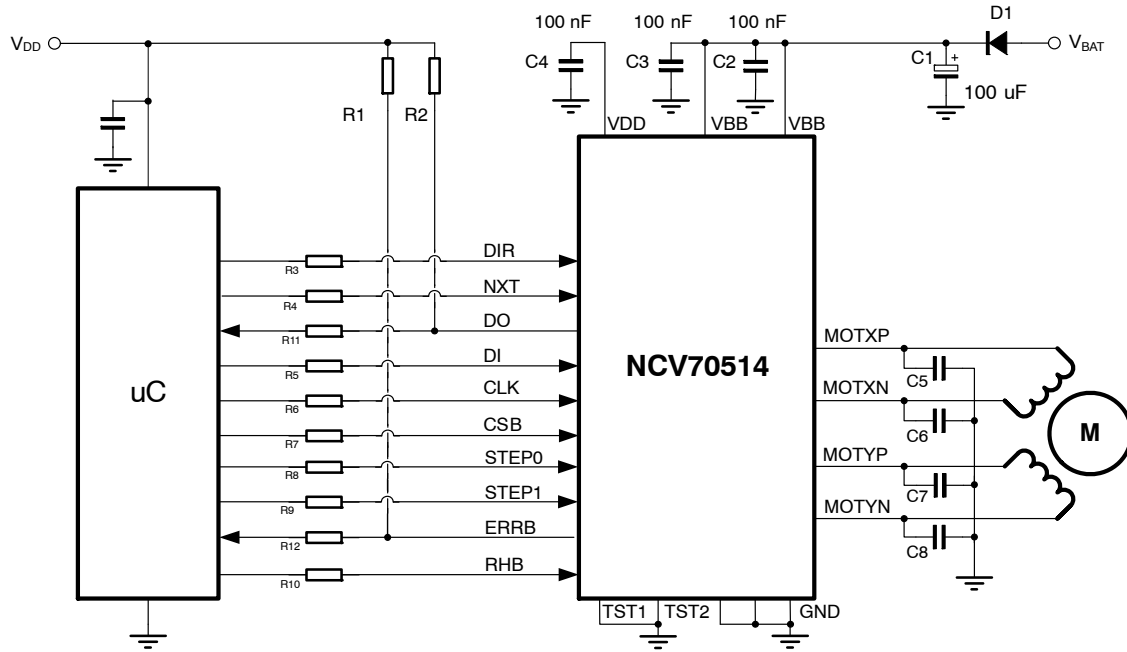


Figure 1. Typical Application Schematic

Table 1. EXTERNAL COMPONENTS

| Component      | Function                                      | Typ. Value    | Max Tolerance | Unit |
|----------------|-----------------------------------------------|---------------|---------------|------|
| C1             | V <sub>BB</sub> buffer capacitor (Note 1)     | 22 ... 100    | ±20%          | μF   |
| C2, C3         | V <sub>BB</sub> decoupling capacitor (Note 2) | 100           | ±20%          | nF   |
| C4             | V <sub>DD</sub> decoupling capacitor (Note 3) | 100           | ±20%          | nF   |
| C5, C6, C7, C8 | Optional EMC filtering capacitor (Note 4)     | 1 ... 3.3 max | ±20%          | nF   |
| R1, R2         | Pull up resistor                              | 1..5          | ±10%          | kΩ   |
| R3 – R10       | Optional resistors                            | 1             | ±10%          | kΩ   |
| R11, R12       | Optional resistors (Note 5)                   | 100           | ±10%          | Ω    |
| D1             | Optional reverse protection diode             | e.g. MURD530  |               |      |

1. Low ESR < 4 Ω, mounted as close as possible to the NCV70514. Total decoupling capacitance value has to be chosen properly to reduce the supply voltage ripple and to avoid EM emission.
2. C2 and C3 must be close to pins V<sub>BB</sub> and coupled GND directly.
3. C4 must be a ceramic capacitor to assure low ESR.
4. Optional capacitors for improvement of EMC and system ESD performance. The slope times on motor pins can be longer than specified in the AC table.
5. Value depends on characteristics of μC inputs for DO and ERRB signals.

# NCV70514

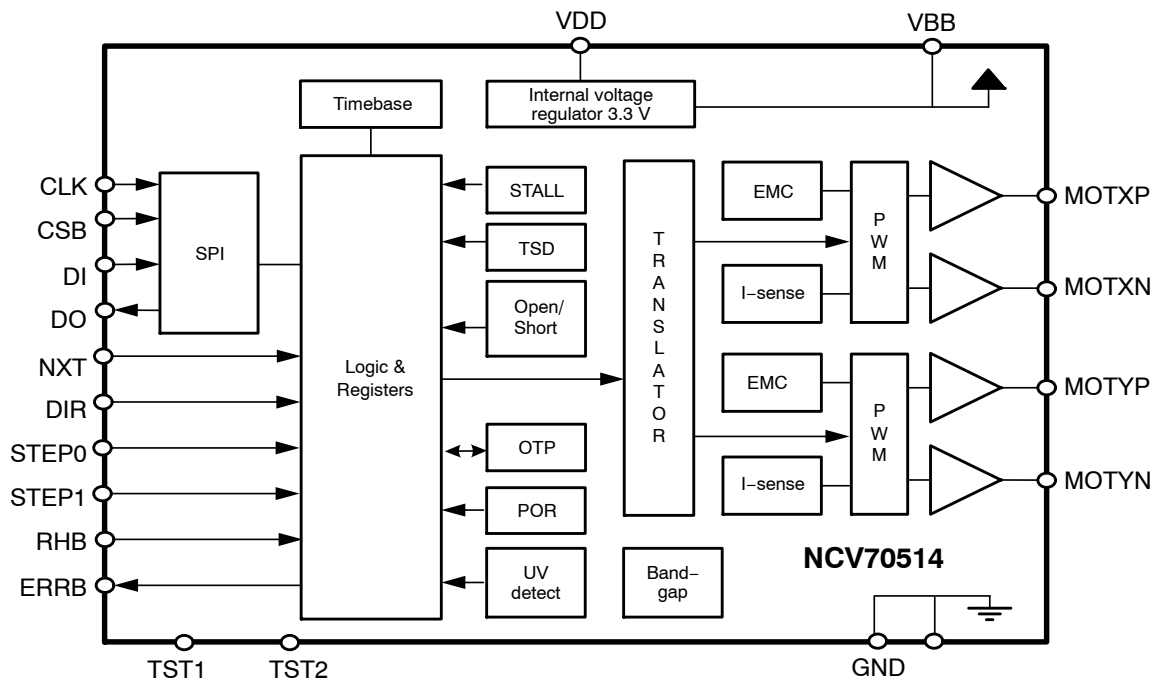


Figure 2. Block Diagram

# NCV70514

## PACKAGE AND PIN DESCRIPTION

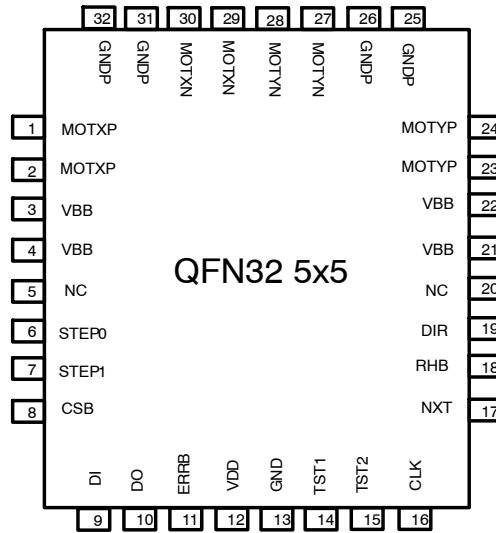


Figure 3. Pin Connections – QFN32 5x5

Table 2. PIN DESCRIPTION

| Pin No.<br>QFN32 5x5 | Pin Name | Description                                               | I/O Type       |
|----------------------|----------|-----------------------------------------------------------|----------------|
| 1, 2                 | MOTXP    | Positive end of phase X coil                              | Driver output  |
| 3, 4, 21, 22         | VBB      | Battery voltage supply                                    | Supply         |
| 5, 20                | NC       | Not Connected                                             |                |
| 6                    | STEP0    | Step mode selection input 0                               | Digital Input  |
| 7                    | STEP1    | Step mode selection input 1                               | Digital Input  |
| 8                    | CSB      | SPI chip select input                                     | Digital Input  |
| 9                    | DI       | SPI data input                                            | Digital Input  |
| 10                   | DO       | SPI data output (Open Drain)                              | Digital Output |
| 11                   | ERRB     | Error Output (Open Drain)                                 | Digital Output |
| 12                   | VDD      | Internal supply (needs external decoupling capacitor)     | Supply         |
| 13                   | GND      | Ground                                                    | Supply         |
| 14                   | TST1     | Test pin input (to be tied to ground in normal operation) | Digital Input  |
| 15                   | TST2     | Test pin input (to be tied to ground in normal operation) | Digital Input  |
| 16                   | CLK      | SPI clock input                                           | Digital Input  |
| 17                   | NXT      | Next micro-step input                                     | Digital Input  |
| 18                   | RHB      | Run/Hold Current selection input                          | Digital Input  |
| 19                   | DIR      | Direction input                                           | Digital Input  |
| 23, 24               | MOTYP    | Positive end of phase Y coil                              | Driver output  |
| 25, 26, 31, 32       | GNDP     | Ground                                                    | Supply         |
| 27, 28               | MOTYN    | Negative end of phase Y coil                              | Driver output  |
| 29, 30               | MOTXN    | Negative end of phase X coil                              | Driver output  |

**Table 3. ABSOLUTE MAXIMUM RATINGS**

| Characteristic                                   | Symbol          | Min  | Max  | Unit |
|--------------------------------------------------|-----------------|------|------|------|
| Supply voltage (Note 6)                          | $V_{BB}$        | -0.3 | +40  | V    |
| Digital input/outputs voltage                    | $V_{IO}$        | -0.3 | +6.0 | V    |
| Junction temperature range (Note 7)              | $T_j$           | -45  | +175 | °C   |
| Storage Temperature (Note 8)                     | $T_{strg}$      | -55  | +160 | °C   |
| HBM Electrostatic discharge voltage (Note 9)     | $V_{esd\_hbm}$  | -2   | +2   | kV   |
| System Electrostatic discharge voltage (Note 10) | $V_{syst\_esd}$ | -8   | +8   | kV   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

6.  $V_{BB}$  Max is +43 V for limited time <0.5 s.

7. The circuit functionality is not guaranteed.

8. For limited time up to 100 hours. Otherwise the max storage temperature is 85°C.

9. HBM according to AEC-Q100: EIA-JESD22-A114-B (100 pF via 1.5 kΩ).

10. System ESD, 150 pF, 330 Ω, contact discharge on the connector pin, unpowered.

Operating ranges define the limits for functional operation and parametric characteristics of the device. A mission profile (Note 11) is a substantial part of the

operation conditions; hence the Customer must contact **onsemi** in order to mutually agree in writing on the allowed missions profile(s) in the application.

**Table 4. RECOMMENDED OPERATING RANGES**

| Characteristic                                                 | Symbol   | Min | Typ | Max  | Unit |
|----------------------------------------------------------------|----------|-----|-----|------|------|
| Battery Supply voltage                                         | $V_{BB}$ | +6  |     | +29  | V    |
| Digital input/outputs voltage                                  | $V_{IO}$ | 0   |     | +5.5 | V    |
| Parametric operating junction temperature range (Notes 12, 14) | $T_{jp}$ | -40 |     | +145 | °C   |
| Functional operating junction temperature range (Notes 13, 14) | $T_{jf}$ | -40 |     | +160 | °C   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

11. A mission profile describes the application specific conditions such as, but not limited to, the cumulative operating conditions over life time, the system power dissipation, the system's environmental conditions, the thermal design of the customer's system, the modes, in which the device is operated by the customer, etc. No more than 100 cumulated hours in life time above  $T_{tw}$ .

12. The parametric characteristics of the circuit are not guaranteed outside the Parametric operating junction temperature range.

13. The maximum functional operating temperature range can be limited by thermal shutdown  $T_{tsd}$ .

14. The cold boost motor current shall be enabled only for ambient temperature below 25°C.

### PACKAGE THERMAL CHARACTERISTIC

The NCV70514 is available in thermally optimized QFN32 5x5 package. For the optimizations, the package has an exposed thermal pad which has to be soldered to the PCB ground plane. The ground plane needs thermal vias to conduct the heat to the bottom layer.

For precise thermal cooling calculations the major thermal resistances of the devices are given. The thermal media to which the power of the devices has to be given are:

- Static environmental air (via the case)

- PCB board copper area (via the device pins and exposed pad)

The major thermal resistances of the device are the  $R_{th}$  from the junction to the ambient ( $R_{thja}$ ) and the  $R_{th}$  from the junction to the exposed pad ( $R_{thjp}$ ).

Using an exposed die pad on the bottom surface of the package is mainly contributing to this performance. In order to take full advantage of the exposed pad, it is most important that the PCB has features to conduct heat away from the package. In the table below, one can find the values for the  $R_{thja}$  and  $R_{thjp}$ :

**Table 5. THERMAL RESISTANCE**

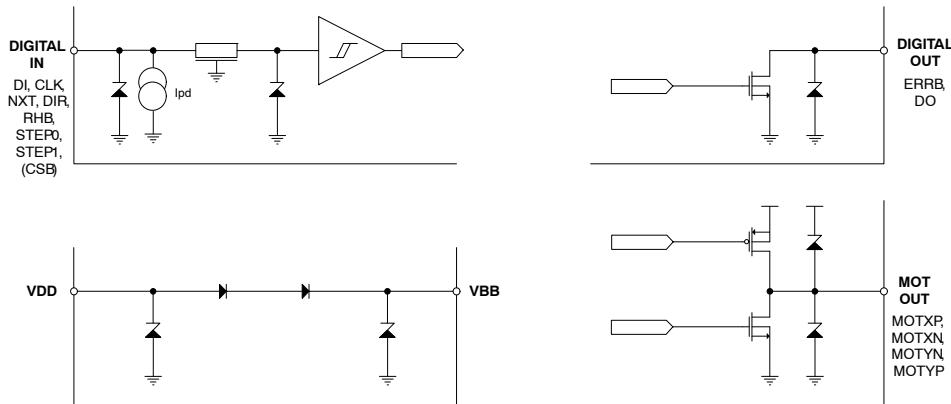
| Package   | $R_{th}$ , Junction-to-Exposed Pad, $R_{thjp}$ | $R_{th}$ , Junction-to-Ambient, $R_{thja}$ (Note 15) |
|-----------|------------------------------------------------|------------------------------------------------------|
| QFN32 5x5 | 15 K/W                                         | 39 K/W                                               |

15. The  $R_{thja}$  for 2S2P simulated for worst case power and following conditions:

- A 4-layer printed circuit board with inner power planes and outer (top and bottom) signal layers is used
- Board thickness is 1.46 mm (FR4 PCB material)
- All four layers: 30  $\mu$ m thick copper with an area of 2500 mm<sup>2</sup> where:
  - Top layer with 70% copper coverage in 20x20 mm around device, rest 40% copper coverage
  - In layer 1 with 70% copper coverage
  - In layer 2 with 98% copper coverage
  - Bottom layer with 90% copper coverage
- The 12 vias in Exposed Pad area, via diameter 0.4 mm
- Gap-filler max 400  $\mu$ m between PCB and heat sink non conductive with worst case thermal conductivity of 1.5 W/mK

### EQUIVALENT SCHEMATICS

The following figure gives the equivalent schematics of the user relevant inputs and outputs. The diagrams are simplified representations of the circuits used.



**Figure 4. Input and Output Equivalent Diagrams**

## ELECTRICAL CHARACTERISTICS

## DC PARAMETERS

The DC parameters are guaranteed over junction temperature from  $-40$  to  $145^{\circ}\text{C}$  and  $V_{\text{BB}}$  in the operating range from 6 to 29 V, unless otherwise specified. Convention: currents flowing into the circuit are defined as positive.

Table 6. DC PARAMETERS

| Symbol                     | Pin(s)                                              | Parameter                                                                 | Test Conditions                                   | Min | Typ | Max | Unit |
|----------------------------|-----------------------------------------------------|---------------------------------------------------------------------------|---------------------------------------------------|-----|-----|-----|------|
| MOTORDRIVER                |                                                     |                                                                           |                                                   |     |     |     |      |
| I <sub>MS-max,Peak</sub>   | MOTXP<br>MOTXN<br>MOTYP<br>MOTYN                    | Max current through motor coil in normal operation                        | V <sub>BB</sub> = 14 V                            |     | 800 |     | mA   |
| I <sub>MSabs</sub>         |                                                     | Absolute error on coil current (Note 16)                                  | V <sub>BB</sub> = 14 V,<br>T <sub>j</sub> = 145°C | -10 |     | 10  | %    |
| I <sub>MSrel</sub>         |                                                     | Matching of X & Y coil currents (Note 16)                                 | V <sub>BB</sub> = 14 V                            | -7  |     | 7   | %    |
| R <sub>DS(on)</sub>        |                                                     | On resistance of High side + Low side Driver at the highest current range | T <sub>j</sub> ≤ 25°C                             |     |     | 1.8 | Ω    |
|                            |                                                     |                                                                           | T <sub>j</sub> = 145°C                            |     |     | 2.4 | Ω    |
| R <sub>mpd</sub>           |                                                     | Motor pin pull-down resistance                                            | HiZ mode                                          |     | 70  |     | kΩ   |
| LOGIC INPUTS               |                                                     |                                                                           |                                                   |     |     |     |      |
| V <sub>inL</sub>           | DI, CLK,<br>NXT,<br>DIR,<br>RHB,<br>STEP0,<br>STEP1 | Logic low input level, max                                                | T <sub>j</sub> = 145°C                            |     |     | 0.8 | V    |
| V <sub>inH</sub>           |                                                     | Logic high input level, min                                               | T <sub>j</sub> = 145°C                            | 2.4 |     |     | V    |
| I <sub>inL</sub>           |                                                     | Logic low input level, max                                                | T <sub>j</sub> = 145°C                            | -1  |     |     | μA   |
| I <sub>inH</sub>           |                                                     | Logic high input level, max                                               | T <sub>j</sub> = 145°C                            | 1   | 2   | 4   | μA   |
| V <sub>inL</sub>           | CSB                                                 | Logic low input level, max                                                | T <sub>j</sub> = 145°C                            |     |     | 0.8 | V    |
| V <sub>inH</sub>           |                                                     | Logic high input level, min                                               | T <sub>j</sub> = 145°C                            | 2.4 |     |     | V    |
| I <sub>inL</sub>           |                                                     | Logic low input level, max (Note 17)                                      | T <sub>j</sub> = 145°C                            | -50 | -30 | -10 | μA   |
| I <sub>inH</sub>           |                                                     | Logic high input level, max (Note 17)                                     | T <sub>j</sub> = 145°C                            |     |     | 1   | μA   |
| R <sub>pd</sub>            | TST1                                                | Internal pull-down resistor                                               |                                                   | 3   |     | 9   | kΩ   |
| LOGIC OUTPUTS              |                                                     |                                                                           |                                                   |     |     |     |      |
| V <sub>OLmax</sub>         | DO,<br>ERRB                                         | Output voltage when                                                       | 8 mA sink current                                 |     |     | 0.4 | V    |
| V <sub>OHmax</sub>         |                                                     | Maximum drain voltage                                                     |                                                   |     |     | 5.5 | V    |
| I <sub>OLmax</sub>         |                                                     | Maximum allowed drain current (Note 25)                                   |                                                   |     |     | 12  | mA   |
| THERMAL WARNING & SHUTDOWN |                                                     |                                                                           |                                                   |     |     |     |      |
| T <sub>tw</sub>            |                                                     | Thermal warning (Notes 18 and 19)                                         |                                                   | 136 | 145 | 154 | °C   |
| T <sub>tsd</sub>           |                                                     | Thermal shutdown (Note 20)                                                |                                                   | 156 | 165 | 174 | °C   |

16. Tested in production for 800 mA, 400 mA, 200 mA and 100 mA current settings for both X and Y coil.

17. CSB has an internal weak pull-up resistor of 100 k $\Omega$ .

18. Thermal warning is derived from thermal shutdown ( $T_{\text{tw}} = T_{\text{tsd}} - 20^{\circ}\text{C}$ ).

19. No more than 100 cumulated hours in life time above  $T_{\text{tw}}$ .

20. Parameter guaranteed by trimming relevant OTPs in production test at  $160^{\circ}\text{C}$  and  $V_{\text{BB}} = 14\text{ V}$ .

21. Dynamic current is with oscillator running, all analogue cells active. Coil currents 0 mA, SPI active, ERRB inactive, no floating inputs, TST input tied to GND.

22. All analog cells in power down. Logic powered, no clocks running. All outputs unloaded, no floating inputs.

23. Pin VDD must not be used for any external supply.

24. The SPI registers content will not be altered above this voltage.

25. Maximum allowed drain current that the output can withstand without getting damaged. Not tested in production.

Table 6. DC PARAMETERS

| Symbol                                       | Pin(s)          | Parameter                                         | Test Conditions                                 | Min | Typ   | Max | Unit |
|----------------------------------------------|-----------------|---------------------------------------------------|-------------------------------------------------|-----|-------|-----|------|
| SUPPLY AND VOLTAGE REGULATOR                 |                 |                                                   |                                                 |     |       |     |      |
| UV <sub>3</sub>                              | V <sub>BB</sub> | H-Bridge off voltage low threshold                |                                                 |     | 5.98  |     | V    |
| UV <sub>1</sub><br>UV <sub>2</sub>           |                 | Under voltage low threshold                       | UVxThr[3:0] = 0000                              |     | 5.98  |     | V    |
|                                              |                 |                                                   | UVxThr[3:0] = 1111                              |     | 10.96 |     | V    |
| UV <sub>1_STEP</sub><br>UV <sub>2_STEP</sub> |                 | Under voltage low threshold step                  | Between two UVxThr codes                        |     | 0.33  |     | V    |
| UV <sub>X_ACC</sub>                          |                 | Under voltage low threshold accuracy              |                                                 | -4  |       | 4   | %    |
| UV <sub>X_HYST</sub>                         |                 | Under voltage hysteresis                          |                                                 | 30  | 150   | 310 | mV   |
| I <sub>bat</sub>                             |                 | Total current consumption (Note 21)               | Unloaded outputs<br>V <sub>BB</sub> = 29 V      |     | 4     | 15  | mA   |
| I <sub>bat_s</sub>                           |                 | Sleep mode current consumption (Note 22)          | V <sub>BB</sub> = 5.5 V & 18 V                  |     | 90    | 150 | μA   |
| V <sub>DD</sub>                              | V <sub>DD</sub> | Regulated internal supply (Note 23)               | 5.5 V < V <sub>BB</sub> < 29 V                  | 3.0 | 3.3   | 3.6 | V    |
| V <sub>ddReset</sub>                         |                 | Digital supply reset level @ power down (Note 24) |                                                 |     |       | 3.0 | V    |
| I <sub>ddLim</sub>                           |                 | Current limitation                                | Pin shorted to ground<br>V <sub>BB</sub> = 14 V |     |       | 80  | mA   |

16. Tested in production for 800 mA, 400 mA, 200 mA and 100 mA current settings for both X and Y coil.

17. CSB has an internal weak pull-up resistor of 100 kΩ.

18. Thermal warning is derived from thermal shutdown ( $T_{tw} = T_{tsd} - 20^{\circ}\text{C}$ ).

19. No more than 100 cumulated hours in life time above  $T_{tw}$ .

20. Parameter guaranteed by trimming relevant OTPs in production test at 160°C and V<sub>BB</sub> = 14 V.

21. Dynamic current is with oscillator running, all analogue cells active. Coil currents 0 mA, SPI active, ERRB inactive, no floating inputs, TST input tied to GND.

22. All analog cells in power down. Logic powered, no clocks running. All outputs unloaded, no floating inputs.

23. Pin VDD must not be used for any external supply.

24. The SPI registers content will not be altered above this voltage.

25. Maximum allowed drain current that the output can withstand without getting damaged. Not tested in production.

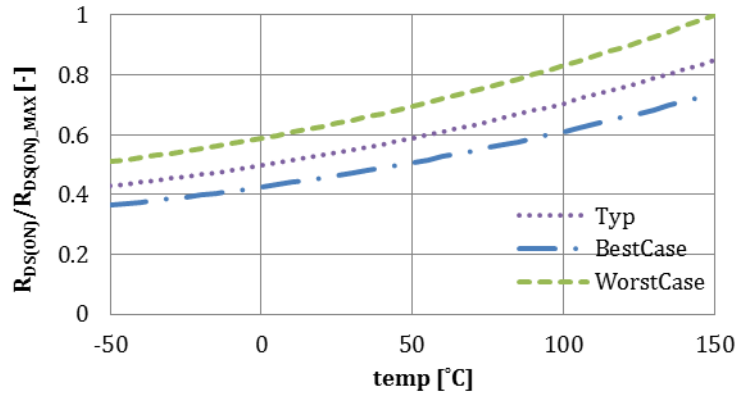


Figure 5. ON Resistance of High Side + Low Side Driver at the Highest Current Range



## AC PARAMETERS

The AC parameters are guaranteed over junction temperature from –40 to 145°C and V<sub>BB</sub> in the operating range from 6 to 29 V, unless otherwise specified.

**Table 7. AC PARAMETERS**

| Symbol                     | Pin(s)                 | Parameter                                                                                                          | Test Conditions                           | Min  | Typ  | Max                       | Unit |
|----------------------------|------------------------|--------------------------------------------------------------------------------------------------------------------|-------------------------------------------|------|------|---------------------------|------|
| INTERNAL OSCILLATOR        |                        |                                                                                                                    |                                           |      |      |                           |      |
| f <sub>osc</sub>           |                        | Frequency of internal oscillator                                                                                   | V <sub>BB</sub> = 14 V                    | 7.2  | 8    | 8.8                       | MHz  |
| MOTORDRIVER                |                        |                                                                                                                    |                                           |      |      |                           |      |
| f <sub>pwm</sub>           | MOTxx                  | PWM frequency                                                                                                      | (Note 26)                                 | 20.5 | 22.8 | 25.1                      | kHz  |
| t <sub>OCdet</sub>         |                        | Open coil detection with PWM=100% (Note 26)                                                                        | SPI bit OpenDet[1:0] = 00                 |      | 5    |                           | ms   |
|                            |                        |                                                                                                                    | SPI bit OpenDet [1:0] = 01                |      | 25   |                           |      |
|                            |                        |                                                                                                                    | SPI bit OpenDet [1:0] = 10                |      | 50   |                           |      |
|                            |                        |                                                                                                                    | SPI bit OpenDet [1:0] = 11                |      | 200  |                           |      |
| t <sub>brise</sub>         |                        | Turn-on transient time, between 10% and 90%, I <sub>MD</sub> = 200 mA, V <sub>BB</sub> = 14 V, 1 nF at motor pins  | SPI bit EMC[1:0] = 00                     |      | 80   |                           | ns   |
|                            |                        |                                                                                                                    | SPI bit EMC[1:0] = 01                     |      | 120  |                           |      |
|                            |                        |                                                                                                                    | SPI bit EMC[1:0] = 10                     |      | 190  |                           |      |
| t <sub>bfall</sub>         |                        | Turn-off transient time, between 10% and 90%, I <sub>MD</sub> = 200 mA, V <sub>BB</sub> = 14 V, 1 nF at motor pins | SPI bit EMC[1:0] = 00                     |      | 70   |                           | ns   |
|                            |                        |                                                                                                                    | SPI bit EMC[1:0] = 01                     |      | 110  |                           |      |
|                            |                        |                                                                                                                    | SPI bit EMC[1:0] = 10                     |      | 180  |                           |      |
| DIGITAL OUTPUTS            |                        |                                                                                                                    |                                           |      |      |                           |      |
| t <sub>H2L</sub>           | DO, ERRB               | Output fall-time (90% to 10%) from V <sub>InH</sub> to V <sub>InL</sub>                                            | Capacitive load 200 pF and pull-up 1.5 kΩ |      |      | 50                        | ns   |
| HARD RESET FUNCTION        |                        |                                                                                                                    |                                           |      |      |                           |      |
| t <sub>hr_trig</sub>       | DIR                    | Hard reset trigger time (Note 26)                                                                                  | See hard reset function                   | 20   |      | 200                       | μs   |
| t <sub>hr_dir</sub>        |                        | Hard reset DIR pulse width                                                                                         | (Note 26)                                 | 2.5  |      | t <sub>hr_trig</sub> -2.5 | μs   |
| t <sub>hr_set</sub>        | RHB                    | RHB set-up time                                                                                                    | (Note 26)                                 | 5    |      |                           | ms   |
| t <sub>hr_err</sub>        | ERRB                   | Hard reset error indication                                                                                        | (Note 26)                                 |      | 2    |                           | ms   |
| t <sub>csb_width</sub>     | CSB                    | CSB wake-up low pulse width                                                                                        | (Note 26)                                 | 1    |      | 150                       | μs   |
| t <sub>wu</sub>            |                        | Wake-up time                                                                                                       | See Sleep Mode                            | 250  |      |                           | μs   |
| NXT/DIR/STEP0/STEP1 INPUTS |                        |                                                                                                                    |                                           |      |      |                           |      |
| t <sub>NXT_HI</sub>        | NXT                    | NXT minimum, high pulse width                                                                                      |                                           | 2    |      |                           | μs   |
| t <sub>NXT_LO</sub>        |                        | NXT minimum, low pulse width                                                                                       |                                           | 2    |      |                           | μs   |
| f <sub>NXT</sub>           | NXT                    | NXT max repetition rate                                                                                            |                                           |      |      | f <sub>PWM</sub> /2       | kHz  |
| t <sub>CSB_LO_WIDTH</sub>  |                        | NXT pin trigger after SPI NXT command                                                                              |                                           | 1    |      |                           | μs   |
| t <sub>DIR_SET</sub>       | NXT, DIR, STEP0, STEP1 | NXT hold time, following change of DIR, STEP0 or STEP1                                                             |                                           | 25   |      |                           | μs   |
| t <sub>DIR_HOLD</sub>      |                        | NXT hold time, before change of DIR, STEP0 or STEP1                                                                |                                           | 25   |      |                           | μs   |

26. Derived from the internal oscillator

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 8. SPI INTERFACE

| Symbol             | Parameter                                                    | Min | Typ | Max | Unit    |
|--------------------|--------------------------------------------------------------|-----|-----|-----|---------|
| $t_{CLK}$          | SPI clock period                                             | 1   |     |     | $\mu s$ |
| $t_{HI\_CLK}$      | SPI clock high time                                          | 200 |     |     | ns      |
| $t_{CLKRISE}$      | SPI clock rise time                                          |     |     | 1   | $\mu s$ |
| $t_{CLKFALL}$      | SPI clock fall time                                          |     |     | 1   | $\mu s$ |
| $t_{LO\_CLK}$      | SPI clock low time                                           | 200 |     |     | ns      |
| $t_{SET\_DI}$      | DI set up time, valid data before rising edge of CLK         | 50  |     |     | ns      |
| $t_{HOLD\_DI}$     | DI hold time, hold data after rising edge of CLK             | 50  |     |     | ns      |
| $t_{HI\_CSB}$      | CSB high time                                                | 2.5 |     |     | $\mu s$ |
| $t_{SET\_CSB\_LO}$ | CSB set up time, CSB low before rising edge of CLK (Note 27) | 1   |     |     | $\mu s$ |
| $t_{CLK\_CSB\_HI}$ | CSB set up time, CSB high after rising edge of CLK           | 200 |     |     | ns      |
| $t_{DEL\_CSB\_DO}$ | DO delay time, DO settling time after CSB low (Note 28)      |     |     | 250 | ns      |
| $t_{DEL\_CLK\_DO}$ | DO delay time, DO settling time after CLK low (Note 28)      |     |     | 100 | ns      |

27. After leaving sleep mode an additional wait time of 250  $\mu s$  is needed before pulling CSB low.

28. Specified for a capacitive load 10 pF and a pull-up resistor of 1.5 k $\Omega$ .

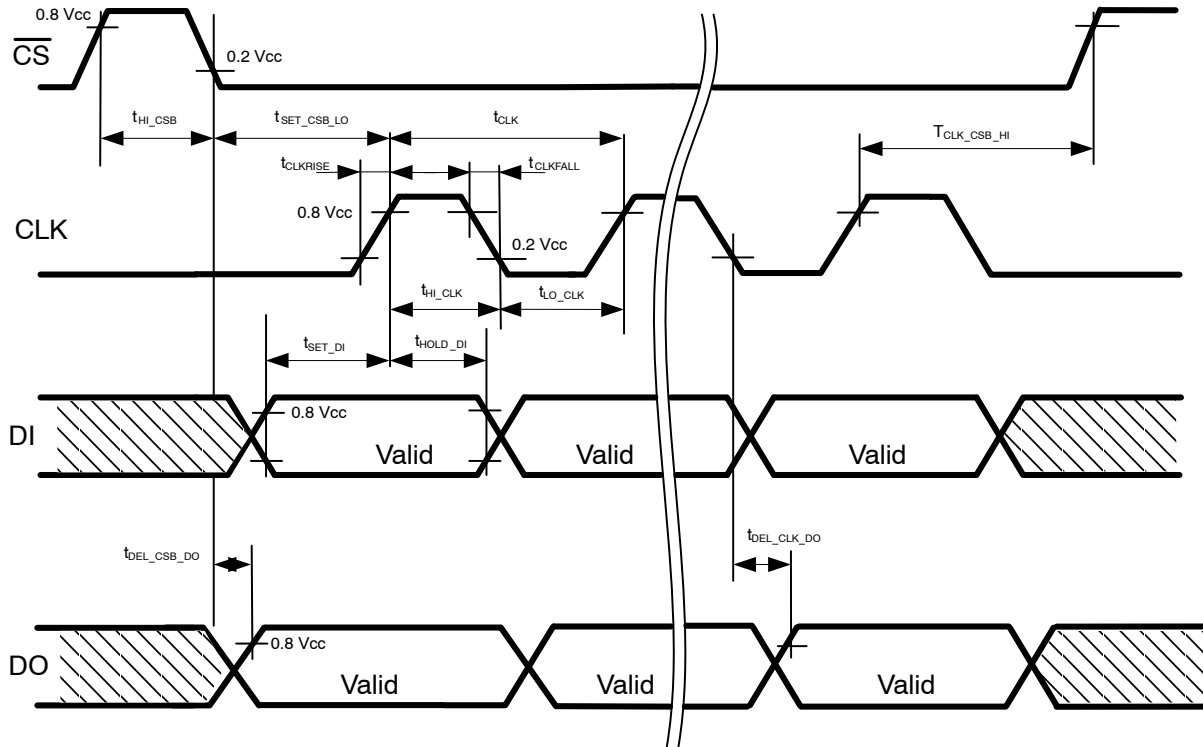


Figure 6. SPI Timing

## DETAILED OPERATING DESCRIPTION

**H-Bridge Drivers with PWM Control**

Two H-bridges are integrated to drive a bipolar stepper motor. Each H-bridge consists of two low-side N-type MOSFET switches and two high-side P-type MOSFET switches. One PWM current control loop with on-chip current sensing is implemented for each H-bridge. Depending on the desired current range and the micro-step position at hand, the  $R_{DS(on)}$  of the low-side transistors will be adapted to maintain current-sense accuracy. A comparator compares continuously the actual winding current with the requested current and feeds back the information to generate a PWM signal, which turns on/off the H-bridge switches. The switching points of the PWM duty-cycle are synchronized to the on-chip PWM clock. For each output bridge the PWM duty cycle is measured and stored in two appropriate status registers of the motor controller.

The PWM frequency will not vary with changes in the supply voltage. Also variations in motor-speed or load-conditions of the motor have no effect. There are no external components required to adjust the PWM frequency. In order to avoid large currents through the H-bridge switches, it is guaranteed that the top- and bottom-switches of the same half-bridge are never conductive simultaneously (interlock delay).

In order to reduce the radiated/conducted emission, voltage slope control is implemented in the output switches. Two bits in SPI control register 3 allow adjustment of the voltage slopes.

A protection against shorts on motor lines is implemented. When excessive voltage is sensed across a MOSFET for a time longer than the required transition time, then the MOSFET is switched-off.

**Motor Enable-Disable**

The H-bridges and PWM control can be disabled (high-impedance state) by means of a bit <MOTEN> in the SPI control registers. <MOTEN>=0 will only disable the drivers and will not impact the functions of NXT, DIR, RHB, SPI bus, etc. The H-bridges will resume normal PWM operation by writing <MOTEN>=1 in the SPI register. PWM current control is then enabled again and will regulate current in both coils corresponding with the position given by the current translator.

**Automatic Forward and Slow-Fast Decay**

The PWM generation is in steady-state using a combination of forward and slow-decay. For transition to lower current levels, fast-decay is automatically activated to allow high-speed response. The selection of fast or slow decay is completely transparent for the user and no additional parameters are required for operation.

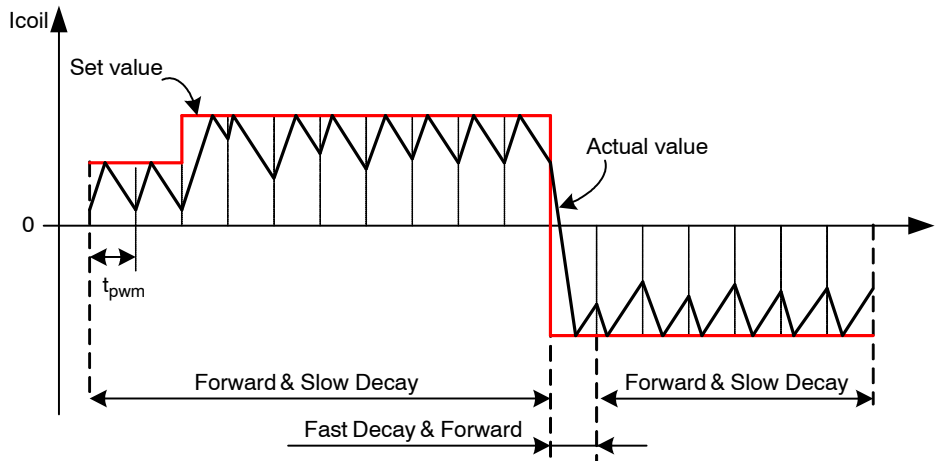


Figure 7. Forward and Slow/Fast Decay PWM

### PWM Duty Cycle Measurement

For both motor windings the actual PWM duty cycle is measured and stored in two status registers. The duty cycle values are a representation of the applied average voltage to

the motor windings to achieve and maintain the actual set point current. Figure 8 gives an example of the duty cycle representation.

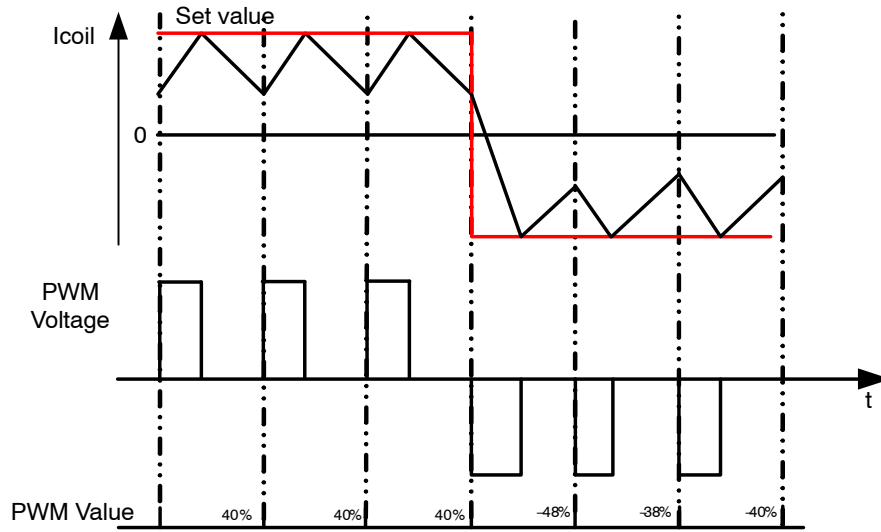


Figure 8. PWM Duty Cycle Measurement

### Automatic Duty Cycle Adaptation

If during regulation the set point current is not reached before 75% of  $t_{pwm}$ , the duty cycle of the PWM is adapted automatically to  $> 50\%$  (top regulation) to maintain the requested average current in the coils. This process is

completely automatic and requires no additional parameters for operation. The state of the duty cycle adaptation mode is represented in the T/B bits of the appropriate status registers for both motor windings X and Y. Figure 9 gives a representation of the duty cycle adaptation.

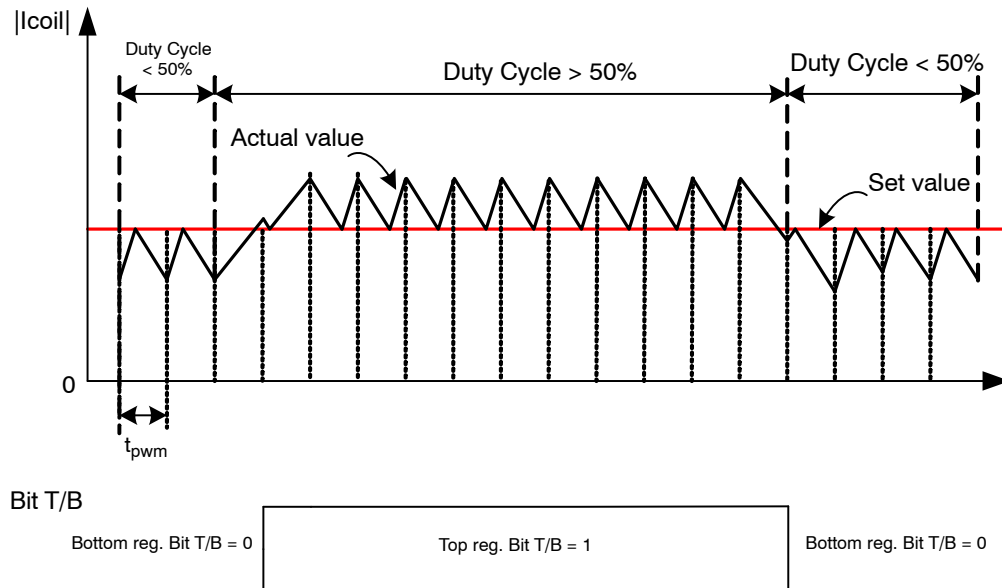


Figure 9. Automatic Duty Cycle Adaptation

## STEP TRANSLATOR

### Step Mode

The step translator provides the control of the motor by means of SPI register step mode: SM[2:0], SPI bits DIRP, RHBP and input pins STEP0, STEP1, DIR (direction of rotation), RHB (run/hold of motor) and NXT (next pulse). It is translating consecutive steps in corresponding currents in both motor coils for a given step mode.

One out of seven possible stepping modes can be selected through SPI-bits SM[2:0] and pins STEP0, STEP1. Device takes the value from SPI-bits SM[2:0] and increases StepMode value with adding binary information from STEP0, STEP1 pins. After power-on or hard reset, the coil-current translator is set to the default to 1/32 micro-stepping at position '16\*'. When remaining in the default step mode, subsequent translator positions are all in the same column and increased or decreased with 1. Table 9 lists the output current versus the translator position.

When the micro-step resolution is reduced, then the corresponding least-significant bits of the translator

position are set to "0". This means that the position in the current table moves to the right and in the case that micro-step position of desired new resolution does not overlap the micro-step position of current resolution, the closest value up or down in required column is set depending on the direction of rotation.

When the micro-step resolution is increased, then the corresponding least-significant bits of the translator position are added as "0": the micro-step position moves to the left on the same row.

In general any change of <SM[2:0]> SPI bits or STEP0 and STEP1 pins have no effect on current micro-step position without consequent occurrence of NXT pulse or <NXTP> SPI command. (see NXT input timing below). When NXT pulse or <NXTP> SPI command arrives, the motor moves into next micro-step position according to the current <SM[2:0]> SPI bits value and STEP0, STEP1 pins level set.

Table 9. CIRCULAR TRANSLATOR TABLE

| MSP[6:0] | Step mode SM[2:0] |      |     |     |     | % of I <sub>max</sub> |        | MSP[6:0] | Step mode SM[2:0] |      |     |     |     | % of I <sub>max</sub> |        |
|----------|-------------------|------|-----|-----|-----|-----------------------|--------|----------|-------------------|------|-----|-----|-----|-----------------------|--------|
|          | 000               | 001  | 010 | 011 | 100 | Coil Y                | Coil X |          | 000               | 001  | 010 | 011 | 100 | Coil Y                | Coil X |
|          | 1/32              | 1/16 | 1/8 | 1/4 | 1/2 |                       |        |          | 1/32              | 1/16 | 1/8 | 1/4 | 1/2 |                       |        |
| 000 0000 | 0                 | 0    | 0   | 0   | 0   | 0                     | 100    | 100 0000 | 64                | 32   | 16  | 8   | 4   | 0                     | −100   |
| 000 0001 | 1                 | −    | −   | −   | −   | 4.9                   | 99.9   | 100 0001 | 65                | −    | −   | −   | −   | −4.9                  | −99.9  |
| 000 0010 | 2                 | 1    | −   | −   | −   | 9.8                   | 99.5   | 100 0010 | 66                | 33   | −   | −   | −   | −9.8                  | −99.5  |
| 000 0011 | 3                 | −    | −   | −   | −   | 14.7                  | 98.9   | 100 0011 | 67                | −    | −   | −   | −   | −14.7                 | −98.9  |
| 000 0100 | 4                 | 2    | 1   | −   | −   | 19.5                  | 98.1   | 100 0100 | 68                | 34   | 17  | −   | −   | −19.5                 | −98.1  |
| 000 0101 | 5                 | −    | −   | −   | −   | 24.3                  | 97     | 100 0101 | 69                | −    | −   | −   | −   | −24.3                 | −97    |
| 000 0110 | 6                 | 3    | −   | −   | −   | 29                    | 95.7   | 100 0110 | 70                | 35   | −   | −   | −   | −29                   | −95.7  |
| 000 0111 | 7                 | −    | −   | −   | −   | 33.7                  | 94.2   | 100 0111 | 71                | −    | −   | −   | −   | −33.7                 | −94.2  |
| 000 1000 | 8                 | 4    | 2   | 1   | −   | 38.3                  | 92.4   | 100 1000 | 72                | 36   | 18  | 9   | −   | −38.3                 | −92.4  |
| 000 1001 | 9                 | −    | −   | −   | −   | 42.8                  | 90.4   | 100 1001 | 73                | −    | −   | −   | −   | −42.8                 | −90.4  |
| 000 1010 | 10                | 5    | −   | −   | −   | 47.1                  | 88.2   | 100 1010 | 74                | 37   | −   | −   | −   | −47.1                 | −88.2  |
| 000 1011 | 11                | −    | −   | −   | −   | 51.4                  | 85.8   | 100 1011 | 75                | −    | −   | −   | −   | −51.4                 | −85.8  |
| 000 1100 | 12                | 6    | 3   | −   | −   | 55.6                  | 83.1   | 100 1100 | 76                | 38   | 19  | −   | −   | −55.6                 | −83.1  |
| 000 1101 | 13                | −    | −   | −   | −   | 59.6                  | 80.3   | 100 1101 | 77                | −    | −   | −   | −   | −59.6                 | −80.3  |
| 000 1110 | 14                | 7    | −   | −   | −   | 63.4                  | 77.3   | 100 1110 | 78                | 39   | −   | −   | −   | −63.4                 | −77.3  |
| 000 1111 | 15                | −    | −   | −   | −   | 67.2                  | 74.1   | 100 1111 | 79                | −    | −   | −   | −   | −67.2                 | −74.1  |
| 001 0000 | 16(*)             | 8    | 4   | 2   | 1   | 70.7                  | 70.7   | 101 0000 | 80                | 40   | 20  | 10  | 5   | −70.7                 | −70.7  |
| 001 0001 | 17                | −    | −   | −   | −   | 74.1                  | 67.2   | 101 0001 | 81                | −    | −   | −   | −   | −74.1                 | −67.2  |
| 001 0010 | 18                | 9    | −   | −   | −   | 77.3                  | 63.4   | 101 0010 | 82                | 41   | −   | −   | −   | −77.3                 | −63.4  |
| 001 0011 | 19                | −    | −   | −   | −   | 80.3                  | 59.6   | 101 0011 | 83                | −    | −   | −   | −   | −80.3                 | −59.6  |
| 001 0100 | 20                | 10   | 5   | −   | −   | 83.1                  | 55.6   | 101 0100 | 84                | 42   | 21  | −   | −   | −83.1                 | −55.6  |
| 001 0101 | 21                | −    | −   | −   | −   | 85.8                  | 51.4   | 101 0101 | 85                | −    | −   | −   | −   | −85.8                 | −51.4  |
| 001 0110 | 22                | 11   | −   | −   | −   | 88.2                  | 47.1   | 101 0110 | 86                | 43   | −   | −   | −   | −88.2                 | −47.1  |
| 001 0111 | 23                | −    | −   | −   | −   | 90.4                  | 42.8   | 101 0111 | 87                | −    | −   | −   | −   | −90.4                 | −42.8  |
| 001 1000 | 24                | 12   | 6   | 3   | −   | 92.4                  | 38.3   | 101 1000 | 88                | 44   | 22  | 11  | −   | −92.4                 | −38.3  |
| 001 1001 | 25                | −    | −   | −   | −   | 94.2                  | 33.7   | 101 1001 | 89                | −    | −   | −   | −   | −94.2                 | −33.7  |
| 001 1010 | 26                | 13   | −   | −   | −   | 95.7                  | 29     | 101 1010 | 90                | 45   | −   | −   | −   | −95.7                 | −29    |
| 001 1011 | 27                | −    | −   | −   | −   | 97                    | 24.3   | 101 1011 | 91                | −    | −   | −   | −   | −97                   | −24.3  |
| 001 1100 | 28                | 14   | 7   | −   | −   | 98.1                  | 19.5   | 101 1100 | 92                | 46   | 23  | −   | −   | −98.1                 | −19.5  |
| 001 1101 | 29                | −    | −   | −   | −   | 98.9                  | 14.7   | 101 1101 | 93                | −    | −   | −   | −   | −98.9                 | −14.7  |
| 001 1110 | 30                | 15   | −   | −   | −   | 99.5                  | 9.8    | 101 1110 | 94                | 47   | −   | −   | −   | −99.5                 | −9.8   |
| 001 1111 | 31                | −    | −   | −   | −   | 99.9                  | 4.9    | 101 1111 | 95                | −    | −   | −   | −   | −99.9                 | −4.9   |
| 010 0000 | 32                | 16   | 8   | 4   | 2   | 100                   | 0      | 110 0000 | 96                | 48   | 24  | 12  | 6   | −100                  | 0      |
| 010 0001 | 33                | −    | −   | −   | −   | 99.9                  | −4.9   | 110 0001 | 97                | −    | −   | −   | −   | −99.9                 | 4.9    |
| 010 0010 | 34                | 17   | −   | −   | −   | 99.5                  | −9.8   | 110 0010 | 98                | 49   | −   | −   | −   | −99.5                 | 9.8    |
| 010 0011 | 35                | −    | −   | −   | −   | 98.9                  | −14.7  | 110 0011 | 99                | −    | −   | −   | −   | −98.9                 | 14.7   |
| 010 0100 | 36                | 18   | 9   | −   | −   | 98.1                  | −19.5  | 110 0100 | 100               | 50   | 25  | −   | −   | −98.1                 | 19.5   |
| 010 0101 | 37                | −    | −   | −   | −   | 97                    | −24.3  | 110 0101 | 101               | −    | −   | −   | −   | −97                   | 24.3   |
| 010 0110 | 38                | 19   | −   | −   | −   | 95.7                  | −29    | 110 0110 | 102               | 51   | −   | −   | −   | −95.7                 | 29     |

\*Default position after reset of the translator position.

Table 9. CIRCULAR TRANSLATOR TABLE

| MSP[6:0] | Step mode SM[2:0] |      |     |     |     | % of I <sub>max</sub> |        | MSP[6:0] | Step mode SM[2:0] |      |     |     |     | % of I <sub>max</sub> |        |
|----------|-------------------|------|-----|-----|-----|-----------------------|--------|----------|-------------------|------|-----|-----|-----|-----------------------|--------|
|          | 000               | 001  | 010 | 011 | 100 | Coil Y                | Coil X |          | 000               | 001  | 010 | 011 | 100 | Coil Y                | Coil X |
|          | 1/32              | 1/16 | 1/8 | 1/4 | 1/2 |                       |        |          | 1/32              | 1/16 | 1/8 | 1/4 | 1/2 |                       |        |
| 010 0111 | 39                | –    | –   | –   | –   | 94.2                  | –33.7  | 110 0111 | 103               | –    | –   | –   | –   | –94.2                 | 33.7   |
| 010 1000 | 40                | 20   | 10  | 5   | –   | 92.4                  | –38.3  | 110 1000 | 104               | 52   | 26  | 13  | –   | –92.4                 | 38.3   |
| 010 1001 | 41                | –    | –   | –   | –   | 90.4                  | –42.8  | 110 1001 | 105               | –    | –   | –   | –   | –90.4                 | 42.8   |
| 010 1010 | 42                | 21   | –   | –   | –   | 88.2                  | –47.1  | 110 1010 | 106               | 53   | –   | –   | –   | –88.2                 | 47.1   |
| 010 1011 | 43                | –    | –   | –   | –   | 85.8                  | –51.4  | 110 1011 | 107               | –    | –   | –   | –   | –85.8                 | 51.4   |
| 010 1100 | 44                | 22   | 11  | –   | –   | 83.1                  | –55.6  | 110 1100 | 108               | 54   | 27  | –   | –   | –83.1                 | 55.6   |
| 010 1101 | 45                | –    | –   | –   | –   | 80.3                  | –59.6  | 110 1101 | 109               | –    | –   | –   | –   | –80.3                 | 59.6   |
| 010 1110 | 46                | 23   | –   | –   | –   | 77.3                  | –63.4  | 110 1110 | 110               | 55   | –   | –   | –   | –77.3                 | 63.4   |
| 010 1111 | 47                | –    | –   | –   | –   | 74.1                  | –67.2  | 110 1111 | 111               | –    | –   | –   | –   | –74.1                 | 67.2   |
| 011 0000 | 48                | 24   | 12  | 6   | 3   | 70.7                  | –70.7  | 111 0000 | 112               | 56   | 28  | 14  | 7   | –70.7                 | 70.7   |
| 011 0001 | 49                | –    | –   | –   | –   | 67.2                  | –74.1  | 111 0001 | 113               | –    | –   | –   | –   | –67.2                 | 74.1   |
| 011 0010 | 50                | 25   | –   | –   | –   | 63.4                  | –77.3  | 111 0010 | 114               | 57   | –   | –   | –   | –63.4                 | 77.3   |
| 011 0011 | 51                | –    | –   | –   | –   | 59.6                  | –80.3  | 111 0011 | 115               | –    | –   | –   | –   | –59.6                 | 80.3   |
| 011 0100 | 52                | 26   | 13  | –   | –   | 55.6                  | –83.1  | 111 0100 | 116               | 58   | 29  | –   | –   | –55.6                 | 83.1   |
| 011 0101 | 53                | –    | –   | –   | –   | 51.4                  | –85.8  | 111 0101 | 117               | –    | –   | –   | –   | –51.4                 | 85.8   |
| 011 0110 | 54                | 27   | –   | –   | –   | 47.1                  | –88.2  | 111 0110 | 118               | 59   | –   | –   | –   | –47.1                 | 88.2   |
| 011 0111 | 55                | –    | –   | –   | –   | 42.8                  | –90.4  | 111 0111 | 119               | –    | –   | –   | –   | –42.8                 | 90.4   |
| 011 1000 | 56                | 28   | 14  | 7   | –   | 38.3                  | –92.4  | 111 1000 | 120               | 60   | 30  | 15  | –   | –38.3                 | 92.4   |
| 011 1001 | 57                | –    | –   | –   | –   | 33.7                  | –94.2  | 111 1001 | 121               | –    | –   | –   | –   | –33.7                 | 94.2   |
| 011 1010 | 58                | 29   | –   | –   | –   | 29                    | –95.7  | 111 1010 | 122               | 61   | –   | –   | –   | –29                   | 95.7   |
| 011 1011 | 59                | –    | –   | –   | –   | 24.3                  | –97    | 111 1011 | 123               | –    | –   | –   | –   | –24.3                 | 97     |
| 011 1100 | 60                | 30   | 15  | –   | –   | 19.5                  | –98.1  | 111 1100 | 124               | 62   | 31  | –   | –   | –19.5                 | 98.1   |
| 011 1101 | 61                | –    | –   | –   | –   | 14.7                  | –98.9  | 111 1101 | 125               | –    | –   | –   | –   | –14.7                 | 98.9   |
| 011 1110 | 62                | 31   | –   | –   | –   | 9.8                   | –99.5  | 111 1110 | 126               | 63   | –   | –   | –   | –9.8                  | 99.5   |
| 011 1111 | 63                | –    | –   | –   | –   | 4.9                   | –99.9  | 111 1111 | 127               | –    | –   | –   | –   | –4.9                  | 99.9   |

\*Default position after reset of the translator position.

Besides the micro-step modes listed above, also two full step modes are implemented. Full step mode 1 activates always only one coil at a time, whereas mode 2 always keeps 2 coils active. The table below lists the output current versus the translator positions for these cases and Figure 10 shows the projection on a square.

Changing between micro-step mode and full step modes follows a similar scheme as changes between micro-step

modes. Changing from one full step mode to another full step mode will always result in a “45deg step-back or forward” depending on the DIR bit. For example: in the table below, when changing full step mode (positioner is on a particular row and full step column), then the new full step location will be one row above or below in the adjacent “full step column”. The step-back and forward is executed after the NXT pulse.

Table 10. SQUARE TRANSLATOR TABLE FOR FULL STEP

| MSP[6:0] | Step mode ( SM[2:0] ) |            | % of I <sub>max</sub> |        |
|----------|-----------------------|------------|-----------------------|--------|
|          | 101 or 110            | 111        | Coil x                | Coil y |
|          | Full Step1            | Full Step2 |                       |        |
| 000 0000 | 0                     | –          | 100                   | 0      |
| 001 0000 | –                     | 0          | 71                    | 71     |
| 010 0000 | 1                     | –          | 0                     | 100    |
| 011 0000 | –                     | 1          | –71                   | 71     |
| 100 0000 | 2                     | –          | –100                  | 0      |
| 101 0000 | –                     | 2          | –71                   | –71    |
| 110 0000 | 3                     | –          | 0                     | –100   |
| 111 0000 | –                     | 3          | 71                    | –71    |

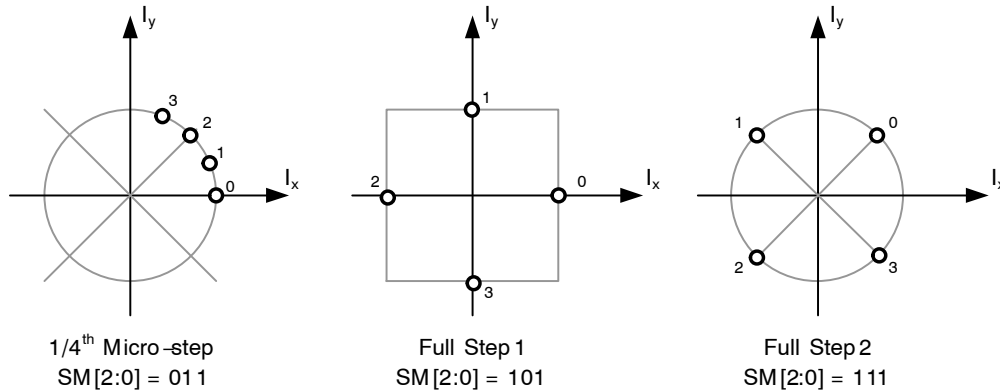


Figure 10. Translator Table: Circular and Square

**Translator Position**

The translator position can be read in the SPI register <MSP[6:0]>. This is a 7-bit number equivalent to the 1/32<sup>th</sup> micro-step from : Circular Translator Table. The translator position is updated immediately following a next micro-step trigger (see below).

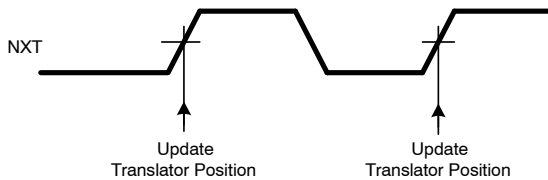


Figure 11. Translator Position Timing Diagram

**Direction**

The direction of rotation is selected by means of input pin DIR and its “polarity bit” <DIRP> (SPI register). The polarity bit <DIRP> allows changing the direction of rotation by means of only SPI commands instead of the dedicated input pin.

$$\text{Direction} = \text{DIR-pin EXOR } \langle \text{DIRP} \rangle$$

Positive direction of rotation means counter-clockwise rotation of electrical vector  $I_x + I_y$ . Also when the motor is disabled (<MOTEN>=0), both the DIR pin and <DIRP> will have an effect on the positioner. The logic state of the DIR pin is visible as a flag in SPI status register.

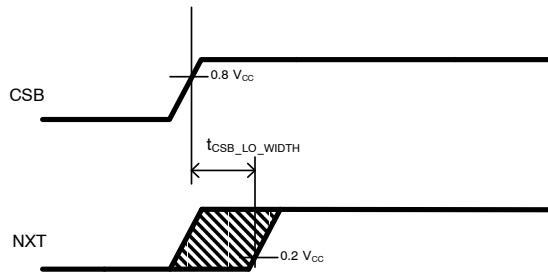
**Next Micro-Step Trigger**

Positive edges on the NXT input – or activation of the “NXT pushbutton” <NXTP> in the SPI input register – will move the motor current one step up/down in the translator table. The <NXTP> bit in SPI is used to move positioner one (micro-)step by means of only SPI commands. If the bit is set to “1”, it is reset automatically to “0” after having advanced the positioner with one micro-step.

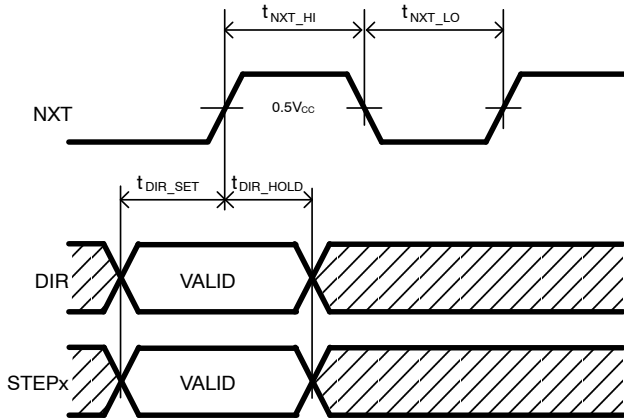
Trigger “Next micro-step” = (positive edge on NXT-pin)  
OR (<NXTP>=1)

- Also when the motor is disabled (<MOTEN>=0), NXT/DIR/RHB functions will move the positioner according to the logic.
- In order to be sure that both the NXT pin and the <NXTP> SPI command are individually attended, the following non overlapping zone has to be respected. In this case it is guaranteed that both triggers will have effect (2 steps are taken).





**Figure 12. NXT Input Non Overlapping Zone with the <NXTP> SPI Command**



**Figure 13. NXT Input Timing Diagram**

For control by means of I/O's, the NXT pin operation with respect to DIR, STEP0 and STEP1 pins should be in a non-overlapped way. See also the timing diagram below (refer to the AC table for the timing values). The STEP0 and STEP1 pins or <SM[2:0]> SPI bits setting, when changed, is accepted upon the consequent either NXT pin rising edge

or <NXTP> SPI command only. On the other hand, the SPI bits <DIRP>, <SM[2:0]> and <NXTP> can change state at the same time in the same SPI command: the next micro-step will be applied with the new settings.

#### IRUN, IHOLD and “Run / Not Hold” Mode

The RHB input pin and its “polarity bit” <RHBP> (SPI register) allow to switch the driver between “Run Mode” and “Hold Mode”.

“Run Mode” = NOT(“Hold Mode”) = RHB-pin EXOR <RHBP>

- In “Run mode”, the current translator table is stepped through based on the “NXT & DIR” commands. The amplitude of the motor current (=Imax) is set by SPI control register <IRUN[3:0]>.
- In “Hold mode”, NXT & DIR will have no effect and the position in the current translator table is maintained. The motor current amplitude is set by SPI control register <IHOLD[3:0]>.

By setting bit <Iboost> in NCV70514MW007 device in SPI Control register 4A, the current table will be changed from 800 mA peak current range to 1.1 A peak current range. All currents will scale proportionally according to the following table. The boost function can be activated at temperatures below thermal warning temperature TW. Above thermal warning temperature TW, the boost function is automatically disabled and current is decreased to unboosted level. Status of the boost function can be read in SPI <Iboost> bit. Thermal profile and mission profile must be checked by **onsemi** to guarantee the reliability.

The run and hold current settings correspond to the following current levels:

**Table 11. IRUN AND IHOLD VALUES (4BIT)**

| Register Value | Peak Motor Current IRUN (mA)<br>$I_{boost} = 0$ | Peak Motor Current IRUN (mA)<br>$I_{boost} = 1$ | Peak Motor Current IHOLD (mA)<br>$I_{boost} = 0$ | Peak Motor Current IHOLD (mA)<br>$I_{boost} = 1$ |
|----------------|-------------------------------------------------|-------------------------------------------------|--------------------------------------------------|--------------------------------------------------|
| 0              | 59                                              | 81                                              | 0                                                | 0                                                |
| 1              | 71                                              | 98                                              | 59                                               | 81                                               |
| 2              | 84                                              | 116                                             | 71                                               | 98                                               |
| 3              | 100                                             | 138                                             | 84                                               | 116                                              |
| 4              | 119                                             | 164                                             | 100                                              | 138                                              |
| 5              | 141                                             | 194                                             | 119                                              | 164                                              |
| 6              | 168                                             | 231                                             | 141                                              | 194                                              |
| 7              | 200                                             | 275                                             | 168                                              | 231                                              |
| 8              | 238                                             | 327                                             | 200                                              | 275                                              |
| 9              | 283                                             | 389                                             | 238                                              | 327                                              |
| A              | 336                                             | 462                                             | 283                                              | 389                                              |
| B              | 400                                             | 550                                             | 336                                              | 462                                              |
| C              | 476                                             | 655                                             | 400                                              | 550                                              |
| D              | 566                                             | 778                                             | 476                                              | 655                                              |

**Table 11. IRUN AND IHOLD VALUES (4BIT)**

|   |     |      |     |     |
|---|-----|------|-----|-----|
| E | 673 | 925  | 566 | 778 |
| F | 800 | 1100 | 673 | 925 |

NOTE: During hold with a hold current of 0 mA the stall and motion detection and the open coil detection are disabled. The PWM duty cycle registers will present 0% duty cycle.

Whenever <IRUN[3:0]> or <IHOLD[3:0]> is changed, the new coil currents will be updated immediately at the next PWM period.

In case the motor is disabled (<MOTEN>=0), the logic is functional and both RHB pin and <RHBP> bit will have effect on NXT/DIR operation (not on the H-bridges). When the chip is in sleep mode, the logic is not functional and as a result, the RHB pin will have no effect.

The logic state of the RHB pin is visible as a flag in SPI status register.

**Note:** The hard-reset function is embedded in the “Hold mode” by means of a special sequence on the DIR pin, see also Hard-Reset Function chapter.

#### Under-voltage Detection

The NCV70514 has three UV threshold levels. Two higher threshold levels are programmable over SPI register UVxThr, third threshold level is fixed.

Each UV level has its own flag readable via SPI and can create interrupt to microcontroller when dedicated bit of interrupt enable register is set.

All interrupt sources UV's, BEMF, etc. are grouped into single interrupt line (pin) ERRB.

When supply voltage VBB drops under dedicated UVx level, several actions are performed.

- UV1 level – no action inside device regarding to H-bridges – only when UV1IntEn interrupt enable bit is set, ERRB pin is pulled down. Microcontroller needs to do action like Soft stop, etc based on this interrupt.
- UV2 level – when UV2IntEn interrupt enable bit is set, ERRB pin is pulled down. When UV2MIntEn interrupt enable bit is set, the ERRB pin is pulled down in the moment NXP pulse comes, the device then stops executing NXT pulses and starts counting them in Step loss counter <SI[6:0]>.
- UV3 level – device each time disables H-Bridge drivers (<MOTEN> = 0). When UV3IntEn interrupt enable bit is set, ERRB pin is pulled down. When UV3MIntEn interrupt enable bit is set, the ERRB pin is pulled down in the moment NXP pulse comes, the device then stops executing NXT pulses and starts counting them in Step loss counter <SI[6:0]>.

Only if the <UV3>=0 the motor can be enabled again by writing <MOTEN>=1 in the control register 1.

**Note:** The change of DIR and step mode will not be taken into account in Step loss counter.

Step loss register range is 7 bits => 0 to 127 NXT pulses, no overflow, keeping the counter at maximum value of 127 if more than 127 NXT pulses are received.

**Table 12. UV1/2 THRESHOLDS SETTINGS (4BIT)**

| UVxThr Index | UV1/2 Threshold Level (V) |
|--------------|---------------------------|
| 0            | 5.98                      |
| 1            | 6.31                      |
| 2            | 6.65                      |
| 3            | 6.98                      |
| 4            | 7.31                      |
| 5            | 7.64                      |
| 6            | 7.97                      |
| 7            | 8.31                      |
| 8            | 8.64                      |
| 9            | 8.97                      |
| A            | 9.3                       |
| B            | 9.63                      |
| C            | 9.97                      |
| D            | 10.3                      |
| E            | 10.63                     |
| F            | 10.96                     |

#### Stall and Motion Detection

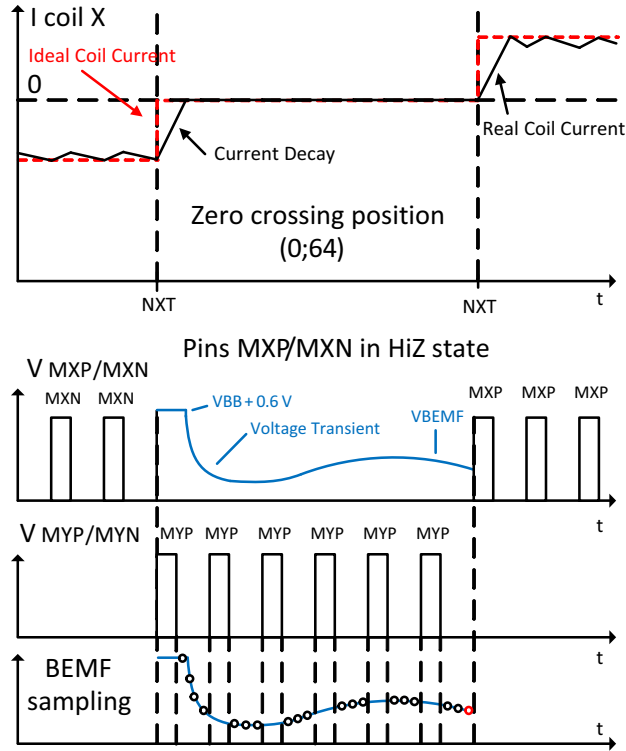
Motion detection is based on the Back Electromotive Force (BEMF or back emf) generated into the running motor. When the motor is blocked, e.g. when it hits the end-position, the velocity and as a result also the generated back emf, is disturbed. The NCV70514 measures the back emf during the current zero crossing phase and makes it available in the SPI status register 4. The back emf voltage is measured several times in each PWM cycle during zero crossing phase. Samples taken during PWM ON phase of the switches in the second coil are discarded not to add noise to measurement (see Figure 14). Results are then converted into a 5-bits word <Bemf[4:0]> with the following formula:

$$\text{BEMF\_code(dec)} = V\_MOT\_XorY\_diff(V) \cdot \text{Gain} \cdot \left(\frac{5}{4}\right) \cdot \frac{2^5}{2.41}$$

When the result is ready, it is indicated by <BemfRes> bit in status register.

When using normal mode of back emf measurement ( $\langle \text{EnhBemfEn} \rangle = 0$ ), last sample before end of current zero crossing phase becomes available in  $\langle \text{Bemf}[4:0] \rangle$  register (see the red circle on Figure 14).

When the enhanced back emf measurement mode is set by  $\langle \text{EnhBemfEn} \rangle$  bit, all non discarded results are continuously available in  $\langle \text{Bemf}[4:0] \rangle$  register (see red and all black circles on Figure 14). This allows microcontroller (when reading content of the register fast enough) to follow back emf signal and its shape during zero crossing phase and use more complex algorithms to optimize the work of driven stepper motor.



**Figure 14. Back emf Sampling**

For slow speed or when a motion ends at a full step position (there is an absence of next NXT trigger), the end of the zero crossing is taking too long or is non-existing. In this case, the back emf voltage is taken the latest at “stall time-out” time and this value is used also for comparison with  $\langle \text{StThr}[3:0] \rangle$  stall threshold to detect stall situation in run mode or movement in hold mode. The “stall time-out” is set in SPI by means of  $\langle \text{StTo}[7:0] \rangle$  register and is expressed in counts of  $4/f_{\text{PWM}}$  (See AC Table), roughly

in steps of 0.2 ms. If  $\langle \text{StTo}[7:0] \rangle = 0$ , time-out is not active.

At the end of the current zero crossing phase the internal circuitry compares measured back emf voltages with  $\langle \text{StThr}[3:0] \rangle$  register, which determines threshold for stall detection. The last sample of back emf taken before end of zero crossing phase is used for stall detection in normal mode as well as in enhanced back emf mode. When  $\langle \text{StThr}[3:0] \rangle = 0$  then stall detection is disabled. When value of  $\langle \text{StThr}[3:0] \rangle$  is different from 0 and measured back emf signal is lower than  $\langle \text{StThr}[3:0] \rangle$  threshold for 2 succeeding coil current zero-crossings (including both X and Y coil), then the  $\langle \text{STALL} \rangle$  bit in SPI status register 1 is set, the current translator table goes 135 degrees in opposite direction and the ERRB pin is pulled down, Irun is maintained. The stall bit is cleared by reading the status register 1, also the ERRB pin becomes inactive again. With stall bit cleared, the chip reacts on “Next Micro-step Triggers” only after direction has changed its state at least once.

An additional feature of the NCV70514 is the detection of uncontrolled motion during Hold. If the stall detection is enabled and the hold position is at full steps (full step mode1,  $0^\circ$ ,  $90^\circ$ ,  $180^\circ$ ,  $270^\circ$ ) with only excitation of one coil, the NCV70514 is checking upon back emf voltages higher than or equal to the  $\langle \text{StThr}[3:0] \rangle$  threshold. If this voltage is detected, it indicates there is a motor movement. The stall bit in the SPI register is set and the ERRB pin is pulled down. The motion detection during hold does not work for IHold 0 A.

**Notes:**

1. Used stall detection is covered by patent US 8,058,894B2
2. As the stall threshold register  $\langle \text{StThr}[3:0] \rangle$  is 4 bits wide, the 4 MSBs of 5-bit  $\langle \text{Bemf}[4:0] \rangle$  register are taken for comparison.

Stall detection and Bemf measurement are performed only when Speed register value  $\langle \text{Sp}[7:0] \rangle$  is less than or equal to Speed threshold register value  $\langle \text{SpThr}[7:0] \rangle$ .

Range and resolution of Speed register and Speed threshold register are 0 to 5100  $\mu\text{s}$  and 20  $\mu\text{s}/\text{digit}$  for half stepping mode. Accuracy of speed (time) measurement is given by the accuracy of the internal oscillator.

If measured back emf voltage has not expected polarity, the back emf sign flag  $\langle \text{Bemfs} \rangle$  is set. Motor pin, where lower voltage is expected, is tied to GND by pull down current. Sign is determined by comparator, which compares

the polarity of voltage measured over the coil with expected polarity of voltage.

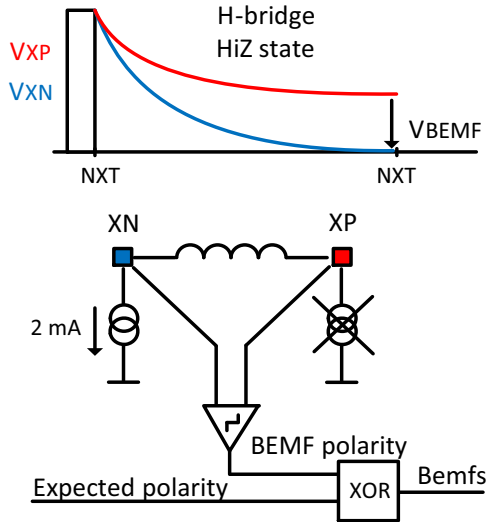


Figure 15. Back emf Sign Value

The last measured back emf value <Bemf[4:0]>, sign flag <Bems> and coil where the last back emf sample was taken <Bemfcoil> can be read out via SPI.

Table 13. STALL THRESHOLDS SETTINGS (4BIT)

| StThr index | StThr Level (V) | StThr Level (V) |
|-------------|-----------------|-----------------|
|             | BemfGain = 1    | BemfGain = 0    |
| 0           | Disable         | Disable         |
| 1           | 0.48            | 0.24            |
| 2           | 0.96            | 0.48            |
| 3           | 1.44            | 0.72            |
| 4           | 1.92            | 0.96            |
| 5           | 2.4             | 1.2             |
| 6           | 2.88            | 1.44            |
| 7           | 3.36            | 1.68            |
| 8           | 3.84            | 1.92            |
| 9           | 4.32            | 2.16            |
| A           | 4.8             | 2.4             |
| B           | 5.28            | 2.64            |
| C           | 5.76            | 2.88            |
| D           | 6.24            | 3.12            |
| E           | 6.72            | 3.36            |
| F           | 7.2             | 3.6             |

## WARNING, ERROR DETECTION AND DIAGNOSTICS FEEDBACK

### Open & Short Circuit Diagnostic

The NCV70514 stepper driver features an enhanced diagnostic detection and feedback, to be read by the external microcontroller unit (MCU). Among the main items of interest for the application and typical failures, are open coil and the short circuit condition, which may be to ground (chassis), or to supply (battery line).

To serve this purpose two diagnostic modes are available in the device. The first is called “Automatic Diagnostic” and is executed after each power-up sequence. In addition, by a specific bit setting, it can be enabled after any output (H-bridge) activation. The other mode is defined as “User Diagnostic” or “Normal Mode Diagnostic” and consists in applying activation sequences directly from the MCU and read back the consequent status via the proper device registers.

### Open & Short circuit Automatic Diagnostic

The auto-diagnostic is executed after each power up, or when enabling the H-bridge (<MOTEN>=0 → <MOTEN>=1) in case the <DIAGEN> bit would be programmed to one (see SPI table, control register 0x03, bit 6).

During the auto-diagnostic sequence, the device makes use of internal pull-ups and pull-downs (see Figure 16) to test the connections at the XP, XN, YP, YN pins with weak currents. This mechanism guarantees a very wide coverage; however, some conditions are reported as multiple failure source detections. This is due to the impossibility to discern between the two cases from electrical point of view. Details of failures combination coverage by the automatic diagnostic for the X coil are shown in Figure 14. The same is applicable for Y coil.

Any short circuit detection disables the output H-bridges (<MOTEN> = 0) and does not allow the device to automatically proceed to “normal mode”. To permit entering normal mode, the registers involved must be cleared out by SPI reading and the error condition removed prior enabling again the outputs (<MOTEN> set to “1”).

The dead time for automatic diagnostic routine is 2 ms (\*). The automatic diagnostic is interrupted when the supply voltage drops below UV3 level.

**Note: (\*)**: For a controlled start of the automatic diagnostics, the user has to place the motor driver in high impedance state by setting the <MOTEN> bit to ‘0’. After setting the <MOTEN> bit to ‘1’, there is a need for an additional delay time. This is needed for recirculation of the motor current. An average time of approximately 2 ms is needed. This time has to be taken into account by the user.

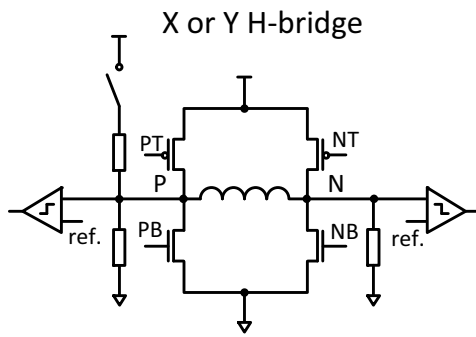


Figure 16. Automatic Diagnostic

Table 14. DIAGNOSTICS OPEN/SHORT DETECTION

| Fault condition                                                                            | SR1[5:4] =<br>{SHORT,<br>OPEN} | SR7A[6] =<br>{OPENX,L} | SR7A[3] =<br>{SHRTXPB} | SR7A[2] =<br>{SHRTXNB} | SR7A[1] =<br>{SHRTXPT} | SR7A[0] =<br>{SHRTXNT} |
|--------------------------------------------------------------------------------------------|--------------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| No short, No open coil – unique detection                                                  | 0, 0                           | 0                      | 0                      | 0                      | 0                      | 0                      |
| Short XP and/or XN top side, no open coil;<br>Short XP and XN top side and open coil       | 1, 0                           | 0                      | 0                      | 0                      | 1                      | 1                      |
| Short XP and/or XN bottom side, no open coil;<br>Short XP and XN bottom side and open coil | 1, 1                           | 1                      | 1                      | 1                      | 0                      | 0                      |
| No short or short XN bottom side, open coil                                                | 1, 1                           | 1                      | 0                      | 1                      | 0                      | 0                      |
| Short XP top side, open coil                                                               | 1, 1                           | 1                      | 0                      | 0                      | 1                      | 0                      |
| Short XN top side and short XP bottom side,<br>open coil                                   | 1, 1                           | 1                      | 1                      | 0                      | 0                      | 1                      |
| Short XN top side, open coil                                                               | 1, 1                           | 1                      | 0                      | 0                      | 0                      | 1                      |

### Open & Short circuit User Diagnostic

When in normal mode, the device will continuously check upon errors with respect to the expected behavior.

The open load condition is determined by the fact that the PWM duty cycle keeps 100% value for a time longer than set by <OpenDet[1:0]> register. This is valid of course only for the X/Y coil where the current is supposed to circulate, meaning that in full step positions (MSP[6:0] = {0; 32; 64; 96} (dec)) the open load can be detected only for one of the coil at a time (respectively {X; Y; X; Y}). The same reasoning applies for the short circuits detection.

Due to the timeout value set by <OpenDet[1:0]>, the open coil detection is dependent on the motor speed. In more detail, there is a maximum speed at which it can be done. Table 15 specifies these maxima for the different step modes. For practical reasons, all values are given in full steps per second.

Table 15. MAXIMUM VELOCITIES FOR OPEN COIL DETECTION

| Step Mode  | Speed [FS/s] for given <OpenDet[1:0]> |      |      |     |
|------------|---------------------------------------|------|------|-----|
|            | 00                                    | 01   | 10   | 11  |
| Full Step1 | 200                                   | 40   | 20   | 5   |
| Full Step2 | 400                                   | 80   | 40   | 10  |
| 1/2        | 300                                   | 60   | 30   | 7.5 |
| 1/4        | 350                                   | 70   | 35   | 8.8 |
| 1/8        | 375                                   | 75   | 37.5 | 9.4 |
| 1/16       | 387.5                                 | 77.5 | 38.8 | 9.7 |
| 1/32       | 393.8                                 | 78.8 | 39.4 | 9.8 |

When Open coil condition is detected, the appropriate bit (<OPENX> or <OPENY>) together with <OPEN> bit in the SPI status register are set. Reaction of the H-bridge to Open coil condition depends on the settings of <OpenHiZ> and <OpenDis> bits.

When both <OpenHiZ> and <OpenDis> bits are 0, <MOTEN> bit stays in 1 and only H-bridge where open coil is detected is disabled. When <OpenHiZ> bit is set, both

H-bridges are disabled (<MOTEN>=0) in case of Open coil detection. When <OpenDis> bit is set, drivers remain active for both coils independently of <OpenHiZ> bit.

The short circuit detection monitors the load current in each activated output stage. The current is measured in terms of voltage drop over the MOSFETS'  $R_{DS(ON)}$ . If the load current exceeds the over-current detection threshold, then the over-current flag <SHORT> is set and the drivers are switched off to protect the integrated circuit. Each driver stage has an individual detection bit for the N side and the P side.

When short circuit is detected, <MOTEN> is set to 0. The positioner, the NXT, RHB, STEP0, STEP1 and DIR stay operational. The flag <SHORT> (result of OR-ing the latched flags: <SHRTXPT> OR <SHRTXPB> OR <SHRTXNT> OR <SHRTYXNB> OR <SHRTYPT> OR <SHRTYPB> OR <SHRTYNT> OR <SHRTYNB>) is reset when the microcontroller reads out the short circuit status flags in status registers 7A and 8A.

To enable the motor again after reading out of the status flags, <MOTEN>=1 has to be written. Depending on the <DIAGEN> bit, Automatic diagnostic can be performed after enabling the outputs (H-bridges) prior to going to normal mode operation.

### Notes:

1. Successive reading of the <SHRTij> flags and re-enabling the motor in case of a short circuit condition may lead to damage of the drivers.
2. Example: SHRTXPT means: Short at X coil, Positive output pin, Top transistor.
3. In case of the short from any stepper motor pin to the top side during switching event from bottom to top on motor pin, the flag “short to bottom side” is set instead of the expected “short to top side” flag.

### Thermal Warning and Shutdown

When junction temperature is above  $T_{TW}$ , the thermal warning bit <TW> is set (SPI register) and the ERRB pin is



pulled down (\*). If junction temperature increases above thermal shutdown level, then also the <TSD> flag is set, the ERRB pin is pulled down, the motor is disabled (<MOTEN> = 0) and the hardware reset is disabled. If  $T_j < T_{TW}$  level and <TSD> bit has been read-out, the status of <TSD> is cleared and the ERRB pin is released.

Only if the <TSD>=<TW>=0, the motor can be enabled again by writing <MOTEN>=1 in the control register 1.

During the over temperature condition the hardware reset will not work until  $T_j < T_{TW}$  and the <TSD> readout is done.

In this way it is guaranteed that after a <TSD>=1 event, the die-temperature decreases back to the level of <TW>.

**Note:** (\*): During the <TW> situation the motor is not disabled while the ERRB is pulled down. To be informed about other error situations it is recommended to poll the status registers on a regular base (time base driven by application software in the millisecond domain).

### SPI Framing Error

The SPI transmission is continuously monitored for correct amounts of incoming data bits. If within one frame of data the number of SPI CLK high transitions is not equal to a multiple of 16 (16,32,48,...), then the SPI error bit in the status register is set and the ERRB pin goes low to indicate this error to the micro controller. During this fault condition the incoming data are not loaded into the internal registers and the transmit shift register is not loaded with the requested data.

The status of the SPI framing error is reset by an errorless received frame requesting for the motor controller status register 0. This request will reset the SPI error bit and releases the ERRB pin (high).

### Error Output

This is an open drain output to flag a problem to the external microcontroller. The signal on this output is active low and the logic combination of:

NOT(ERRB) = (<SPI> OR <SHORT> OR <OPENX> OR <OPENY> OR <TSD> OR <TW> OR <STALL> OR (BemfIntEn AND BemfRes) OR (UV1IntEn AND UV1) OR (UV2IntEn AND UV2) OR (UV2MIntEn AND UV2M) OR (UV3IntEn AND UV3) OR (UV3MIntEn AND UV3M) OR (\*)reset state) AND not (\*\*)sleep mode

**Note:** (\*) reset state: After a power-on or a hard-reset, the ERRB is pulled low during  $t_{hr\_err}$  (Table 7 – AC PARAMETERS).

**Note:** (\*\*) sleep mode: In sleep mode the ERRB is always inactive (high).

### Sleep Mode

The motor driver can be put in a low-power consumption mode (sleep mode). The sleep mode is entered automatically

after a power-on or hard reset and can also be activated by means of SPI bit <SLP>. In sleep-mode, all analog circuits are suspended in low-power and all digital clocks are stopped: SPI communication is impossible. The motor driver is disabled (even if <MOTEN>=1), the content of all logic registers is maintained (including <MOTEN>, <TSD> and <TW>), all logic output pins are disabled (ERRB has no function) and none of the input pins are functional with the exception of pin CSB. Only this pin can wake-up the chip to normal mode (i.e. clear bit <SLP>) by means of a “high-to-low voltage” transition. After wake-up, time  $t_{wu}$  (see AC Table) is needed to restore analog and digital clocks and to bring SPI communication within specification.

### Notes:

- The hard-reset function is disabled in sleep mode.
- The thermal shutdown function will be “frozen” during sleep mode and re-activated at wake-up. This is important in case bit <TSD>=1 was cleared already by the micro and <TW> was not “0” yet.
- The CSB low pulse width has to be within  $t_{csb\_with}$ , (see AC Table) to guarantee a correct wake-up.

### Power-on Reset, Hard-Reset Function

After a power-on or a hard-reset, a flag <HR> in the SPI status register is set and the ERRB is pulled low. The ERRB stays low during this reset state. The typical power-on reset time is given by  $t_{hr\_err}$  (Table 7 – AC PARAMETERS). After the reset state the device enters sleep mode and the ERRB pin goes high to indicate the motor controller is ready for operation.

By means of a specific pattern on the DIR pin during the “Hold Mode”, the complete digital part of driver can be reset without a power-cycle. This hard-reset function is activated when the input pin DIR changes logic state “0 → 1 → 0 → 1” within  $t_{hr\_trig}$  in five consecutive patterns during “Hold Mode”. See figure below and Table 7 – AC PARAMETERS. With the device NCV70514MW007, the DIR change pattern can be alternatively created via the <DIRP> bit in SPI control register 1.

The operation of all analog circuits is suspended during the reset state of the digital. Similar as for a normal power-on, the flag <HR> is set in the SPI register after a hard-reset and the ERRB pin is pulled low during  $t_{hr\_err}$  (Table 7 – AC PARAMETERS).

To enable the motor controller to perform a proper self diagnosis, it is recommended that the motor is in “Hold Mode” before the hard reset is generated. The minimum time ( $t_{hr\_set}$ ) between the beginning of “Hold Mode” and the first rising edge of the DIR pin is given in Table 7 – AC PARAMETERS.

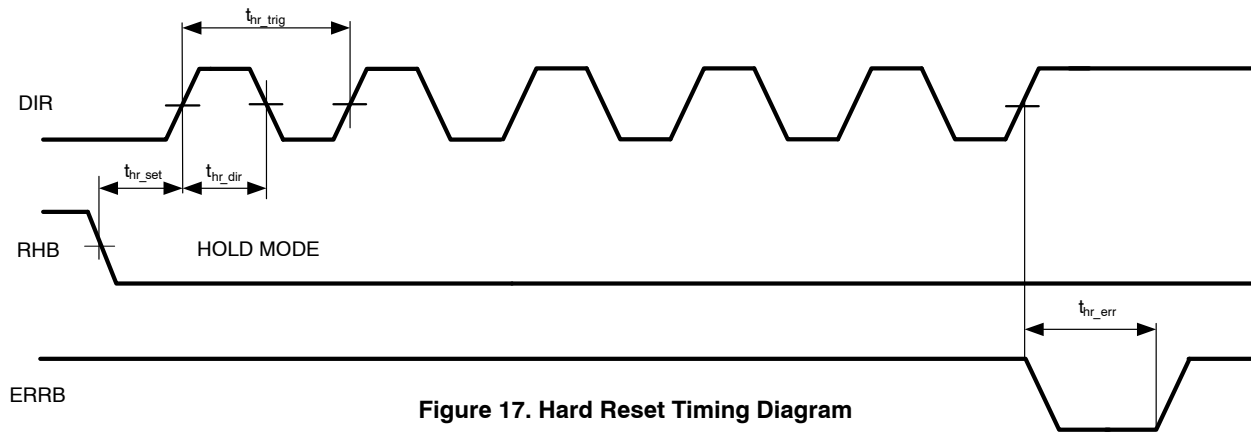


Figure 17. Hard Reset Timing Diagram

## SPI INTERFACE

The serial peripheral interface (SPI) is used to allow an external microcontroller (MCU) to communicate with the device. NCV70514 acts always as a slave and it cannot initiate any transmission. The operation of the device is configured and controlled by means of SPI registers, which are observable for read and/or write from the master. The NCV70514 SPI transfer size is 16 bits.

During an SPI transfer, the data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines:

DO and DI. The DO signal is the output from the Slave (NCV70514), and the DI signal is the output from the Master. A slave or chip select line (CSB) allows individual selection of a slave SPI device in a time multiplexed multiple-slave system.

The CSB line is active low. If an NCV70514 is not selected, DO is in high impedance state and it does not interfere with SPI bus activities. Since the NCV70514 always clocks data out on the falling edge and samples data in on rising edge of clock, the MCU SPI port must be configured to match this operation.

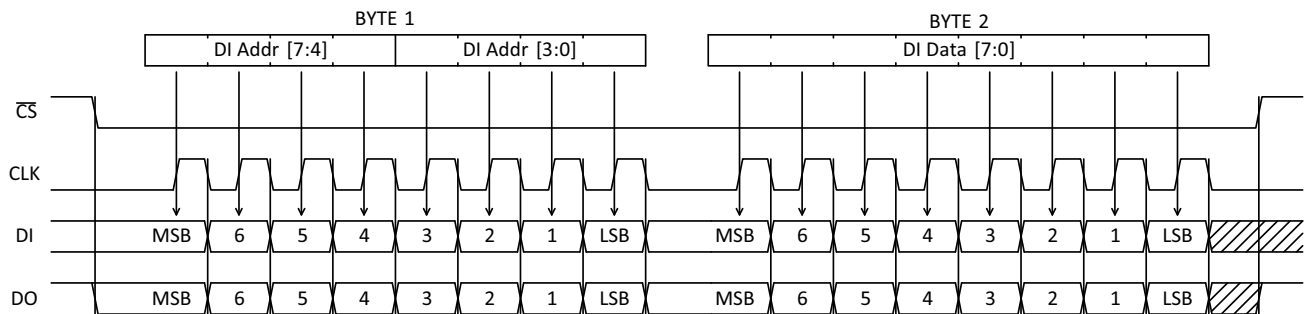


Figure 18. SPI Frame Structure

The implemented SPI allows connection to multiple slaves by means of both time-multiplexing (CSB per slave) and daisy-chain (CSB per group of slaves). Multi-axis connections schemes are discussed in a separate chapter below.

## SPI Transfer Format and Pin Signals

All SPI commands (to DI pin of NCV70514) from the micro controller consist of one “address byte” and one “data byte”. The address byte contains up to two addresses of each 4 bit long. These addresses are pointing to a command or requested action in a SPI slave. Three command-types can be distinguished: “Write to a control register”, “Read from a control register” and “Read from a status register”.

- Writing to a control register is accomplished only if the address of the target register appears in the first half of the address byte. The contents of the data-byte will be

copied in the control register. The contents of the addressed control register will be sent back by the NCV70514 in the next SPI access.

- Reading from a control register is accomplished by putting its address in the second half of the address byte. The data byte has no function for this command.
- Reading from a status register is accomplished by putting its address either in the first or in the second half of the address byte. The data byte has no function for this command.

The response (from DO pin of NCV70514) on these commands is always 2 bytes long. The possible combinations of DI/DO and their use are summarized in the following Table 16. Figure 19 gives examples of the data streaming:



**Table 16. SPI COMMAND ADDRESS, DATA AND RESPONSE STRUCTURE**

| DI ADDR[7:4] | DI ADDR[3:0] | DI DATA[7:0] | DO BYTE1 | DO BYTE2 | Comment on Use           |
|--------------|--------------|--------------|----------|----------|--------------------------|
| ACR1         | ACR2         | DICR1        | DOCR1    | DOCR2    | Control and Status of CR |
| ACR1         | ASR1         | DICR1        | DOCR1    | DOSR1    | Control and Status of SR |
| ACR1         | Nop          | DICR1        | DOCR1    | 00h      | Control and no Status    |
| ASR1         | ACR1         | XXh          | DOSR1    | DOCR1    | Status of SR and CR      |
| ASR1         | ASR2         | XXh          | DOSR1    | DOSR2    | Status of SR and SR      |
| ASR1         | Nop          | XXh          | DOSR1    | 00h      | Status of SR             |
| Nop          | ACR1         | XXh          | 00h      | DOCR1    | Status of CR             |
| Nop          | ASR1         | XXh          | 00h      | DOSR1    | Status of SR             |
| Nop          | Nop          | XXh          | 00h      | 00h      | Dummy/Placeholder        |

With:

ACRx = Address of control register x

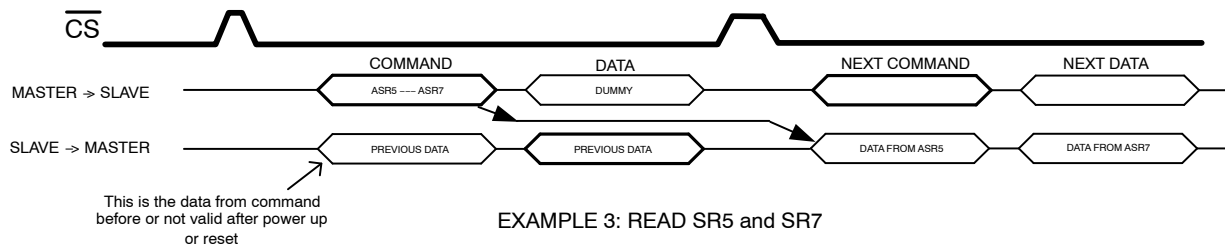
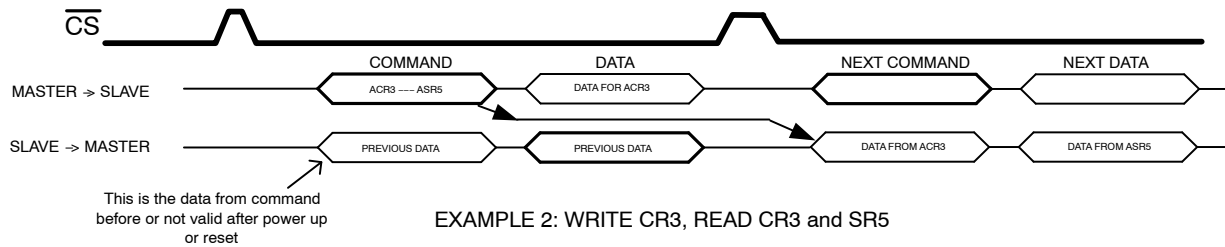
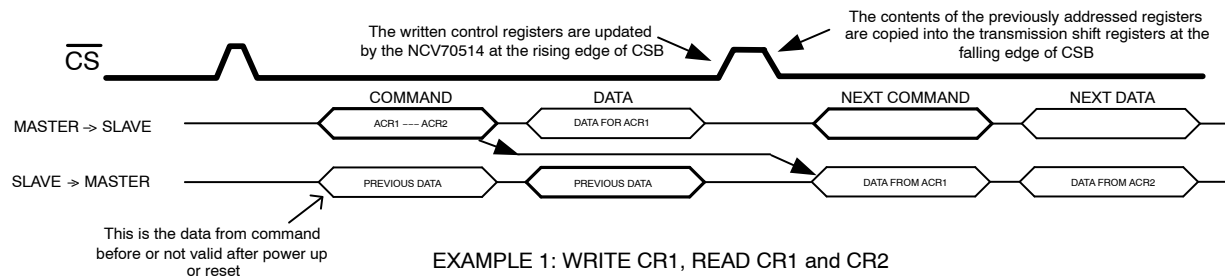
ASRx = Address of status register x

DICRx = Data input of Control Register x

DOxy = Data output of corresponding register contents transmitted in the next SPI access

Nop = Register address outside range : 0h

XXh = any byte



**Figure 19. Command and Data Streaming of SPI**

### SPI Control Registers (CR)

All SPI control registers have Read/Write access.

**Table 17. SPI CONTROL REGISTERS (CR)**

| 4-bit Address    | Bit 7      | Bit 6    | Bit 5         | Bit 4    | Bit 3    | Bit 2     | Bit 1    | Bit 0     | Default after Reset |
|------------------|------------|----------|---------------|----------|----------|-----------|----------|-----------|---------------------|
| 01h or 11h (CR1) | DIRP       | RHBP     | NXTP          | MOTEN    | StThr3   | StThr2    | StThr1   | StThr0    | 0000 0000           |
| 02h or 12h (CR2) | lhold3     | lhold2   | lhold1        | lhold0   | lrun3    | lrun2     | lrun1    | lrun0     | 0000 0000           |
| 03h or 13h (CR3) | EnhBemf En | DIAGEN   | EMC1          | EMC0     | SLP      | SM2       | SM1      | SM0       | 0010 0000           |
| 04h (CR4)        | StTo7      | StTo6    | StTo5         | StTo4    | StTo3    | StTo2     | StTo1    | StTo0     | 0001 0000           |
| 05h or 15h (CR5) | SpThr7     | SpThr6   | SpThr5        | SpThr4   | SpThr3   | SpThr2    | SpThr1   | SpThr0    | 0000 0000           |
| 06h or 16h (CR6) | UV1Thr3    | UV1Thr2  | UV1Thr1       | UV1Thr0  | UV2Thr3  | UV2Thr2   | UV2Thr1  | UV2Thr0   | 0000 0000           |
| 07h or 17h (CR7) | AD4        | BemfGain | Bemf ResIntEn | UV1IntEn | UV2IntEn | UV2MIntEn | UV3IntEn | UV3MIntEn | 0000 0000           |
| 14h (CR4A)       | NotUsed    | NotUsed  | NotUsed       | lboost   | OpenDet1 | OpenDet0  | OpenDis  | OpenHiZ   | 0000 0100           |

NCV70514 responds on every incoming byte by shifting out the data stored on the last address sent via the bus. After POR the initial address is unknown, so the first data shifted out are undefined.

Table 18. BIT DEFINITION

| Symbol       | MAP position                         | Description                                                                                                                                                                                                                                                                                                     |
|--------------|--------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DIRP         | Bit 7 – ADDR_0x01 or 0x11 (CR1)      | Polarity of DIR pin, which controls direction status; DIRP = 1 inverts the logic polarity of the DIR pin)                                                                                                                                                                                                       |
| RHBP         | Bit 6 – ADDR_0x01 or 0x11 (CR1)      | Polarity of RHB pin, which controls RUN/HOLD status; RHBP = 1 inverts logic polarity of the RHB pin (Hold = NOT(RHB XOR <RHBP>))                                                                                                                                                                                |
| NXTP         | Bit 5 – ADDR_0x01 or 0x11 (CR1)      | Push button pin, generating next step in position table                                                                                                                                                                                                                                                         |
| MOTEN        | Bit 4 – ADDR_0x01 or 0x11 (CR1)      | Enables the H-bridges (motor activated in RUN or HOLD mode)                                                                                                                                                                                                                                                     |
| StThr[3:0]   | Bits [3:0] – ADDR_0x01 or 0x11 (CR1) | Threshold level for stall detection, when “0”, stall detection is disabled                                                                                                                                                                                                                                      |
| Ihold[3:0]   | Bits [7:4] – ADDR_0x02 or 0x12 (CR2) | Current amplitude in HOLD mode                                                                                                                                                                                                                                                                                  |
| Irun[3:0]    | Bits [3:0] – ADDR_0x02 or 0x12 (CR2) | Current amplitude in RUN mode                                                                                                                                                                                                                                                                                   |
| EnhBemfEn    | Bit 7 – ADDR_0x03 or 0x13 (CR3)      | Enhanced BEMF measurement functionality is activated when bit is set                                                                                                                                                                                                                                            |
| DIAGEN       | Bit 6 – ADDR_0x03 or 0x13 (CR3)      | Enables automatic diagnostic at rising edge of <MOTEN> bit                                                                                                                                                                                                                                                      |
| EMC[1:0]     | Bits [5:4] – ADDR_0x03 or 0x13 (CR3) | Voltage slope defining bits for motor driver switching                                                                                                                                                                                                                                                          |
| SLP          | Bit 3 – ADDR_0x03 or 0x13 (CR3)      | Places device in sleep mode with low current consumption (when 1)                                                                                                                                                                                                                                               |
| SM[2:0]      | Bits [2:0] – ADDR_0x03 or 0x13 (CR3) | Step mode selection                                                                                                                                                                                                                                                                                             |
| StTo[7:0]    | Bits [7:0] – ADDR_0x04 (CR4)         | Max difference between two successive full step next pulse periods (time-out), after this time the BEMF sample is taken to verify stall                                                                                                                                                                         |
| SpThr[7:0]   | Bits [7:0] – ADDR_0x05 or 0x15 (CR5) | Speed threshold register, BEMF measurement and stall detection is activated when Speed register value is less than or equal to <SpThr> value                                                                                                                                                                    |
| UV1Thr[3:0]  | Bits [7:4] – ADDR_0x06 or 0x16 (CR6) | Setting of under voltage level UV1. See chapter UV detection                                                                                                                                                                                                                                                    |
| UV2Thr[3:0]  | Bits [3:0] – ADDR_0x06 or 0x16 (CR6) | Setting of under voltage level UV2. See chapter UV detection                                                                                                                                                                                                                                                    |
| AD4          | Bit 7 – ADDR_0x07 or 0x17 (CR7)      | Address selection bit, alternating register “Banks”. When AD = 1, all addresses will be interpreted with a “1” in the first nibble (allowing to access registers CR4A, SR7A, SR8A). When AD = 0, all addresses will be interpreted with a “0” in the first nibble (allowing to access registers CR4, SR7, SR8). |
| BemfGain     | Bit 6 – ADDR_0x07 or 0x17 (CR7)      | Gain of BEMF measurement channel – “0”: gain 0.5, “1”: gain 0.25                                                                                                                                                                                                                                                |
| BemfResIntEn | Bit 5 – ADDR_0x07 or 0x17 (CR7)      | BEMF result interrupt enable                                                                                                                                                                                                                                                                                    |
| UV1IntEn     | Bit 4 – ADDR_0x07 or 0x17 (CR7)      | Under voltage 1 detection interrupt enable                                                                                                                                                                                                                                                                      |
| UV2IntEn     | Bit 3 – ADDR_0x07 or 0x17 (CR7)      | Under voltage 2 detection interrupt enable                                                                                                                                                                                                                                                                      |
| UV2MIntEn    | Bit 2 – ADDR_0x07 or 0x17 (CR7)      | Under voltage 2 detection and Motion interrupt enable                                                                                                                                                                                                                                                           |
| UV3IntEn     | Bit 1 – ADDR_0x07 or 0x17 (CR7)      | Under voltage 3 detection interrupt enable                                                                                                                                                                                                                                                                      |
| UV3MIntEn    | Bit 0 – ADDR_0x07 or 0x17 (CR7)      | Under voltage 3 detection and Motion interrupt enable                                                                                                                                                                                                                                                           |
| Iboost       | Bit 4 – ADDR_0x14 (CR4A)             | Motor current boost function activation and status                                                                                                                                                                                                                                                              |
| OpenDet[1:0] | Bits [3:2] – ADDR_0x14 (CR4A)        | Open Coil detection time setting bits (see Table 7 – AC PARAMETERS)                                                                                                                                                                                                                                             |
| OpenDis      | Bit 1 – ADDR_0x14 (CR4A)             | When bit is set, Open Coil detection status is flagged, but drivers control remain active for both coils, <OpenDis> bit setting has higher priority than <OpenHiZ> bit                                                                                                                                          |
| OpenHiZ      | Bit 0 – ADDR_0x04 (CR4A)             | When bit is set, during Open Coil detection both drivers are deactivated (MOTEN=0)                                                                                                                                                                                                                              |

## SPI Status Registers (SR)

All SPI status registers have Read Only Access, with the odd parity on Bit7. Parity bit makes the numbers of 1 in the byte odd.

**Table 19. SPI STATUS REGISTERS (SR)**

| 4-bit Address    | Bit 7 | Bit 6       | Bit 5      | Bit 4      | Bit 3     | Bit 2     | Bit 1     | Bit 0     | Comment              | Default after Reset |
|------------------|-------|-------------|------------|------------|-----------|-----------|-----------|-----------|----------------------|---------------------|
| 08h or 18h (SR1) | PAR   | SPI,L       | SHORT,R*   | OPEN,R*    | TSD,L     | TW,R      | STALL,L   | HR,L      | Errors               | 0xx 0001            |
| 09h or 19h (SR2) | PAR   | ORErr, R    | BemfRes    | UV1,L      | UV2,L     | UV2M,L    | UV3,L     | UV3M,L    | INTst                | 101 1010            |
| 0Ah or 1Ah (SR3) | PAR   | MSP6,R      | MSP5,R     | MSP4,R     | MSP3,R    | MSP2,R    | MSP1,R    | MSP0,R    | Micro-step position  | 001 0000            |
| 0Bh or 1Bh (SR4) | PAR   | BemfCoil, R | Bemfs, R   | Bemf4, R   | Bemf3, R  | Bemf2, R  | Bemf1, R  | Bemf0, R  | Bemf                 | x00 0000            |
| 0Ch or 1Ch (SR5) | Sp7,R | Sp6,R       | Sp5,R      | Sp4,R      | Sp3,R     | Sp2,R     | Sp1,R     | Sp0,R     | Speed                | 1111 1111           |
| 0Dh or 1Dh (SR6) | PAR   | SI6,L       | SI5,L      | SI4,L      | SI3,L     | SI2,L     | SI1,L     | SI0,L     | StepLoss             | 000 0000            |
| 0Eh (SR7)        | PAR   | T/BX,R      | SignX,R    | PWMX4,R    | PWMX3,R   | PWMX2,R   | PWMX1,R   | PWMX0,R   | PWMX                 | 000 0000            |
| 0Fh (SR8)        | PAR   | T/BY,R      | SignY,R    | PWMY4,R    | PWMY3,R   | PWMY2,R   | PWMY1,R   | PWMY0,R   | PWMY                 | 000 0000            |
| 1Eh (SR7A)       | PAR   | OPENX,L     | STEP0pin,R | STEP1pin,R | SHRTXPB,L | SHRTXNB,L | SHRTXPT,L | SHRTXNT,L | Input pins & ShortsX | xxx 0000            |
| 1Fh (SR8A)       | PAR   | OPENY,L     | RHBpin,R   | DIRpin, R  | SHRTYPB,L | SHRTYNB,L | SHRTYPT,L | SHRTYNT,L | Input pins & ShortsY | xxx 0000            |

Flags have “L” for latched information or “R” for real time information. All latched flags are “cleared upon read”.

X = value after reset is defined during reset phase (diagnostics)

R\* = real time read out of values of other latches. Reading out this R\* value does not reset the bit, and does not reset the values of the latches this bit reads out.

**Table 20. BIT DEFINITION**

| Symbol  | MAP Position                    | Description                                                                                           |
|---------|---------------------------------|-------------------------------------------------------------------------------------------------------|
| PAR     | Bit 7 – ADDR_0x08 or 0x18 (SR1) | Parity bit for SR1                                                                                    |
| SPI     | Bit 6 – ADDR_0x08 or 0x18 (SR1) | SPI error: no multiple of 16 rising clock edges between falling and rising edge of CSB line           |
| SHORT   | Bit 5 – ADDR_0x08 or 0x18 (SR1) | An over current detected (common: set if at least one of the SHORTij individual bits is set)          |
| OPEN    | Bit 4 – ADDR_0x08 or 0x18 (SR1) | Open Coil X or Y detected (common: set if at least one of the two specific X/Y open coil bits is set) |
| TSD     | Bit 3 – ADDR_0x08 or 0x18 (SR1) | Thermal shutdown                                                                                      |
| TW      | Bit 2 – ADDR_0x08 or 0x18 (SR1) | Thermal warning                                                                                       |
| STALL   | Bit 1 – ADDR_0x08 or 0x18 (SR1) | Stall detected by the internal algorithm                                                              |
| HR      | Bit 0 – ADDR_0x08 or 0x18 (SR1) | Hard reset flag: 1 indicates a hard reset has occurred                                                |
| PAR     | Bit 7 – ADDR_0x09 or 0x19 (SR2) | Parity bit for SR2                                                                                    |
| ORErr   | Bit 6 – ADDR_0x09 or 0x19 (SR2) | Logic OR of all bits of SR1 (Error bits)                                                              |
| BemfRes | Bit 5 – ADDR_0x09 or 0x19 (SR2) | BEMF result ready at <Bemf> register                                                                  |
| UV1     | Bit 4 – ADDR_0x09 or 0x19 (SR2) | Under voltage 1 detection                                                                             |
| UV2     | Bit 3 – ADDR_0x09 or 0x19 (SR2) | Under voltage 2 detection                                                                             |
| UV2M    | Bit 2 – ADDR_0x09 or 0x19 (SR2) | Under voltage 2 detection and NXT pulse arrive during UV2 state (Motion)                              |
| UV3     | Bit 1 – ADDR_0x09 or 0x19 (SR2) | Under voltage 3 detection                                                                             |
| UV3M    | Bit 0 – ADDR_0x09 or 0x19 (SR2) | Under voltage 3 detection and NXT pulse arrive during UV3 state (Motion)                              |
| PAR     | Bit 7 – ADDR_0x0A or 0x1A (SR3) | Parity bit for SR3                                                                                    |

Table 20. BIT DEFINITION

| Symbol    | MAP Position                         | Description                                                                                                                                                                                                                                                     |
|-----------|--------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MSP[6:0]  | Bits [6:0] – ADDR_0x0A or 0x1A (SR3) | Translator micro-step position                                                                                                                                                                                                                                  |
| PAR       | Bit 7 – ADDR_0x0B or 0x1B (SR4)      | Parity bit for SR4                                                                                                                                                                                                                                              |
| BemfCoil  | Bit 6 – ADDR_0x0B or 0x1B (SR4)      | Last BEMF measurement was done on coil: 0 = X, 1 = Y                                                                                                                                                                                                            |
| Bemfs     | Bit 5 – ADDR_0x0B or 0x1B (SR4)      | BEMF measured voltage has expected polarity (Yes = 0, No = 1)                                                                                                                                                                                                   |
| Bemf[4:0] | Bits [4:0] – ADDR_0x0B or 0x1B (SR4) | BEMF value measured during zero crossing                                                                                                                                                                                                                        |
| Sp[7:0]   | Bits [7:0] – ADDR_0x0C or 0x1C (SR5) | Speed register                                                                                                                                                                                                                                                  |
| PAR       | Bit 7 – ADDR_0x0D or 0x1D (SR6)      | Parity bit for SR6                                                                                                                                                                                                                                              |
| Sl[6:0]   | Bits [6:0] – ADDR_0x0D or 0x1D (SR6) | Step loss register counts number of NXT pulses arrived after activation of under-voltage event or other failure state when NXT pulses are ignored (e.g. TSD, OVC, STALL). Counter keeps maximum value of 127 after more pulses have been received (no overflow) |
| PAR       | Bit 7 – ADDR_0x0E (SR7)              | Parity bit for SR7                                                                                                                                                                                                                                              |
| T/BX      | Bit 6 – ADDR_0x0E (SR7)              | PWM Regulation mode on X coil (Top = 1 or Bottom = 0 regulation)                                                                                                                                                                                                |
| SignX     | Bit 5 – ADDR_0x0E (SR7)              | PWM sign for X coil regulation (“0” = positive, “1” = negative)                                                                                                                                                                                                 |
| PWMX[4:0] | Bits [4:0] – ADDR_0x0E (SR7)         | Actual PWM duty cycle value for coil X                                                                                                                                                                                                                          |
| PAR       | Bit 7 – ADDR_0x0F (SR8)              | Parity bit for SR8                                                                                                                                                                                                                                              |
| T/BY      | Bit 6 – ADDR_0x0F (SR8)              | PWM Regulation mode on Y coil (Top = 1 or Bottom = 0 regulation)                                                                                                                                                                                                |
| SignY     | Bit 5 – ADDR_0x0F (SR8)              | PWM sign for Y coil regulation (“0” = positive, “1” = negative)                                                                                                                                                                                                 |
| PWMY[4:0] | Bits [4:0] – ADDR_0x0F (SR8)         | Actual PWM duty cycle value for coil Y                                                                                                                                                                                                                          |
| PAR       | Bit 7 – ADDR_0x1E (SR7A)             | Parity bit for SR7A                                                                                                                                                                                                                                             |
| OPENX     | Bit 6 – ADDR_0x1E (SR7A)             | Open Coil X detected                                                                                                                                                                                                                                            |
| STEP0pin  | Bit 5 – ADDR_0x1E (SR7A)             | Read out of STEP0 pin logic status                                                                                                                                                                                                                              |
| STEP1pin  | Bit 4 – ADDR_0x1E (SR7A)             | Read out of STEP1 pin logic status                                                                                                                                                                                                                              |
| SHRTXPB   | Bit 3 – ADDR_0x1E (SR7A)             | Short circuit detected at XP pin towards ground (Bottom)                                                                                                                                                                                                        |
| SHRTXNB   | Bit 2 – ADDR_0x1E (SR7A)             | Short circuit detected at XN pin towards ground (Bottom)                                                                                                                                                                                                        |
| SHRTXPT   | Bit 1 – ADDR_0x1E (SR7A)             | Short circuit detected at XP pin towards supply (Top)                                                                                                                                                                                                           |
| SHRTXNT   | Bit 0 – ADDR_0x1E (SR7A)             | Short circuit detected at XN pin towards supply (Top)                                                                                                                                                                                                           |
| PAR       | Bit 7 – ADDR_0x1F (SR8A)             | Parity bit for SR8A                                                                                                                                                                                                                                             |
| OPENY     | Bit 6 – ADDR_0x1F (SR8A)             | Open Coil Y detected                                                                                                                                                                                                                                            |
| RHBpin    | Bit 5 – ADDR_0x1F (SR8A)             | Read out of RHB pin logic status                                                                                                                                                                                                                                |
| DIRpin    | Bit 4 – ADDR_0x1F (SR8A)             | Read out of DIR pin logic status                                                                                                                                                                                                                                |
| SHRTYPB   | Bit 3 – ADDR_0x1F (SR8A)             | Short circuit detected at YP pin towards ground (Bottom)                                                                                                                                                                                                        |
| SHRTYNB   | Bit 2 – ADDR_0x1F (SR8A)             | Short circuit detected at YN pin towards ground (Bottom)                                                                                                                                                                                                        |
| SHRTYPT   | Bit 1 – ADDR_0x1F (SR8A)             | Short circuit detected at YP pin towards supply (Top)                                                                                                                                                                                                           |
| SHRTYNT   | Bit 0 – ADDR_0x1F (SR8A)             | Short circuit detected at YN pin towards supply (Top)                                                                                                                                                                                                           |

## APPLICATION EXAMPLES FOR MULTI-AXIS CONTROL

The wiring diagrams below show possible connections of multiple slaves to one microcontroller. In these examples, all movements of the motors are synchronized by means of a common NXT wire. The direction and Run/Hold activation is controlled by means of an SPI bus.

Further I/O reduction is accomplished in case the ERRB is not connected. This would mean that the microcontroller operates while polling the error flags of the slaves. Ultimately, one can operate multiple slaves by means of only 4 SPI connections: even the NXT pin can be avoided if the microcontroller operates the motors by means of the “NXT” bit.

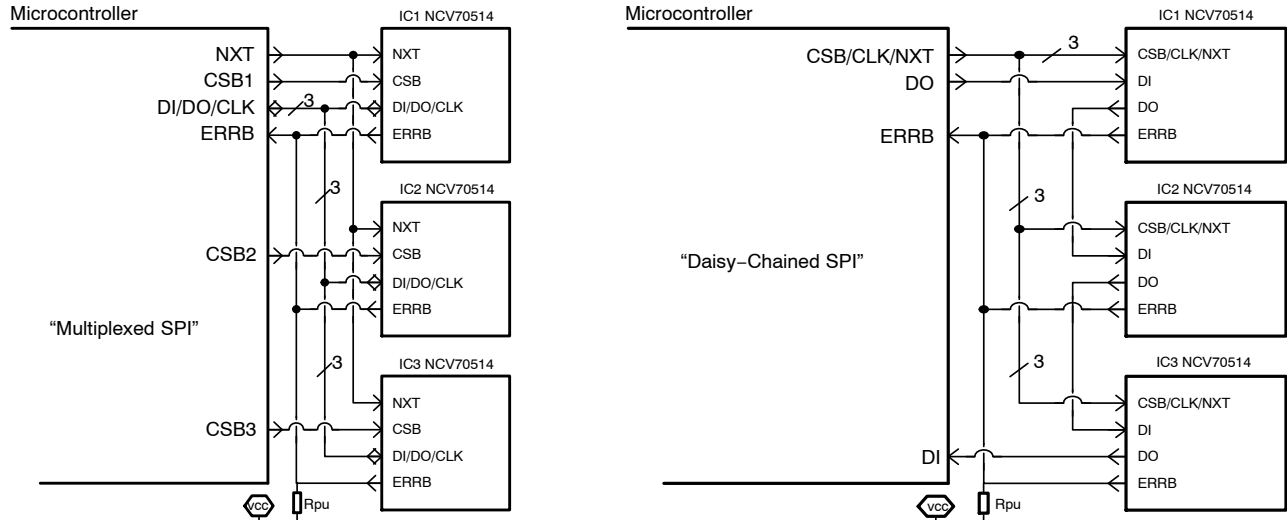


Figure 20. Examples of Wiring Diagrams for Multi-axis Control\*

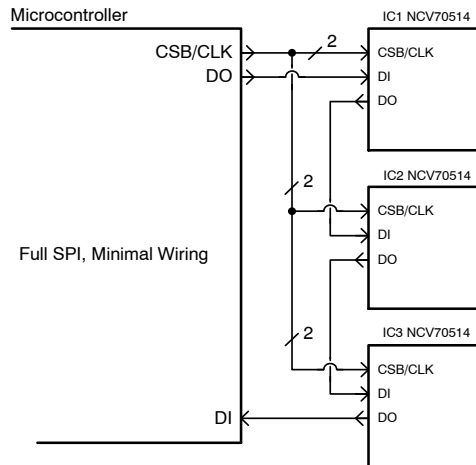


Figure 21. Minimal Wiring Diagram for Multi-axis Control\*

\*This drawing does not present the Hard Reset interconnection. For the functionality of the Hard Reset function the RHB and DIR pins have to be connected to the micro controller.

## ELECTRO MAGNETIC COMPATIBILITY

The NCV70514 has been developed using state-of-the-art design techniques for EMC. The overall system performance depends on multiple aspects of the system (IC design & lay-out, PCB design and layout ...) of which some are not solely under control of the IC manufacturer. Therefore, meeting system EMC requirements can only happen in collaboration with all involved parties.

Special care has to be taken into account with long wiring to motors and inductors. A modern methodology to regulate the current in inductors and motor windings is based on controlling the motor voltage by PWM. This low frequency switching of the battery voltage is present at the wiring towards the motor or windings. To reduce possible radiated transmission, it is advised to use twisted pair cable and/or shielded cable.

## PCB LAYOUT RECOMMENDATIONS

Recommended PCB layout for the NCV70514 is shown on the following figure. The VDD capacitor C4 must be placed close to the device and with GND straight to the

device and not the common GND. This is crucial for optimum EMC performance.

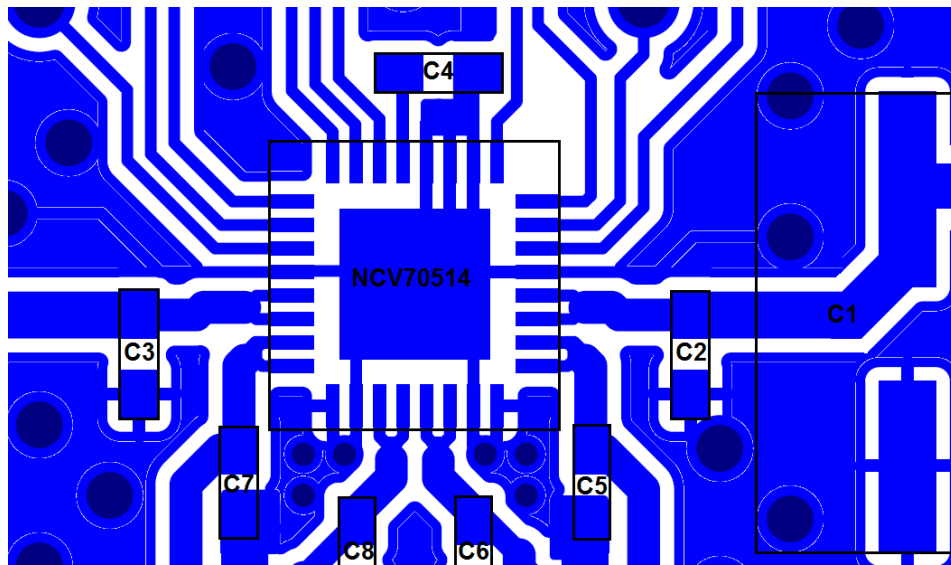


Figure 22. Recommended PCB Layout

# NCV70514

## ORDERING INFORMATION

| Device              | Marking  | Peak Current | Boost Peak Current | End Market/Version                  | Package*                                          | Shipping†          |
|---------------------|----------|--------------|--------------------|-------------------------------------|---------------------------------------------------|--------------------|
| NCV70514MW003BR2G   | N70514-3 | 800 mA       | N.A.               | Automotive High Temperature Version | QFNW32 5x5 with step-cut wettable flank (Pb-Free) | 5000 / Tape & Reel |
| NCV70514MW007AR2G** | N70514-7 | 800 mA       | 1100 mA            |                                     | QFNW32 5x5 with step-cut wettable flank (Pb-Free) | 5000 / Tape & Reel |

## DISCONTINUED (Note 29)

|                  |          |        |         |                                     |                                          |                    |
|------------------|----------|--------|---------|-------------------------------------|------------------------------------------|--------------------|
| NCV70514MW007R2G | N70514-7 | 800 mA | 1100 mA | Automotive High Temperature Version | QFN32 5x5 with wettable flanks (Pb-Free) | 5000 / Tape & Reel |
|------------------|----------|--------|---------|-------------------------------------|------------------------------------------|--------------------|

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

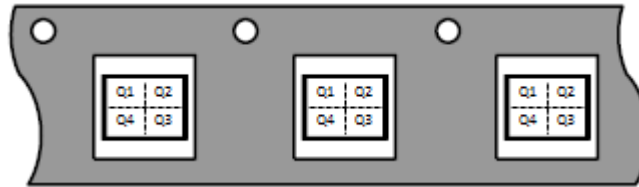
\*Devices NCV70514MW003 and NCV70514MW007 have different package mold compound. Please contact **onsemi** for technical details.

\*\*NCV70514MW007A is recommended for new designs.

29. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on [www.onsemi.com](http://www.onsemi.com).

## PIN 1 ORIENTATION IN TAPE AND REEL

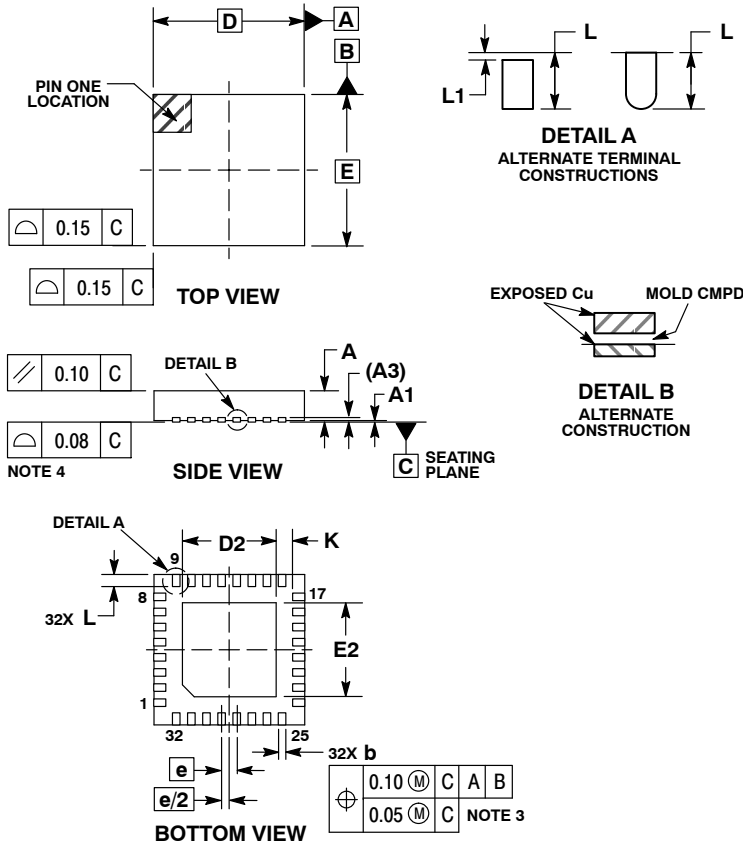
Direction of Feed





PACKAGE DIMENSIONS

QFN32 5x5, 0.5P  
CASE 488AM  
ISSUE A

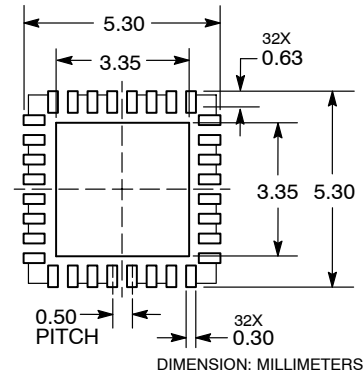


NOTES:

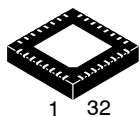
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN         | MAX  |
| A   | 0.80        | 1.00 |
| A1  | ---         | 0.05 |
| A3  | 0.20        | REF  |
| b   | 0.18        | 0.30 |
| D   | 5.00        | BSC  |
| D2  | 2.95        | 3.25 |
| E   | 5.00        | BSC  |
| E2  | 2.95        | 3.25 |
| e   | 0.50        | BSC  |
| K   | 0.20        | ---  |
| L   | 0.30        | 0.50 |
| L1  | ---         | 0.15 |

RECOMMENDED  
SOLDERING FOOTPRINT\*



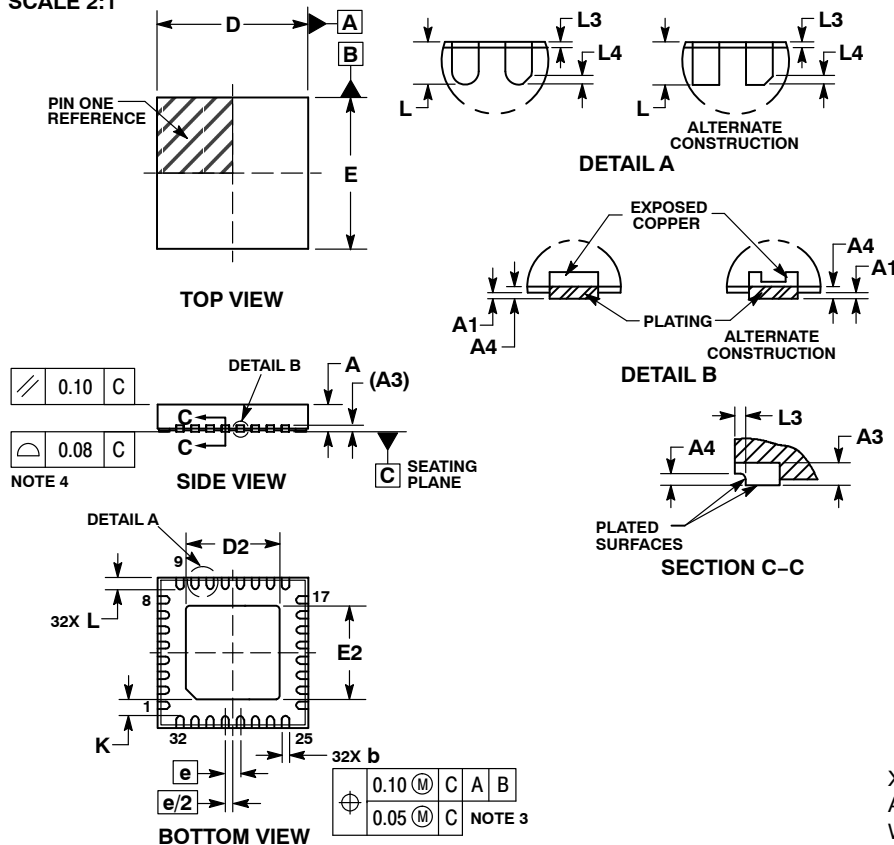
\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



1 32  
SCALE 2:1

**QFNW32 5x5, 0.5P**  
**CASE 484AB**  
**ISSUE D**

DATE 07 SEP 2018

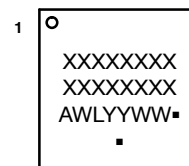


#### NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.20MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS |      |          |      |
|-------------|------|----------|------|
| DIM         | MIN  | NOM      | MAX  |
| A           | 0.80 | 0.90     | 1.00 |
| A1          |      |          | 0.05 |
| A3          |      | 0.20 REF |      |
| A4          | 0.10 |          |      |
| b           | 0.20 | 0.25     | 0.30 |
| D           | 4.90 | 5.00     | 5.10 |
| D2          | 3.00 | 3.10     | 3.20 |
| E           | 4.90 | 5.00     | 5.10 |
| E2          | 3.00 | 3.10     | 3.20 |
| e           |      | 0.50 BSC |      |
| K           | 0.35 |          |      |
| L           | 0.30 | 0.40     | 0.50 |
| L3          |      |          | 0.10 |
| L4          |      | 0.08 REF |      |

#### GENERIC MARKING DIAGRAM\*

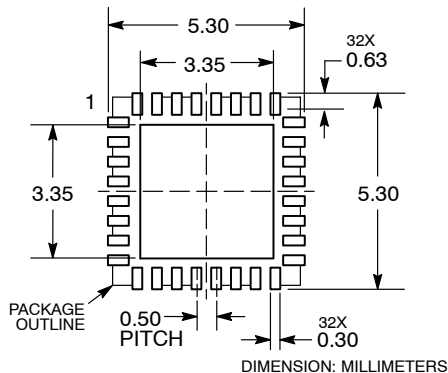


XXXXXX = Specific Device Code  
 A = Assembly Location  
 WL = Wafer Lot  
 YY = Year  
 WW = Work Week  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "C" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

#### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                         |                         |                                                                                                                                                                                  |
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