

# FlexRay® Transceiver, Clamp 30

## NCV7381

NCV7381 is a single-channel FlexRay bus driver compliant with the FlexRay Electrical Physical Layer Specification Rev. 3.0.1, capable of communicating at speeds of up to 10 Mbit/s. It provides differential transmit and receive capability between a wired FlexRay communication medium on one side and a protocol controller and a host on the other side.

NCV7381 mode control functionality is optimized for nodes permanently connected to car battery.

It offers excellent EMC and ESD performance.

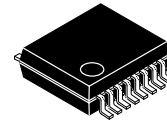
### KEY FEATURES

#### General

- Compliant with FlexRay Electrical Physical Layer Specification Rev 3.0.1
- FlexRay Transmitter and Receiver in Normal-power Modes for Communication up to 10 Mbit/s
- Support of 60 ns Bit Time
- FlexRay Low-power Mode Receiver for Remote Wakeup Detection
- Excellent Electromagnetic Susceptibility (EMS) Level over Full Frequency Range. Very Low Electromagnetic Emissions (EME)
- Bus Pins Protected against >10 kV System ESD Pulses
- Safe Behavior under Missing Supply or No Supply Conditions
- Interface Pins for a Protocol Controller and a Host (TxD, RxD, TxEN, RxEN, STBN, BGE, EN, ERRN)
- INH Output for Control of External Regulators
- Local Wakeup Pin WAKE
- TxEN Time-out
- BGE Feedback
- Supply Pins V<sub>BAT</sub>, V<sub>CC</sub>, V<sub>IO</sub> with Independent Voltage Ramp Up:
  - ♦ V<sub>BAT</sub> Supply Parametrical Range from 5.5 V to 50 V
  - ♦ V<sub>CC</sub> Supply Parametrical Range from 4.75 V to 5.25 V
  - ♦ V<sub>IO</sub> Supply Parametrical Range from 2.3 V to 5.25 V
- Compatible with 14 V and 28 V Systems
- Operating Ambient Temperature -40°C to +125°C (T<sub>AMB\_Class1</sub>)
- Junction Temperature Monitoring with Two Levels
- SSOP-16 Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

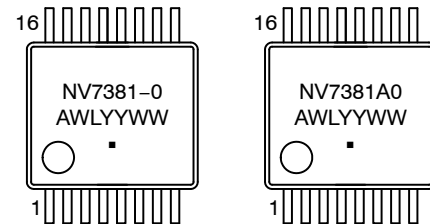
#### FlexRay Functional Classes

- Bus Driver Voltage Regulator Control
- Bus Driver – Bus Guardian Interface
- Bus Driver Logic Level Adaptation
- Bus Driver Remote Wakeup



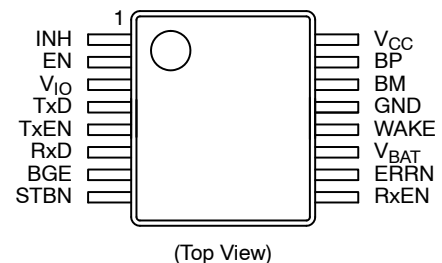
SSOP-16  
DP SUFFIX  
CASE 565AE

### MARKING DIAGRAM



A = Assembly Location  
 WL = Wafer Lot  
 YYWW = Year / Work Week  
 ■ = Pb-Free Package

### PIN CONNECTIONS



(Top View)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 21 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 21.

### Quality

- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

# NCV7381

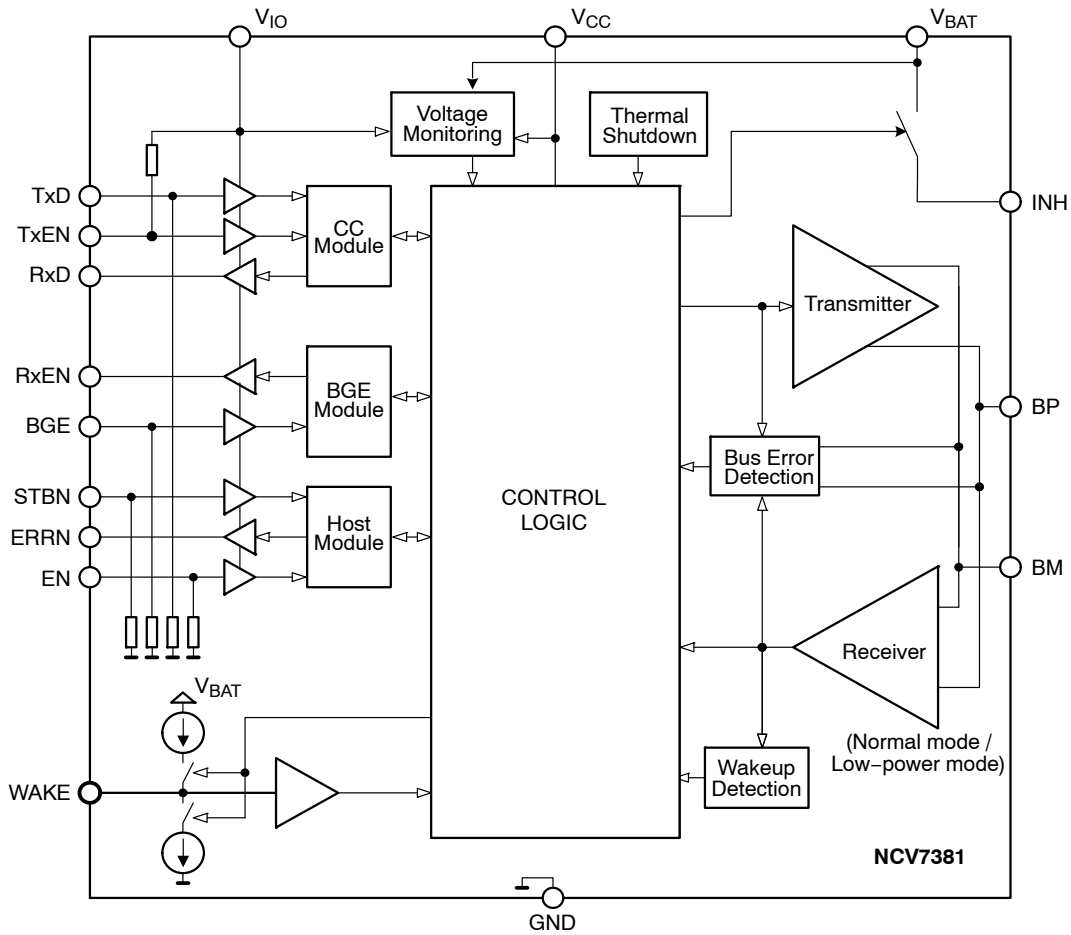


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

| Pin Number | Pin Name         | Pin Type                         | Pin Function                                                                          |
|------------|------------------|----------------------------------|---------------------------------------------------------------------------------------|
| 1          | INH              | high-voltage analog output       | External regulator control output                                                     |
| 2          | EN               | digital input                    | Mode control input; internal pull-down resistor                                       |
| 3          | V <sub>IO</sub>  | supply                           | Supply voltage for digital pins level adaptation                                      |
| 4          | TxD              | digital input                    | Data to be transmitted; internal pull-down resistor                                   |
| 5          | TxEN             | digital input                    | Transmitter enable input; when High transmitter disabled; internal pull-up resistor   |
| 6          | RxD              | digital output                   | Receive data output                                                                   |
| 7          | BGE              | digital input                    | Bus guardian enable input; when Low transmitter disabled; internal pull-down resistor |
| 8          | STBN             | digital input                    | Mode control input; internal pull-down resistor                                       |
| 9          | RxEN             | digital output                   | Bus activity detection output; when Low bus activity detected                         |
| 10         | ERRN             | digital output                   | Error diagnosis and status output                                                     |
| 11         | V <sub>BAT</sub> | supply                           | Battery supply voltage                                                                |
| 12         | WAKE             | high-voltage analog input        | Local wake up input; internal pull up or pull down (depends on voltage at pin WAKE)   |
| 13         | GND              | ground                           | Ground connection                                                                     |
| 14         | BM               | high-voltage analog input/output | Bus line minus                                                                        |
| 15         | BP               | high-voltage analog input/output | Bus line plus                                                                         |
| 16         | V <sub>CC</sub>  | supply                           | Bus driver core supply voltage; 5 V nominal                                           |

APPLICATION INFORMATION

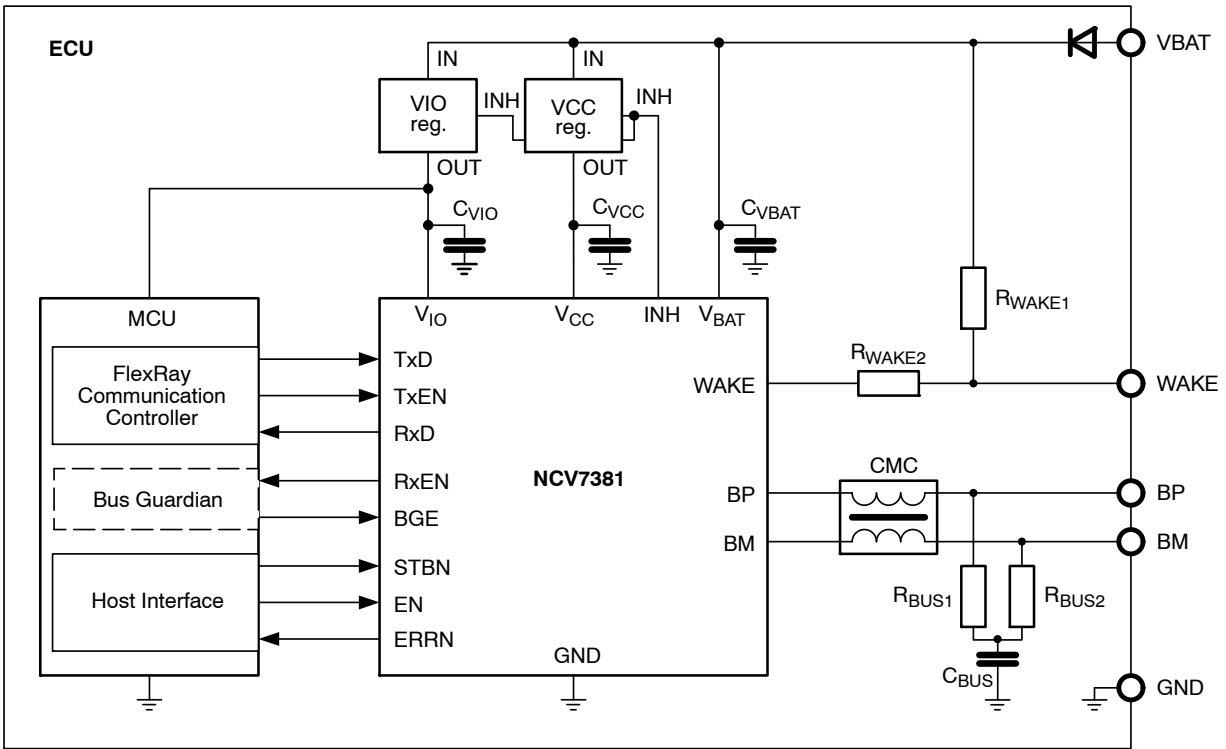


Figure 2. Application Diagram

Table 2. RECOMMENDED EXTERNAL COMPONENTS FOR THE APPLICATION DIAGRAM

| Component          | Function                                                     | Min | Typ  | Max | Unit |
|--------------------|--------------------------------------------------------------|-----|------|-----|------|
| C <sub>VBAT</sub>  | Decoupling capacitor on battery line, ceramic                |     | 100  |     | nF   |
| C <sub>VCC</sub>   | Decoupling capacitor on V <sub>CC</sub> supply line, ceramic |     | 100  |     | nF   |
| C <sub>VIO</sub>   | Decoupling capacitor on V <sub>IO</sub> supply line, ceramic |     | 100  |     | nF   |
| R <sub>WAKE1</sub> | Pull-up resistor on WAKE pin                                 |     | 33   |     | kΩ   |
| R <sub>WAKE2</sub> | Serial protection resistor on WAKE pin                       |     | 3.3  |     | kΩ   |
| R <sub>BUS1</sub>  | Bus termination resistor (Note 1)                            |     | 47.5 |     | Ω    |
| R <sub>BUS2</sub>  | Bus termination resistor (Note 1)                            |     | 47.5 |     | Ω    |
| C <sub>BUS</sub>   | Common-mode stabilizing capacitor, ceramic (Note 2)          |     | 4.7  |     | nF   |
| CMC                | Common-mode choke                                            |     | 100  |     | μH   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Tolerance ±1%, type 0805

2. Tolerance ±20%, type 0805

NCV7381 can switch between several operating modes depicted in Figure 3. In Normal and Receive-only modes, the chip interconnects a FlexRay communication controller with the bus medium for full-speed communication. These two modes are also referred to as normal-power modes.

correct transition between any mode and the Sleep mode. All three modes – Standby, Sleep and Go-to-sleep – are referred to as low-power modes.

The operating mode selected is a function of the host signals STBN and EN, the state of the supply voltages and the wakeup detection. As long as all three supplies ( $V_{BAT}$ ,  $V_{CC}$ ,  $V_{IO}$ ) remain above their respective under-voltage detection levels, the logical control by EN and STBN pins shown in Figure 3 applies. Influence of the power-supplies and of the wakeup detection on the operating modes is described in subsequent paragraphs.



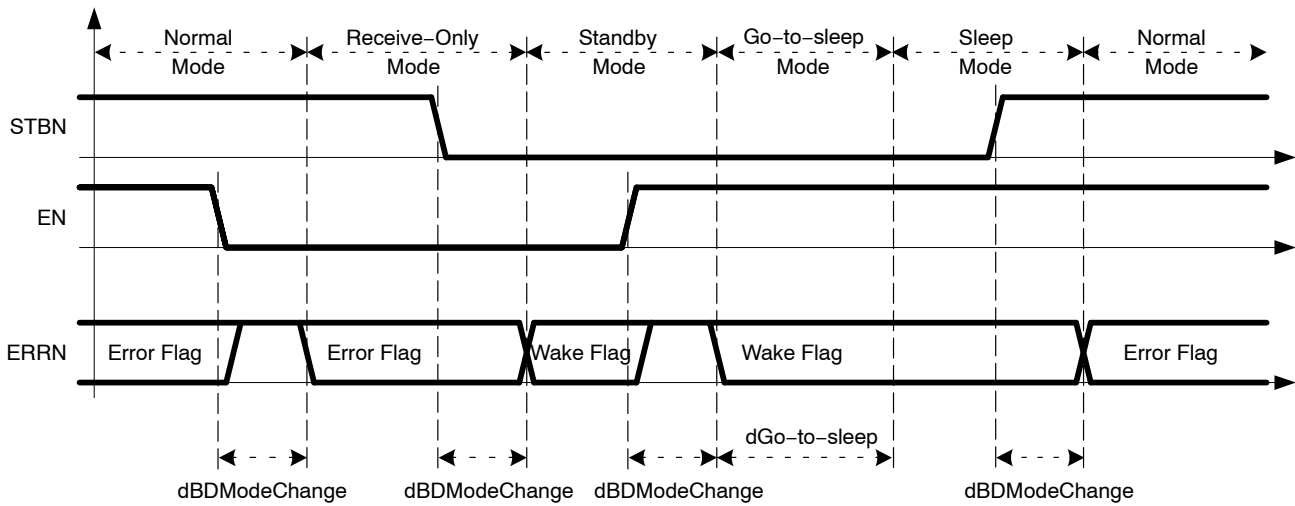


Figure 4. Timing Diagram of Operating Modes Control by the STBN and EN Pins

#### Power Supplies and Power Supply Monitoring

NCV7381 is supplied by three pins.  $V_{BAT}$  is the main supply both for NCV7381 and the full electronic module.  $V_{BAT}$  will be typically connected to the automobile battery through a reverse-polarity protection.  $V_{CC}$  is a 5 V low-voltage supply primarily powering the FlexRay bus driver core in a normal-power mode.  $V_{IO}$  supply serves to adapt the logical levels of NCV7381 to the host and/or the FlexRay communication controller digital signal levels. All supplies should be properly decoupled by filtering capacitors – see Figure 2 and Table 2.

All three supplies are monitored by under-voltage detectors with individual thresholds and filtering times both for under-voltage detection and recovery – see Table 18.

#### Logic Level Adaptation

Level shift input  $V_{IO}$  is used to apply a reference voltage  $uV_{DIG} = uV_{IO}$  to all digital inputs and outputs in order to adapt the logical levels of NCV7381 to the host and/or the FlexRay communication controller digital signal levels

### Internal Flags

The NCV7381 control logic uses a number of internal flags (i.e. one-bit memories) reflecting important conditions or events. Table 3 summarizes the individual flags and the conditions that lead to a set or reset of the flags.

**Table 3. INTERNAL FLAGS**

| Flag                    | Set Condition                                                                                                                                                                                             | Reset Condition                                                                                                                                                                                              | Comment                                                                 |
|-------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------|
| Local Wakeup            | Low level detected on WAKE pin in a low-power mode                                                                                                                                                        | Low-power mode is entered                                                                                                                                                                                    |                                                                         |
| Remote Wakeup           | Remote wakeup detected on the bus in a low-power mode                                                                                                                                                     | Low-power mode is entered                                                                                                                                                                                    |                                                                         |
| Wakeup                  | Local Wakeup flag changes to set<br>or<br>Remote Wakeup flag changes to set                                                                                                                               | Normal mode is entered<br>or<br>Low-power mode is entered<br>or<br>Any under-voltage flag becomes set                                                                                                        |                                                                         |
| Power-on                | Internal power supply of the chip becomes sufficient for the operation of the control logic                                                                                                               | Normal mode is entered                                                                                                                                                                                       |                                                                         |
| Thermal Warning         | Junction temperature is higher than $T_{jw}$ (typ. 140°C) in a normal-power mode and $V_{BAT}$ is not in under-voltage                                                                                    | (Junction temperature is below $T_{jw}$ in a normal-power mode<br>or<br>the status register is read in a low-power mode)<br>and<br>$V_{BAT}$ is not in under-voltage                                         | The thermal warning flag has no influence on the bus driver function    |
| Thermal Shutdown        | Junction temperature is higher than $T_{jwd}$ (typ. 165°C) in a normal-power mode and $V_{BAT}$ is not in under-voltage                                                                                   | Junction temperature is below $T_{jwd}$ in a normal-power mode<br>and<br>falling edge on TxEN<br>and<br>$V_{BAT}$ is not in under-voltage                                                                    | The transmitter is disabled as long as the thermal shutdown flag is set |
| TxEN Timeout            | TxEN is Low for longer than $dBdTxActiveMax$ (typ. 1.5 ms) and bus driver is in Normal mode                                                                                                               | TxEN is High or Normal mode is left                                                                                                                                                                          | The transmitter is disabled as long as the timeout flag is set          |
| Bus Error               | Transmitter is enabled and Data on bus are different from TxD signal (sampled after each TXD edge)                                                                                                        | (Transmitter is enabled and Data on bus are identical to TxD signal)<br>or<br>Transmitter is disabled                                                                                                        | The bus error flag has no influence on the bus driver function          |
| $V_{BAT}$ Under-voltage | $V_{BAT}$ is below the under-voltage threshold for longer than $dBdUVV_{BAT}$                                                                                                                             | $V_{BAT}$ is above the under-voltage threshold for longer than $dBdRV_{BAT}$<br>or<br>Wake flag becomes set                                                                                                  |                                                                         |
| $V_{CC}$ Under-voltage  | $V_{CC}$ is below the under-voltage threshold for longer than $dBdUVV_{CC}$                                                                                                                               | $V_{CC}$ is above the under-voltage threshold for longer than $dBdRV_{CC}$<br>or<br>Wake flag becomes set                                                                                                    |                                                                         |
| $V_{IO}$ Under-voltage  | $V_{IO}$ is below the under-voltage threshold for longer than $dUV_{IO}$                                                                                                                                  | $V_{IO}$ is above the under-voltage threshold for longer than $dBdRV_{IO}$<br>or<br>Wake flag becomes set                                                                                                    |                                                                         |
| Error                   | Any of the following status bits is set:<br>• Bus error<br>• Thermal Warning<br>• Thermal Shutdown<br>• TxEN Timeout<br>• $V_{BAT}$ Under-voltage<br>• $V_{CC}$ Under-voltage<br>• $V_{IO}$ Under-voltage | All of the following status bits are reset:<br>• Bus error<br>• Thermal Warning<br>• Thermal Shutdown<br>• TxEN Timeout<br>• $V_{BAT}$ Under-voltage<br>• $V_{CC}$ Under-voltage<br>• $V_{IO}$ Under-voltage |                                                                         |

### Operating Mode Changes Caused by Internal Flags

Changes of some internal flags described in Table 3 can force an operating mode transition complementing or overruling the operating mode control by the digital inputs STBN and EN which is shown in Figure 3:

- Setting the  $V_{BAT}$  or  $V_{IO}$  under-voltage flag causes a transition to the Sleep mode
- Setting the  $V_{CC}$  under-voltage flag, while the bus driver is not in Sleep, causes a transition to the Standby mode
- Reset of the Under-voltage flag (i.e. recovery from under-voltage) re-enables the control of the chip by digital inputs STBN and EN.
- Setting of the Wake flag causes the reset of all under-voltage flags and the NCV7381 transitions to the Standby mode. The reset of the under-voltage flags allows the external power supplies to stabilize properly if, for example, they were previously switched off during Sleep mode.

### FlexRay Bus Driver

NCV7381 contains a fully-featured FlexRay bus driver compliant with Electrical Physical Layer Specification Rev. 3.0.1. The transmitter part translates logical signals on digital inputs TxEN, BGE and TxD into appropriate bus levels on pins BP and BM. A transmission cannot be started with Data\_1. In case the transmitter is enabled for longer than  $dBDTxActiveMax$ , the TxEN Timeout flag is set and the current transmission is disabled. The receiver part monitors bus pins BP and BM and signals the detected levels on digital outputs RxD and RxEN. The different bus levels are defined in Figure 5. The function of the bus driver and the related digital pins in different operating modes is detailed in Table 4 and Table 5.

- The transmitter can only be enabled if the activation of the transmitter is initiated in Normal mode.
- The receiver function is enabled by entering a normal-power mode.

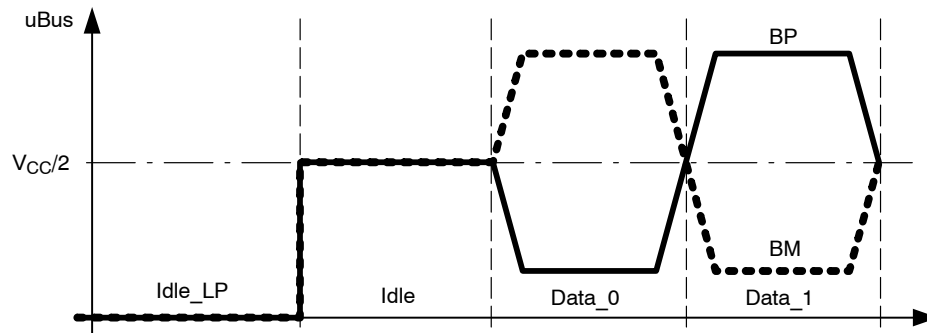


Figure 5. FlexRay Bus Signals

Table 4. TRANSMITTER FUNCTION AND TRANSMITTER-RELATED PINS

| Operating Mode              | BGE | TxEN | TxD | Transmitted Bus Signal |
|-----------------------------|-----|------|-----|------------------------|
| Standby, Go-to-sleep, Sleep | x   | x    | x   | Idle_LP                |
| Receive-only                | x   | x    | x   | Idle                   |
| Normal                      | 0   | x    | x   | Idle                   |
|                             | 1   | 1    | x   | Idle                   |
|                             | 1   | 0    | 0   | Data_0                 |
|                             | 1   | 0    | 1   | Data_1                 |

Table 5. RECEIVER FUNCTION AND RECEIVER-RELATED PINS

| Operating Mode              | Signal on Bus | Wake flag | RxD  | RxEN |
|-----------------------------|---------------|-----------|------|------|
| Standby, Go-to-sleep, Sleep | x             | not set   | High | High |
|                             | x             | set       | Low  | Low  |
| Normal, Receive-only        | Idle          | x         | High | High |
|                             | Data_0        | x         | Low  | Low  |
|                             | Data_1        | x         | High | Low  |

### Bus Guardian Interface

The interface consists of the BGE digital input signal allowing a Bus Guardian unit to disable the transmitter and of the RxEN digital output signal used to signal whether the communication signal is Idle or not.

### Bus Driver Voltage Regulator Control

NCV7381 provides a high-voltage output pin INH which can be used to control an external voltage regulator (see Figure 2). The pin INH is driven by a switch to  $V_{BAT}$  supply. In Normal, Receive-only, Standby and Go-to-Sleep modes, the switch is activated thus forcing a High level on pin INH. In the Sleep mode, the switch is open and INH pin remains floating. If a regulator is directly controlled by INH, it is then active in all operating modes with the exception of the Sleep mode.

### Bus Driver Remote Wakeup Detection

During a low-power mode and under the presence of  $V_{BAT}$  voltage, a low-power receiver constantly monitors the activity on bus pins BP and BM. A valid remote wake-up is detected when either a wakeup pattern or a dedicated wakeup frame is received. A valid remote wake-up is also detected when wakeup pattern has been started in normal-power mode already.

A wakeup pattern is composed of two Data\_0 symbols separated by Data\_1 or Idle symbols. The basic wakeup pattern composed of Data\_0 and Idle symbols is shown in Figure 6; the wakeup pattern composed of Data\_0 and Data\_1 symbols – referred to as “alternative wakeup pattern” – is depicted in Figure 7.

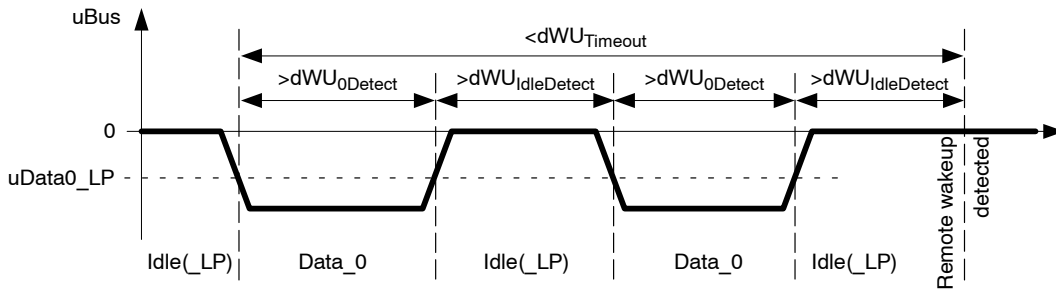


Figure 6. Valid Remote Wakeup Pattern

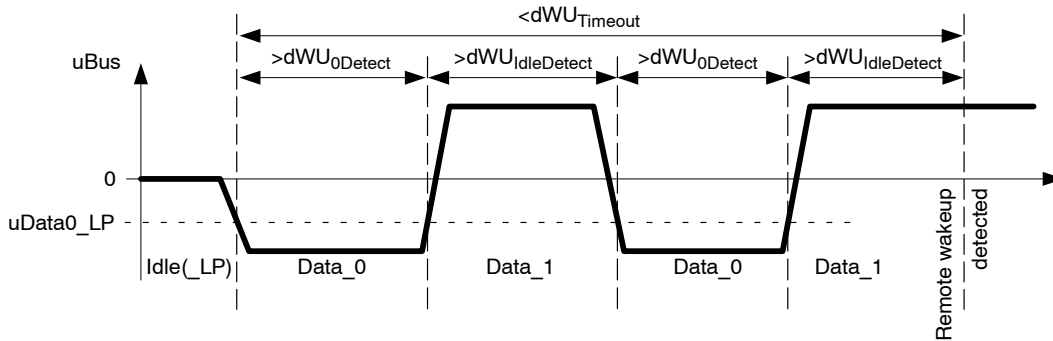


Figure 7. Valid Alternative Remote Wakeup Pattern

A remote wakeup will be also detected if NCV7381 receives a full FlexRay frame at 10 Mbit/s with the following payload data:

0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,  
0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,  
0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,  
0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF

The wakeup pattern, the alternative wakeup pattern and the wakeup frame lead to identical wakeup treatment and signaling.

### Local Wakeup Detection

The high-voltage input WAKE is monitored in low-power modes and under the condition of sufficient  $V_{BAT}$  supply level. If a falling edge is recognized on WAKE pin, a local wakeup is detected. In order to avoid false wakeups, the Low level after the falling edge must be longer than  $dWakePulseFilter$  in order for the wakeup to be valid. The WAKE pin can be used, for example, for switch or contact monitoring.

Internal pull-up and pull-down current sources are connected to WAKE pin in order to minimize the risk of parasitic toggling. The current source polarity is automatically selected based on the WAKE input signal polarity – when the voltage on WAKE stays stable High (Low) for longer than  $dWakePulseFilter$ , the internal current source is switched to pull-up (pull-down).

### ERRN Pin and Status Register

Provided  $V_{IO}$  supply is present together with either  $V_{BAT}$  or  $V_{CC}$ , the digital output ERRN indicates the state of the internal “Error” flag when in Normal mode and the state of the internal “Wake” flag when in Standby, Go-to-Sleep or Sleep. In Receive-only mode ERRN indicates either the

state of the internal “Error” or the wakeup source (See Table 6).

The polarity of the indication is reversed – ERRN pin is pulled Low when the “Error” flag is set. The signaling on pin ERRN functions in all operating modes.

**Table 6. SIGNALING ON ERRN PIN**

| STBN | EN   | Conditions                                        | Error flag | Wake flag  | ERRN |
|------|------|---------------------------------------------------|------------|------------|------|
| High | High | –                                                 | not set    | x          | High |
|      |      |                                                   | set        | x          | Low  |
| High | Low  | EN has been set to High after previous wakeup     | not set    | x          | High |
|      |      |                                                   | set        | x          | Low  |
|      |      | EN has not been set to High after previous wakeup | x          | Set local  | High |
|      |      |                                                   | x          | Set remote | Low  |
| Low  | x    | –                                                 | x          | not set    | High |
|      |      |                                                   | x          | set        | Low  |

Additionally, a full set of internal bits referred to as status register can be read through ERRN pin with EN pin used as a clock signal – the status register content is described in Table 7 while an example of the read-out waveforms is shown in Figure 8 and Figure 9. The individual status bits are channeled to ERRN pin with reversed polarity (if a status bit is set, ERRN is pulled Low) at the falling edge on EN pin (the status register starts to be shifted only at the second falling edge). As long as the EN pin toggling period falls in the  $dEN_{STAT}$  range, the operating mode is not changed and the

read-out continues. As soon as the EN level is stable for more than  $dBDModeChange$ , the read-out is considered as finished and the operating mode is changed according the current EN value. At the same time, the status register bits S4 to S10 are reset provided the particular bits have been read-out and the corresponding flags are not set any more – see Table 7. The status register read-out always starts with bit S0 and the exact number of bits shifted to ERRN during the read-out is not relevant.

**Table 7. STATUS REGISTER**

| Bit Number | Status Bit Content                  | Note                                                                                                                                             | Reset after Finished Read-out                                    |
|------------|-------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------|
| S0         | Local wakeup flag                   | reflects directly the corresponding flag                                                                                                         | no                                                               |
| S1         | Remote wakeup flag                  |                                                                                                                                                  |                                                                  |
| S2         | not used; always High               |                                                                                                                                                  |                                                                  |
| S3         | Power-on status                     | the status bit is set if the corresponding flag was set previously (the respective High level of the flag is latched in its status counter-part) | yes, if the corresponding flag is reset and the bit was read-out |
| S4         | Bus error status                    |                                                                                                                                                  |                                                                  |
| S5         | Thermal shutdown status             |                                                                                                                                                  |                                                                  |
| S6         | Thermal warning status              |                                                                                                                                                  |                                                                  |
| S7         | TxEN Timeout status                 |                                                                                                                                                  |                                                                  |
| S8         | $V_{BAT}$ Under-voltage status      |                                                                                                                                                  |                                                                  |
| S9         | $V_{CC}$ Under-voltage status       |                                                                                                                                                  |                                                                  |
| S10        | $V_{IO}$ Under-voltage status       |                                                                                                                                                  |                                                                  |
| S11        | BGE Feedback                        | Normal mode: BGE pin logical state (Note 3)<br>Other modes: Low                                                                                  | –                                                                |
| S12–S15    | not used; always Low                |                                                                                                                                                  | no                                                               |
| S16–S23    | Version of the NCV7381 analog part  | fixed values identifying the production masks version                                                                                            | no                                                               |
| S24–S31    | Version of the NCV7381 digital part |                                                                                                                                                  |                                                                  |

3. The BGE pin state is latched during status register read-out at rising edge of the EN pin.

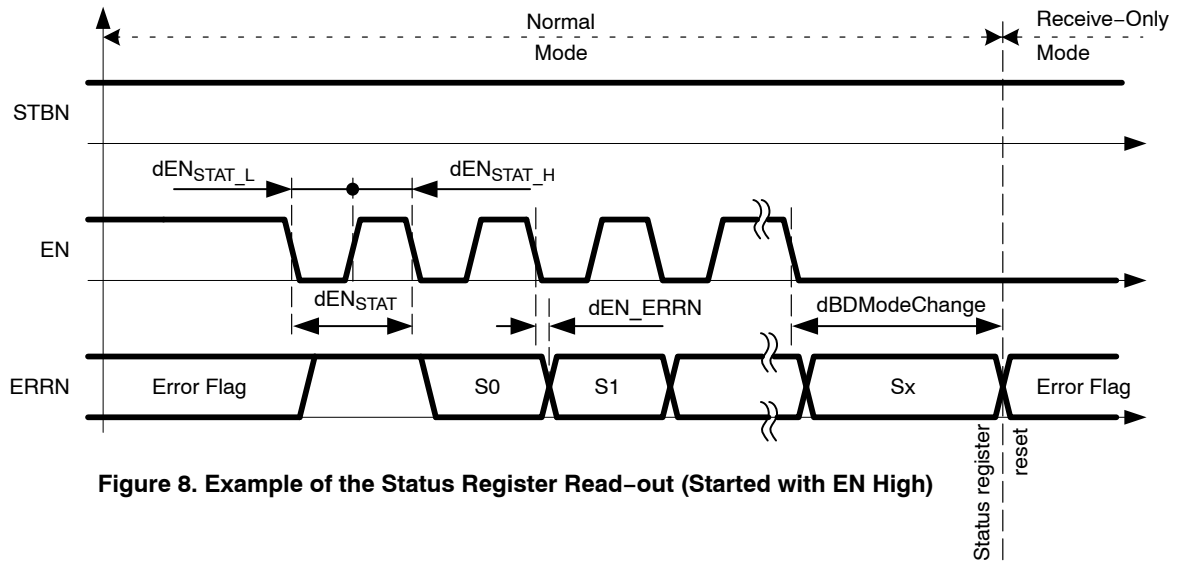


Figure 8. Example of the Status Register Read-out (Started with EN High)

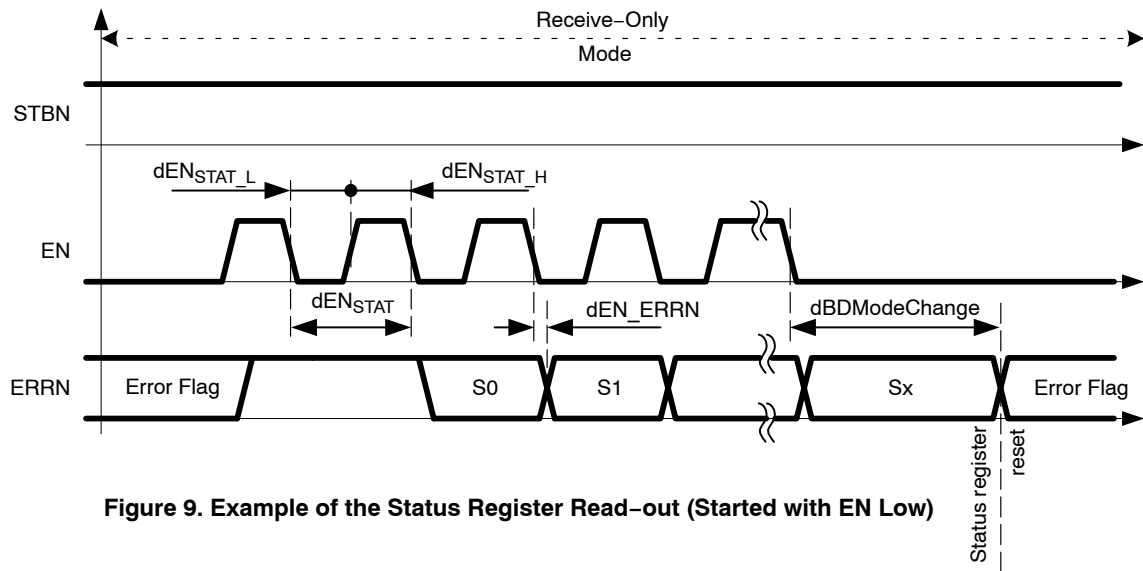


Figure 9. Example of the Status Register Read-out (Started with EN Low)

**Table 8. ABSOLUTE MAXIMUM RATINGS**

| Symbol                     | Parameter                                                                                           |                                                | Min        | Max                   | Units |
|----------------------------|-----------------------------------------------------------------------------------------------------|------------------------------------------------|------------|-----------------------|-------|
| uV <sub>BAT-MAX</sub>      | Battery voltage power supply                                                                        |                                                | −0.3       | 50                    | V     |
| uV <sub>CC-MAX</sub>       | 5 V Supply voltage                                                                                  |                                                | −0.3       | 5.5                   | V     |
| uV <sub>IO-MAX</sub>       | Supply voltage for V <sub>IO</sub> voltage level adaptation                                         |                                                | −0.3       | 5.5                   | V     |
| uDigiIn <sub>MAX</sub>     | DC voltage at digital inputs (BGE, EN, STBN, TXD, TXEN)                                             |                                                | −0.3       | 5.5                   | V     |
| uDigiOut <sub>MAX</sub>    | DC voltage at digital outputs (ERRN, RxD, RxEN)                                                     |                                                | −0.3       | V <sub>IO</sub> +0.3  | V     |
| iDigiOut <sub>IN-MAX</sub> | Digital output pins input current (V <sub>IO</sub> = 0 V)                                           |                                                | −10        | +10                   | mA    |
| uBM <sub>MAX</sub>         | DC voltage at pin BM                                                                                |                                                | −50        | 50                    | V     |
| uBP <sub>MAX</sub>         | DC voltage at pin BP                                                                                |                                                | −50        | 50                    | V     |
| uINH <sub>MAX</sub>        | DC voltage at pin INH                                                                               |                                                | −0.3       | V <sub>BAT</sub> +0.3 | V     |
| iINH <sub>MAX</sub>        | INH pin maximum load current                                                                        |                                                | −10        | −                     | mA    |
| uWAKE <sub>MAX</sub>       | DC voltage at WAKE pin                                                                              |                                                | −0.3       | V <sub>BAT</sub> +0.3 | V     |
| T <sub>J_MAX</sub>         | Junction temperature                                                                                |                                                | −40        | 175                   | °C    |
| T <sub>STG</sub>           | Storage Temperature Range                                                                           |                                                | −55        | 150                   | °C    |
| MSL                        | Moisture Sensitivity Level                                                                          |                                                | 2          |                       | −     |
| uESD <sub>IEC</sub>        | System HBM on pins BP and BM (as per IEC 61000−4−2; 150 pF / 330 Ω)                                 |                                                | −10        | +10                   | kV    |
| uESD <sub>EXT</sub>        | Component HBM on pins BP, BM, V <sub>BAT</sub> and WAKE (as per EIA−JESD22−A114−B; 100 pF / 1500 Ω) |                                                | −6         | +6                    | kV    |
| uESD <sub>INT</sub>        | Component HBM on all other pins (as per EIA−JESD22−A114−B; 100 pF / 1500 Ω)                         |                                                | −4         | +4                    | kV    |
| uV <sub>TRAN</sub>         | Voltage transients, pins BP, BM, VBAT and WAKE. According to ISO7637−2, Class C (Note 4)            | test pulses 1                                  | −100       | −                     | V     |
|                            |                                                                                                     | test pulses 2a                                 | −          | +75                   | V     |
|                            |                                                                                                     | test pulses 3a                                 | −150       | −                     | V     |
|                            |                                                                                                     | test pulses 3b                                 | −          | +100                  | V     |
|                            | Voltage transients, pin VBAT. According to ISO7637−2                                                | test pulse 5 Load Dump                         | −          | 50                    | V     |
|                            |                                                                                                     | Overvoltage, pin VBAT, according to ISO16750−2 | Jump Start | −                     | 50    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. Test is carried out according to setup in *FlexRay Physical Layer EMC Measurement Specification, Version 3.0*. This specification is referring to ISO7637. Test for higher voltages is planned.

**Table 9. OPERATING RANGES**

| Symbol        | Parameter                                                             | Min  | Max       | Units |
|---------------|-----------------------------------------------------------------------|------|-----------|-------|
| $uV_{BAT-OP}$ | Battery voltage power supply (Note 5)                                 | 5.5  | 50        | V     |
| $uV_{CC-OP}$  | Supply voltage 5 V                                                    | 4.75 | 5.25      | V     |
| $uV_{IO-OP}$  | Supply voltage for $V_{IO}$ voltage level adaptation                  | 2.3  | 5.25      | V     |
| $uWAKE_{OP}$  | DC voltage at WAKE pin                                                | 0    | $V_{BAT}$ | V     |
| $uDigIO_{OP}$ | DC voltage at digital pins (EN, TXD, TXEN, RxD, RxE, BGE, STBN, ERRN) | 0    | $V_{IO}$  | V     |
| $uBM_{OP}$    | DC voltage at pin BM                                                  | -50  | 50        | V     |
| $uBP_{OP}$    | DC voltage at pin BP                                                  | -50  | 50        | V     |
| $uINH_{OP}$   | DC voltage at pin INH                                                 | 0    | $V_{BAT}$ | V     |
| $T_{AMB}$     | Ambient temperature (Note 6)                                          | -40  | 125       | °C    |
| $T_{J\_OP}$   | Junction temperature                                                  | -40  | 150       | °C    |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Full functionality is guaranteed from 5.1 V. See also parameter  $uBDUVV_{BAT}$ .

6. The specified range corresponds to  $T_{AMB\_Class1}$

## THERMAL CHARACTERISTICS

**Table 10. PACKAGE THERMAL RESISTANCE**

| Symbol             | Rating                                             | Value | Unit |
|--------------------|----------------------------------------------------|-------|------|
| $R_{\theta JA\_1}$ | Thermal Resistance Junction-to-Air, JEDEC 1S0P PCB | 78    | °C/W |
| $R_{\theta JA\_2}$ | Thermal Resistance Junction-to-Air, JEDEC 2S2P PCB | 69    | °C/W |

## ELECTRICAL CHARACTERISTICS

The characteristics defined in this section are guaranteed within the operating ranges listed in Table 9, unless otherwise specified. Positive currents flow into the respective pin.

**Table 11. CURRENT CONSUMPTION**

| Symbol                       | Parameter                                               | Conditions                                                                                                           | Min | Typ  | Max  | Unit |
|------------------------------|---------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|-----|------|------|------|
| iV <sub>BAT-NORM</sub>       | Current consumption from V <sub>BAT</sub>               | normal-power modes                                                                                                   |     | 0.65 | 1.25 | mA   |
| iV <sub>BAT-LP</sub>         |                                                         | low-power modes; T <sub>AMB</sub> =125°C                                                                             |     |      | 75   | μA   |
|                              |                                                         | Sleep mode, V <sub>IO</sub> = V <sub>CC</sub> = 0 V;<br>T <sub>AMB</sub> = 125°C                                     |     |      | 80   | μA   |
|                              |                                                         | low-power modes, V <sub>IO</sub> = V <sub>CC</sub> = 0 V,<br>V <sub>BAT</sub> = 12 V, T <sub>J</sub> < 85°C (Note 7) |     |      | 55   | μA   |
| iV <sub>CC-NORM-IDLE</sub>   | Current consumption from V <sub>CC</sub>                | Normal mode – bus signals Idle                                                                                       |     |      | 15   | mA   |
| iV <sub>CC-NORM-ACTIVE</sub> |                                                         | Normal mode – bus signals Data_0/1<br>R <sub>BUS</sub> = 40–55 Ω                                                     |     |      | 37   | mA   |
| iV <sub>CC-REC</sub>         |                                                         | Receive-only mode                                                                                                    |     |      | 15   | mA   |
| iV <sub>CC-LP</sub>          |                                                         | low-power modes, T <sub>J</sub> < 85°C (Note 7)                                                                      |     |      | 8    | μA   |
| iV <sub>IO-NORM</sub>        | Current consumption from V <sub>IO</sub>                | normal-power modes                                                                                                   |     |      | 1    | mA   |
| iV <sub>IO-LP</sub>          |                                                         | low-power modes, T <sub>J</sub> < 85°C (Note 7)                                                                      |     |      | 6    | μA   |
| iT <sub>ot-LP</sub>          | Total current consumption –<br>Sum from all supply pins | low-power modes; T <sub>AMB</sub> = 125°C                                                                            |     |      | 95   | μA   |
|                              |                                                         | Sleep mode, V <sub>IO</sub> = V <sub>CC</sub> = 5 V,<br>V <sub>BAT</sub> = 12 V, T <sub>J</sub> < 85°C (Note 7)      |     |      | 65   | μA   |
|                              |                                                         | Sleep mode, V <sub>IO</sub> = V <sub>CC</sub> = 5 V,<br>V <sub>BAT</sub> = 12 V, T <sub>J</sub> < 25°C (Note 7)      |     |      | 55   | μA   |

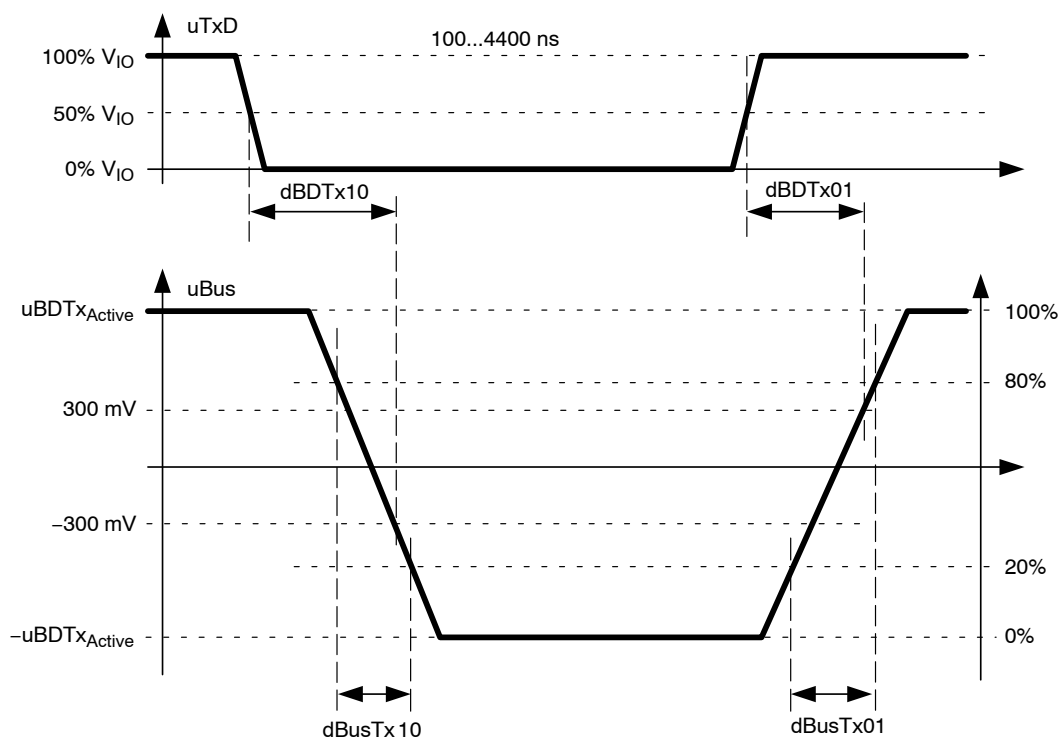
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Values based on design and characterization, not tested in production

Table 12. TRANSMISSION PARAMETERS

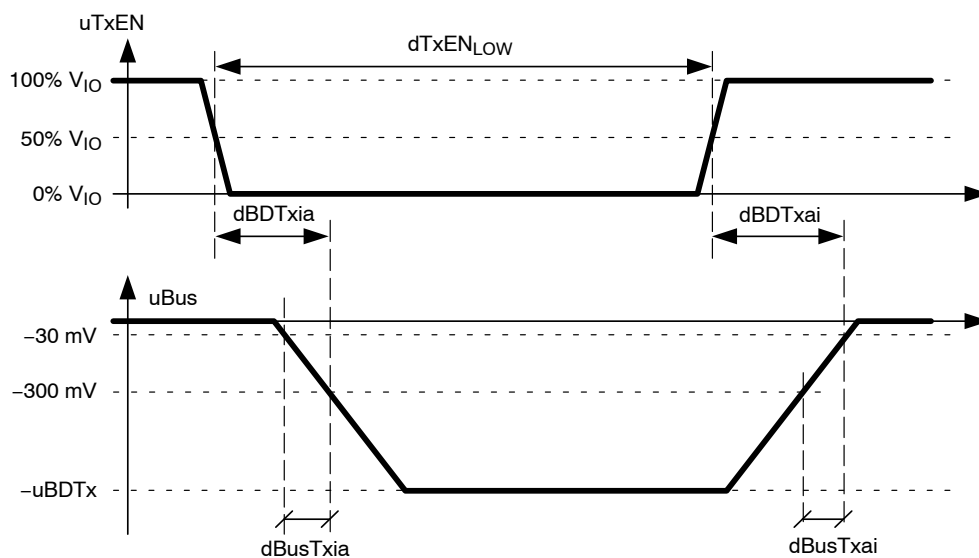
| Symbol                                         | Parameter                                                                                | Conditions                                                                                                                                                          | Min | Typ | Max   | Unit     |
|------------------------------------------------|------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-------|----------|
| $uBDT_{xactive}$                               | Differential voltage $ uBP-uBM $ when sending symbol "Data_0" or "Data_1"                | $R_{BUS} = 40-55 \Omega$ ;<br>$C_{BUS} = 100 \text{ pF}$<br>Parameters defined in Figure 10.                                                                        | 600 |     | 2000  | mV       |
| $uBDT_{xidle}$                                 | Differential voltage $ uBP-uBM $ when driving signal "Idle"                              |                                                                                                                                                                     | 0   |     | 30    | mV       |
| $dBdT_{x10}$                                   | Transmitter delay, negative edge                                                         | Test setup as per Figure 17 with<br>$R_{BUS} = 40 \Omega$ ;<br>$C_{BUS} = 100 \text{ pF}$<br>Sum of TXD signal rise and fall time (20%–80% $V_{IO}$ ) of up to 9 ns |     |     | 75    | ns       |
| $dBdT_{x01}$                                   | Transmitter delay, positive edge                                                         |                                                                                                                                                                     |     |     | 75    | ns       |
| $dBdT_{xAsym}$                                 | Transmitter delay mismatch, $ dBdT_{x10}-dBdT_{x01} $ (Note 8)                           |                                                                                                                                                                     |     |     | 4     | ns       |
| $dBusTx10$                                     | Fall time of the differential bus voltage from 80% to 20%                                |                                                                                                                                                                     | 6   |     | 18.75 | ns       |
| $dBusTx01$                                     | Rise time of the differential bus voltage from 20% to 80%                                |                                                                                                                                                                     | 6   |     | 18.75 | ns       |
| $dBusTxDif$                                    | Differential bus voltage fall and rise time mismatch $ dBusTx10-dBusTx01 $               |                                                                                                                                                                     |     |     | 3     | ns       |
| $dBdT_{xia}$                                   | Transmitter delay idle → active                                                          | Test setup as per Figure 17 with<br>$R_{BUS} = 40 \Omega$ ;<br>$C_{BUS} = 100 \text{ pF}$<br>Parameters defined in Figure 11.                                       |     |     | 75    | ns       |
| $dBdT_{xai}$                                   | Transmitter delay active → idle                                                          |                                                                                                                                                                     |     |     | 75    | ns       |
| $dBdT_{xDM}$                                   | Idle–active transmitter delay mismatch $ dBdT_{xia} - dBdT_{xai} $                       |                                                                                                                                                                     |     |     | 50    | ns       |
| $dBusTxia$                                     | Transition time idle → active                                                            |                                                                                                                                                                     |     |     | 30    | ns       |
| $dBusTxai$                                     | Transition time active → idle                                                            |                                                                                                                                                                     |     |     | 30    | ns       |
| $dTxEN_{LOW}$                                  | Time span of bus activity                                                                |                                                                                                                                                                     | 550 |     | 650   | ns       |
| $dBdT_{xActiveMax}$                            | Maximum length of transmitter activation                                                 |                                                                                                                                                                     | 650 |     | 2600  | $\mu s$  |
| $iBP_{BMSHORTMax}$<br>$iBM_{BPSHORTMax}$       | Absolute maximum output current when BP shorted to BM – no time limit                    | $R_{ShortCircuit} \leq 1 \Omega$                                                                                                                                    |     |     | 60    | mA       |
| $iBP_{GNDSHORTMax}$<br>$iBM_{GNDSHORTMax}$     | Absolute maximum output current when shorted to GND – no time limit                      | $R_{ShortCircuit} \leq 1 \Omega$                                                                                                                                    |     |     | 60    | mA       |
| $iBP_{-5VSHORTMax}$<br>$iBM_{-5VSHORTMax}$     | Absolute maximum output current when shorted to $V_{BAT} = -5 \text{ V}$ – no time limit | $R_{ShortCircuit} \leq 1 \Omega$                                                                                                                                    |     |     | 60    | mA       |
| $iBP_{BAT27SHORTMax}$<br>$iBM_{BAT27SHORTMax}$ | Absolute maximum output current when shorted to $V_{BAT} = 27 \text{ V}$ – no time limit | $R_{ShortCircuit} \leq 1 \Omega$                                                                                                                                    |     |     | 60    | mA       |
| $iBP_{BAT48SHORTMax}$<br>$iBM_{BAT48SHORTMax}$ | Absolute maximum output current when shorted to $V_{BAT} = 48 \text{ V}$ – no time limit | $R_{ShortCircuit} \leq 1 \Omega$                                                                                                                                    |     |     | 72    | mA       |
| $R_{BDTransmitter}$                            | Bus interface equivalent output impedance (Bus driver simulation model parameter)        |                                                                                                                                                                     | 31  | 105 | 500   | $\Omega$ |

8. Guaranteed for  $\pm 300 \text{ mV}$  and  $\pm 150 \text{ mV}$  level of uBus



**Figure 10. Transmission Parameters (TxEN is Low and BGE is High)**

NOTE: TXD signal is constant for 100..4400 ns before the first edge.  
All parameters values are valid even if the test is performed with opposite polarity.



**Figure 11. Transmission Parameters for Transitions between Idle and Active (TXD is Low)**

Table 13. RECEPTION PARAMETERS

| Symbol                             | Parameter                                                                                                                  | Conditions                                                                                                | Min  | Typ  | Max  | Unit          |
|------------------------------------|----------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| uData0                             | Receiver threshold for detecting Data_0                                                                                    | Activity detected previously.<br>$ uBP - uBM  \leq 3 \text{ V}$                                           | -300 |      | -150 | mV            |
| uData1                             | Receiver threshold for detecting Data_1                                                                                    |                                                                                                           | 150  |      | 300  | mV            |
| $ uData1  -  uData0 $              | Mismatch of receiver thresholds                                                                                            | $(uBP + uBM)/2 = 2.5 \text{ V}$                                                                           | -30  |      | 30   | mV            |
| uData0_LP                          | Low power receiver threshold for detecting Data_0                                                                          | $uV_{BAT} \geq 7 \text{ V}$                                                                               | -400 |      | -100 | mV            |
| uCM                                | Common mode voltage range (with respect to GND) that does not disturb the receiver function and reception level parameters | $uBP = (uBP + uBM)/2$<br>(Note 9)                                                                         | -10  |      | 15   | V             |
| uBias                              | Bus bias voltage during bus state Idle in normal-power modes                                                               | $R_{BUS} = 40\text{--}55 \text{ }\Omega$ ;<br>$C_{BUS} = 100 \text{ pF}$<br>(Note 10)                     | 1800 | 2500 | 3200 | mV            |
|                                    | Bus bias voltage during bus state Idle in low-power modes                                                                  |                                                                                                           | -200 | 0    | 200  | mV            |
| $R_{CM1}, R_{CM2}$                 | Receiver common mode resistance                                                                                            | (Note 10)                                                                                                 | 10   |      | 40   | k $\Omega$    |
| $C_{BP}, C_{BM}$                   | Input capacitance on BP and BM pin (Note 11)                                                                               | $f = 5 \text{ MHz}$                                                                                       |      |      | 20   | pF            |
| $C_{BUSDIFF}$                      | Bus differential input capacitance (Note 11)                                                                               | $f = 5 \text{ MHz}$                                                                                       |      |      | 5    | pF            |
| $iBP_{LEAK}$<br>$iBM_{LEAK}$       | Absolute leakage current when driver is off                                                                                | $uBP = uBM = 5 \text{ V}$<br>All other pins = 0 V                                                         |      |      | 25   | $\mu\text{A}$ |
| $iBP_{LEAKGND}$<br>$iBM_{LEAKGND}$ | Absolute leakage current, in case of loss of GND                                                                           | $uBP = uBM = 0 \text{ V}$<br>All other pins = 16 V                                                        |      |      | 1600 | $\mu\text{A}$ |
| uBusRxData                         | Test signal parameters for reception of Data_0 and Data_1 symbols                                                          | Test signal and parameters defined in Figure 12 and Figure 13.<br><br>Rx pin loaded with 25 pF capacitor. | 400  |      | 3000 | mV            |
| dBusRx0BD                          |                                                                                                                            |                                                                                                           | 60   |      | 4330 | ns            |
| dBusRx1BD                          |                                                                                                                            |                                                                                                           | 60   |      | 4330 | ns            |
| dBusRx10                           |                                                                                                                            |                                                                                                           |      |      | 22.5 | ns            |
| dBusRx01                           |                                                                                                                            |                                                                                                           |      |      | 22.5 | ns            |
| dBDRx10                            | Receiver delay, negative edge (Note 12)                                                                                    |                                                                                                           |      |      | 75   | ns            |
| dBDRx01                            | Receiver delay, positive edge (Note 12)                                                                                    |                                                                                                           |      |      | 75   | ns            |
| dBDRxAsym                          | Receiver delay mismatch<br>$ dBDRx10 - dBDRx01 $ (Note 12)                                                                 |                                                                                                           |      |      | 5    | ns            |
| uBusRx                             | Test signal parameters for bus activity detection                                                                          |                                                                                                           | 400  |      | 3000 | mV            |
| dBusActive                         |                                                                                                                            |                                                                                                           | 590  |      | 610  | ns            |
| dBusIdle                           |                                                                                                                            |                                                                                                           | 590  |      | 610  | ns            |
| dBusRxia                           |                                                                                                                            |                                                                                                           | 18   |      | 22   | ns            |
| dBusRxai                           |                                                                                                                            |                                                                                                           | 18   |      | 22   | ns            |
| dBdIdleDetection                   | Bus driver filter-time for idle detection                                                                                  |                                                                                                           | 50   |      | 200  | ns            |
| dBdActivityDetection               | Bus driver filter-time for activity detection                                                                              |                                                                                                           | 100  |      | 250  | ns            |
| dBDRxai                            | Bus driver idle reaction time                                                                                              |                                                                                                           | 50   |      | 275  | ns            |
| dBDRxia                            | Bus driver activity reaction time                                                                                          |                                                                                                           | 100  |      | 325  | ns            |
| dBdTxRxai                          | Idle-Loopdelay                                                                                                             |                                                                                                           |      |      | 325  | ns            |

9. Tested on a receiving bus driver. Sending bus driver has a ground offset voltage in the range of  $[-12.5 \text{ V to } +12.5 \text{ V}]$  and sends a 50/50 pattern.

10. Bus driver is connected to GND and  $uV_{CC} = 5 \text{ V}$  and  $uV_{BAT} \geq 7 \text{ V}$ .

11. Values based on design and characterization, not tested in production.

12. Guaranteed for  $\pm 300 \text{ mV}$  and  $\pm 150 \text{ mV}$  level of uBus.

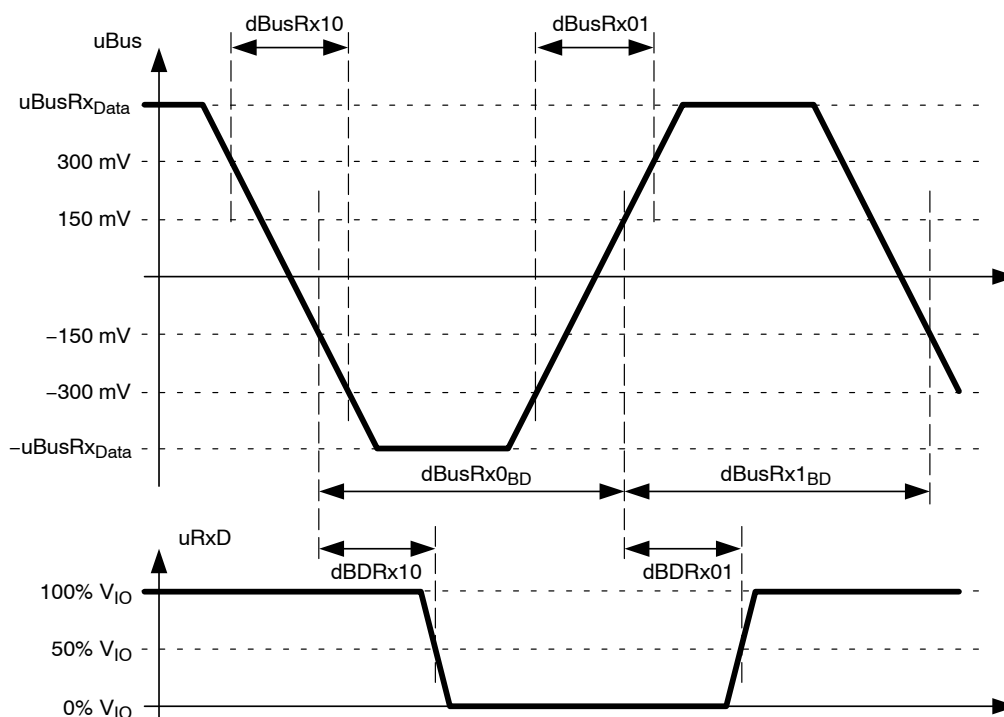
**Table 14. REMOTE WAKEUP DETECTION PARAMETERS**

| Symbol                             | Parameter                                                           | Conditions | Min  | Typ | Max | Unit    |
|------------------------------------|---------------------------------------------------------------------|------------|------|-----|-----|---------|
| $dWU_{0Detect}$                    | Detection time for Wakeup Data_0 symbol                             |            | 1    |     | 4   | $\mu s$ |
| $dWU_{IdleDetect}$                 | Detection time for Wakeup Idle/Data_1 symbol                        |            | 1    |     | 4   | $\mu s$ |
| $dWU_{Timeout}$                    | Maximum accepted Wakeup pattern duration                            |            | 48   |     | 140 | $\mu s$ |
| $dWU_{Interrupt}$                  | Acceptance timeout for interruptions                                | (Note 13)  | 0.13 |     | 1   | $\mu s$ |
| $uV_{BAT-WAKE}$                    | Minimum supply voltage $V_{BAT}$ for remote wakeup events detection |            | –    |     | 5.5 | V       |
| $dBDWakeup$<br>$Reaction_{remote}$ | Reaction time after remote wakeup event                             |            | 7    |     | 35  | $\mu s$ |

13. The minimum value is only guaranteed, when the phase that is interrupted was continuously present for at least 870 ns.

**Table 15. TEMPERATURE MONITORING PARAMETERS**

| Symbol     | Parameter               | Conditions | Min | Typ | Max | Unit        |
|------------|-------------------------|------------|-----|-----|-----|-------------|
| $T_{jw}$   | Thermal warning level   |            | 125 | 140 | 150 | $^{\circ}C$ |
| $T_{jshd}$ | Thermal shut-down level |            | 155 | 165 | 185 | $^{\circ}C$ |



**Figure 12. Reception Parameters**

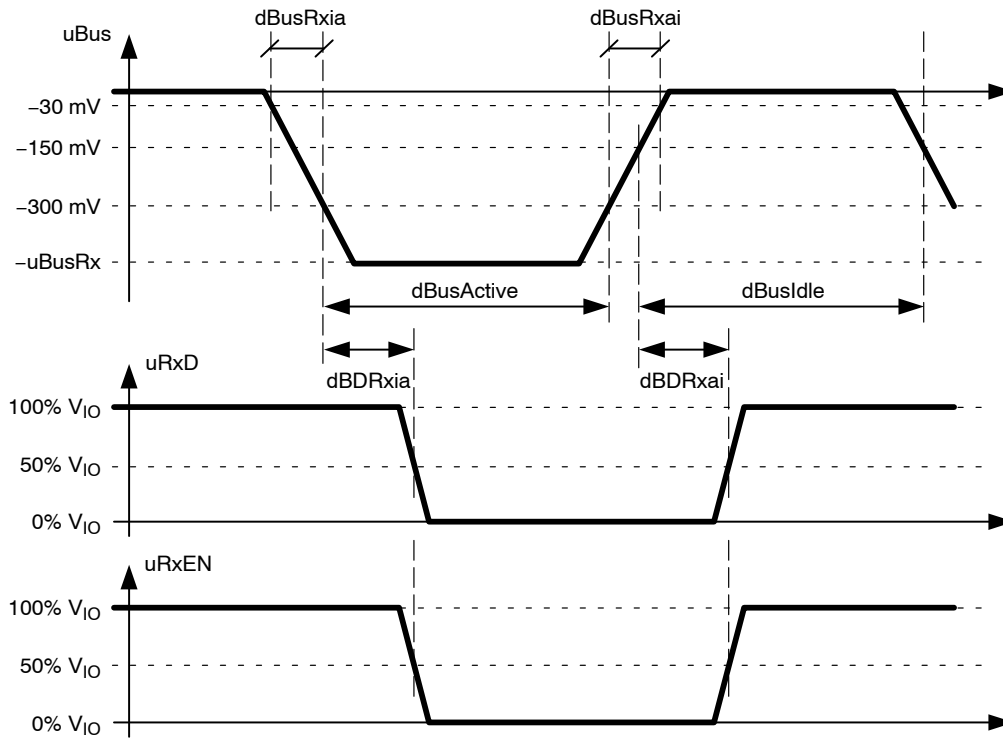


Figure 13. Parameters of Bus Activity Detection

Table 16. WAKE PIN PARAMETERS

| Symbol                      | Parameter                                                          | Conditions                                           | Min | Typ         | Max | Unit    |
|-----------------------------|--------------------------------------------------------------------|------------------------------------------------------|-----|-------------|-----|---------|
| $uV_{BAT-WAKE}$             | Minimum supply voltage $V_{BAT}$ for local wakeup events detection |                                                      |     |             | 7   | V       |
| $uWAKE_{TH}$                | Threshold of wake comparator                                       |                                                      |     | $V_{BAT}/2$ |     | V       |
| $dBDWakePulseFilter$        | Wake pulse filter time (spike rejection)                           |                                                      | 1   |             | 500 | $\mu s$ |
| $dBDWakeupReaction_{local}$ | Reaction time after local wakeup event                             |                                                      | 14  |             | 50  | $\mu s$ |
| $iWAKE_{PD}$                | Internal pull-down current                                         | $uWAKE = 0 V$ for longer than $dWakePulseFilter$     | 3   |             | 11  | $\mu A$ |
| $iWAKE_{PU}$                | Internal pull-up current                                           | $uWAKE = V_{BAT}$ for longer than $dWakePulseFilter$ | -11 |             | -3  | $\mu A$ |

Table 17. INH PIN PARAMETERS

| Symbol               | Parameter                                    | Conditions                           | Min              | Typ               | Max              | Unit    |
|----------------------|----------------------------------------------|--------------------------------------|------------------|-------------------|------------------|---------|
| $uINH1_{Not\_Sleep}$ | Voltage on INH pin, when signaling Not_Sleep | $iINH = -5 mA$<br>$uV_{BAT} > 5.5 V$ | $uV_{BAT} - 0.6$ | $uV_{BAT} - 0.27$ | $uV_{BAT} - 0.1$ | V       |
| $iINH1_{LEAK}$       | Leakage current while signaling Sleep        |                                      | -5               |                   | 5                | $\mu A$ |

Table 18. POWER SUPPLY MONITORING PARAMETERS

| Symbol              | Parameter                                                                   | Conditions | Min | Typ | Max | Unit |
|---------------------|-----------------------------------------------------------------------------|------------|-----|-----|-----|------|
| $uBDUVV_{BAT}$      | $V_{BAT}$ under-voltage threshold                                           |            | 4   |     | 5.1 | V    |
| $uBDUVV_{CC}$       | $V_{CC}$ under-voltage threshold                                            |            | 4   |     | 4.5 | V    |
| $uUV_{IO}$          | $V_{IO}$ under-voltage threshold                                            |            | 2   |     | 2.3 | V    |
| $uBDUVV_{BAT-WAKE}$ | $V_{BAT}$ under-voltage threshold for correct detection of the local wakeup |            | 5   |     | 7   | V    |
| $uUV\_HYST$         | Hysteresis of the under-voltage detectors                                   |            | 20  | 100 | 200 | mV   |

**Table 18. POWER SUPPLY MONITORING PARAMETERS**

| Symbol                | Parameter                                    | Conditions | Min | Typ | Max  | Unit |
|-----------------------|----------------------------------------------|------------|-----|-----|------|------|
| dBDUVV <sub>CC</sub>  | V <sub>CC</sub> Undervoltage detection time  |            | 150 | 350 | 750  | ms   |
| dBDUVV <sub>IO</sub>  | V <sub>IO</sub> Undervoltage detection time  |            | 150 | 350 | 750  | ms   |
| dBDUVV <sub>BAT</sub> | V <sub>BAT</sub> Undervoltage detection time |            | 350 | 750 | 1500 | μs   |
| dBDRV <sub>CC</sub>   | V <sub>CC</sub> Undervoltage recovery time   |            | 1.5 |     | 4.5  | ms   |
| dBDRV <sub>IO</sub>   | V <sub>IO</sub> Undervoltage recovery time   |            |     |     | 1    | ms   |
| dBDRV <sub>BAT</sub>  | V <sub>BAT</sub> Undervoltage recovery time  |            |     |     | 1    | ms   |

**Table 19. HOST INTERFACE PARAMETERS**

| Symbol                        | Parameter                                                      | Conditions                      | Min | Typ | Max | Unit |
|-------------------------------|----------------------------------------------------------------|---------------------------------|-----|-----|-----|------|
| dBDModeChange                 | EN and STBN level filtering time for operating mode transition |                                 | 21  |     | 65  | μs   |
| dGo-to-Sleep                  | Go to Sleep mode timeout                                       |                                 | 14  |     | 33  | μs   |
| dReactionTime <sub>ERRN</sub> | Reaction time on ERRN pin                                      | Error detected                  |     |     | 33  | μs   |
|                               |                                                                | Wakeup detected or Mode changed |     |     | 1   | μs   |

## Digital Input Signals

**Table 20. DIGITAL INPUT SIGNALS VOLTAGE THRESHOLDS (Pins EN, STBN, BGE, TxEN)**

| Symbol                    | Parameter                | Conditions                           | Min                 | Typ | Max                 | Unit |
|---------------------------|--------------------------|--------------------------------------|---------------------|-----|---------------------|------|
| uV <sub>DIG-IN-LOW</sub>  | Low level input voltage  | uV <sub>DIG</sub> = uV <sub>IO</sub> | -0.3                |     | 0.3*V <sub>IO</sub> | V    |
| uV <sub>DIG-IN-HIGH</sub> | High level input voltage |                                      | 0.7*V <sub>IO</sub> |     | 5.5                 | V    |

**Table 21. EN PIN PARAMETERS**

| Symbol                                           | Parameter                                                                               | Conditions | Min | Typ | Max | Unit |
|--------------------------------------------------|-----------------------------------------------------------------------------------------|------------|-----|-----|-----|------|
| R <sub>PD_EN</sub>                               | Pull-down resistance                                                                    |            | 50  | 110 | 200 | kΩ   |
| iEN <sub>IL</sub>                                | Low level input current                                                                 | uEN = 0 V  | -1  | 0   | 1   | μA   |
| dEN <sub>STAT</sub>                              | EN toggling period for status register read-out                                         |            | 2   |     | 20  | μs   |
| dEN <sub>STAT_L</sub> ,<br>dEN <sub>STAT_H</sub> | Duration of EN Low and High level for status register read-out                          |            | 1   |     |     | μs   |
| dEN_ERRN                                         | Delay from EN falling edge to ERRN showing valid signal during status register read-out |            |     |     | 1   | μs   |

**Table 22. STBN PIN PARAMETERS**

| Symbol               | Parameter               | Conditions  | Min | Typ | Max | Unit |
|----------------------|-------------------------|-------------|-----|-----|-----|------|
| R <sub>PD_STBN</sub> | Pull-down resistance    |             | 50  | 110 | 200 | kΩ   |
| iSTBN <sub>IL</sub>  | Low level input current | uSTBN = 0 V | -1  | 0   | 1   | μA   |

**Table 23. BGE PIN PARAMETERS**

| Symbol              | Parameter               | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------|------------|-----|-----|-----|------|
| R <sub>PD_BGE</sub> | Pull-down resistance    |            | 200 | 320 | 450 | kΩ   |
| iBGE <sub>IL</sub>  | Low level input current | uBGE = 0 V | -1  | 0   | 1   | μA   |

**Table 24. TxD PIN PARAMETERS**

| Symbol               | Parameter                              | Conditions | Min                | Typ | Max                | Unit       |
|----------------------|----------------------------------------|------------|--------------------|-----|--------------------|------------|
| uBDLogic_0           | Low level input voltage                |            | -0.3               |     | $0.4 \cdot V_{IO}$ | V          |
| uBDLogic_1           | High level input voltage               |            | $0.6 \cdot V_{IO}$ |     | 5.5                | V          |
| R <sub>PD</sub> _TxD | Pull-down resistance                   |            | 5                  | 11  | 20                 | k $\Omega$ |
| C_BDTxD              | Input capacitance on TxD pin (Note 14) | f = 5 MHz  |                    |     | 10                 | pF         |
| iTxD <sub>LI</sub>   | Low level input current                | uTXD = 0 V | -1                 | 0   | 1                  | $\mu$ A    |

14. Values based on design and characterization, not tested in production

**Table 25. TxEN PIN PARAMETERS**

| Symbol                | Parameter                | Conditions                     | Min | Typ | Max | Unit       |
|-----------------------|--------------------------|--------------------------------|-----|-----|-----|------------|
| R <sub>PU</sub> _TxEN | Pull-up resistance       |                                | 50  | 110 | 200 | k $\Omega$ |
| iTxEN <sub>IH</sub>   | High level input current | uTXEN = $V_{IO}$               | -1  | 0   | 1   | $\mu$ A    |
| iTxEN <sub>LEAK</sub> | Input leakage current    | uTXEN = 5.25 V, $V_{IO}$ = 0 V | -1  | 0   | 1   | $\mu$ A    |

### Digital Output Signals

**Table 26. DIGITAL OUTPUT SIGNALS VOLTAGE LIMITS (Pins RXD, RxEN and ERRN)**

| Symbol         | Parameter                                                        | Conditions                                                                                              | Min                | Typ | Max                | Unit |
|----------------|------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------|--------------------|-----|--------------------|------|
| uVDIG-OUT-LOW  | Low level output voltage                                         | iRxD <sub>OL</sub> = 6 mA<br>iRxEN <sub>OL</sub> = 5 mA<br>iERRN <sub>OL</sub> = 0.7 mA<br>(Note 15)    | 0                  |     | $0.2 \cdot V_{IO}$ | V    |
| uVDIG-OUT-HIGH | High level output voltage                                        | iRxD <sub>OH</sub> = -6 mA<br>iRxEN <sub>OH</sub> = -5 mA<br>iERRN <sub>OH</sub> = -0.7 mA<br>(Note 15) | $0.8 \cdot V_{IO}$ |     | $V_{IO}$           | V    |
| uVDIG-OUT-UV   | Output voltage on a digital output when $V_{IO}$ in undervoltage | R <sub>LOAD</sub> = 100 k $\Omega$ to GND,<br>Either $V_{CC}$ or $V_{BAT}$ supplied                     |                    |     | 500                | mV   |
| uVDIG-OUT-OFF  | Output voltage on a digital output when unsupplied               | R <sub>LOAD</sub> = 100 k $\Omega$ to GND                                                               |                    |     | 500                | mV   |

15. uVDIG = uVIO. No undervoltage on VIO and either VCC or VBAT supplied.

**Table 27. RxD PIN PARAMETERS**

| Symbol                                                 | Parameter                                                                    | Conditions                                                                                                             | Min | Typ | Max  | Unit |
|--------------------------------------------------------|------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|-----|-----|------|------|
| dBDRxD <sub>R15</sub>                                  | RXD signal rise time (20%–80% $V_{IO}$ )                                     | RxD pin loaded with<br>15 pF capacitor<br>(Note 16)                                                                    |     |     | 6.5  | ns   |
| dBDRxD <sub>F15</sub>                                  | RXD signal fall time (20%–80% $V_{IO}$ )                                     |                                                                                                                        |     |     | 6.5  | ns   |
| dBDRxD <sub>R15</sub> +<br>dBDRxD <sub>F15</sub>       | Sum of rise and fall time<br>(20%–80% $V_{IO}$ )                             |                                                                                                                        |     |     | 13   | ns   |
| dBDRxD <sub>R15</sub> -<br>dBDRxD <sub>F15</sub>       | Difference of rise and fall time                                             |                                                                                                                        |     |     | 5    | ns   |
| dBDRxD <sub>R25</sub>                                  | RXD signal rise time (20%–80% $V_{IO}$ )                                     | RxD pin loaded with<br>25 pF capacitor                                                                                 |     |     | 8.5  | ns   |
| dBDRxD <sub>F25</sub>                                  | RXD signal fall time (20%–80% $V_{IO}$ )                                     |                                                                                                                        |     |     | 8.5  | ns   |
| dBDRxD <sub>R25</sub> +<br>dBDRxD <sub>F25</sub>       | Sum of rise and fall time<br>(20%–80% $V_{IO}$ )                             |                                                                                                                        |     |     | 16.5 | ns   |
| dBDRxD <sub>R25</sub> -<br>dBDRxD <sub>F25</sub>       | Difference of rise and fall time                                             |                                                                                                                        |     |     | 5    | ns   |
| dBDRxD <sub>R25_10</sub> +<br>dBDRxD <sub>F25_10</sub> | RXD signal sum of rise and fall time at<br>TP4_CC (20%–80% $V_{IO}$ )        | RxD pin loaded with 25 pF<br>capacitor plus 10 pF at the<br>end of a 50 $\Omega$ , 1 ns<br>microstripline<br>(Note 17) |     |     | 16.5 | ns   |
| dBDRxD <sub>R25_10</sub> -<br>dBDRxD <sub>F25_10</sub> | RXD signal difference of rise and fall<br>time at TP4_CC (20%–80% $V_{IO}$ ) |                                                                                                                        |     |     | 5    | ns   |

16. Values based on design and characterization, not tested in production

17. Simulation result. Simulation performed within T<sub>J</sub>\_OP range, according to *FlexRay Electrical Physical Layer Specification, Version 3.0.1*

TYPICAL CHARACTERISTICS

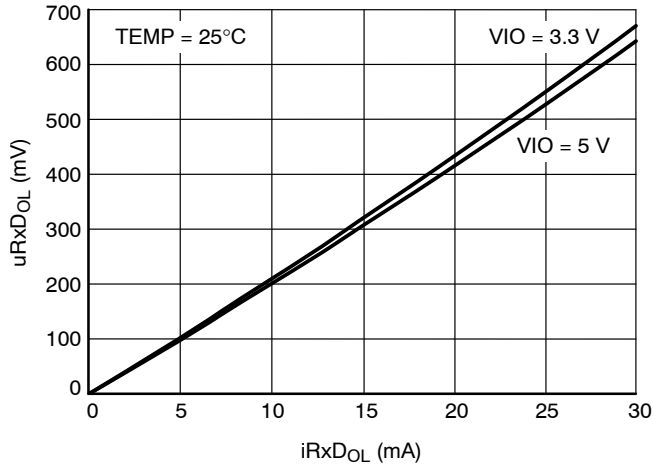


Figure 14. RxD Low Output Characteristic

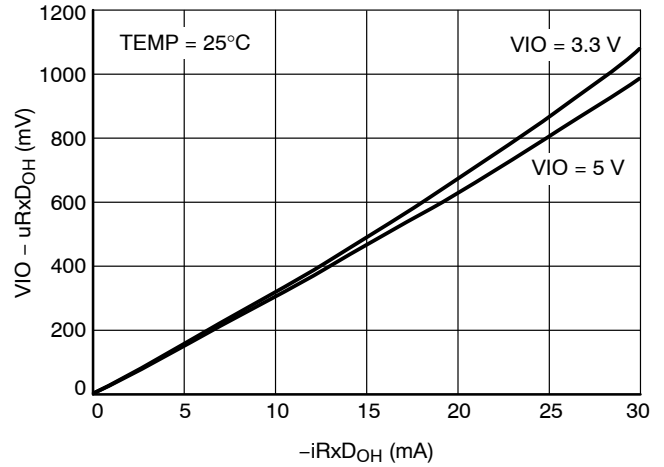


Figure 15. RxD High Output Characteristic

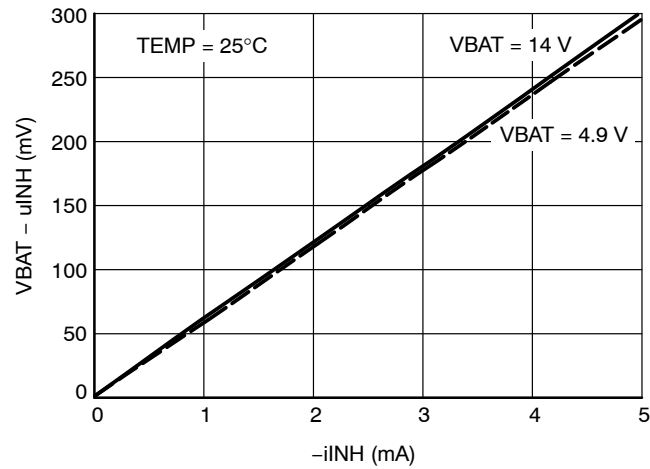


Figure 16. INH Not\_Sleep Output Characteristic

## NCV7381

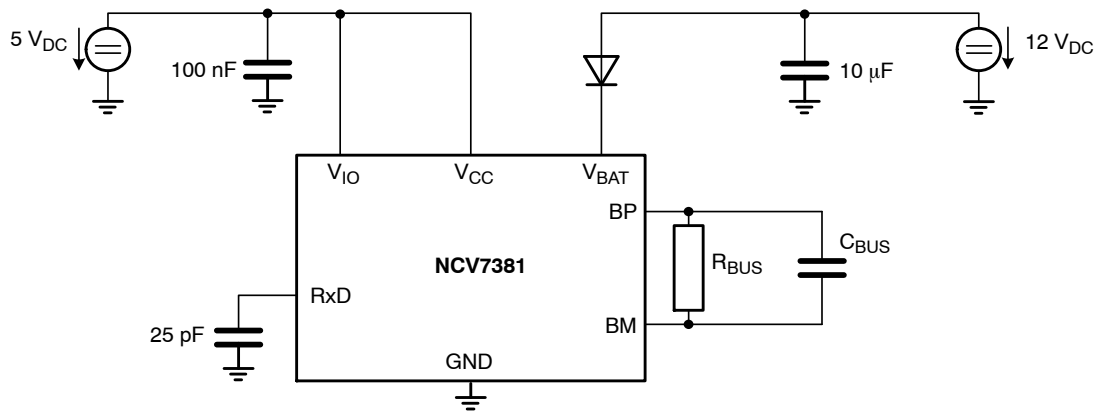


Figure 17. Test Setup for Dynamic Characteristics

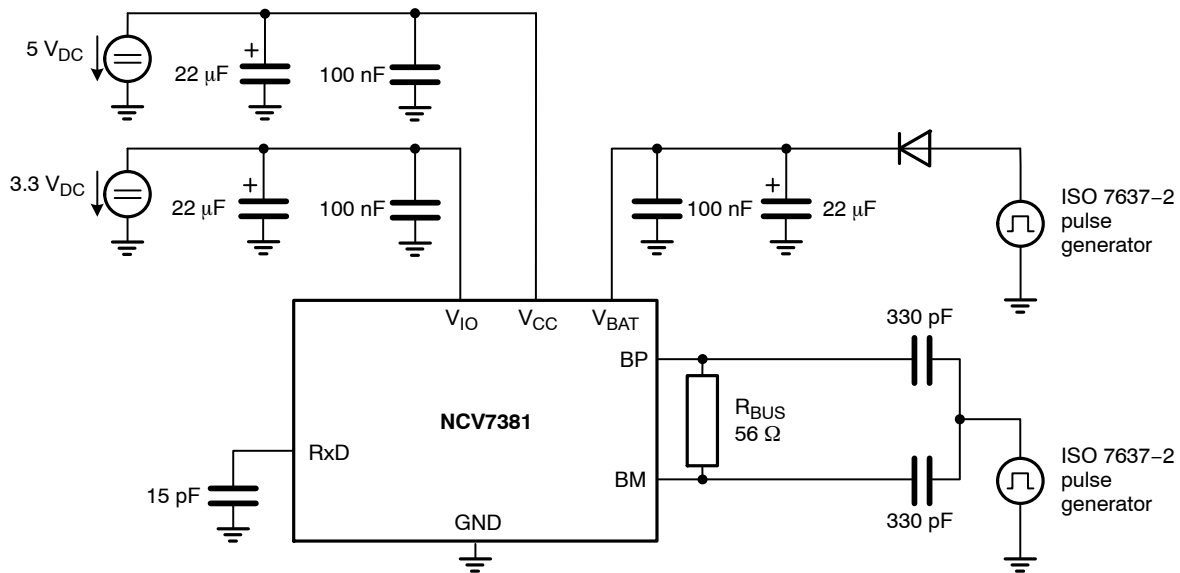


Figure 18. Test Setup for Measuring the Transient Immunity

### ORDERING INFORMATION

| Part Number    | Description                  | Temperature Range | Package       | Container <sup>†</sup> |          |
|----------------|------------------------------|-------------------|---------------|------------------------|----------|
|                |                              |                   |               | Type                   | Quantity |
| NCV7381ADP0R2G | Clamp 30 FlexRay Transceiver | -40°C to +125°C   | SSOP 16 GREEN | Tape & Reel            | 2000     |

### DISCONTINUED (Note 18)

|               |                              |                 |               |             |      |
|---------------|------------------------------|-----------------|---------------|-------------|------|
| NCV7381DP0G   | Clamp 30 FlexRay Transceiver | -40°C to +125°C | SSOP 16 GREEN | Tube        | 76   |
| NCV7381DP0R2G |                              |                 |               | Tape & Reel | 2000 |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

18. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on [www.onsemi.com](http://www.onsemi.com).

**SSOP 16**  
**CASE 565AE**  
**ISSUE O**

DATE 19 SEP 2008

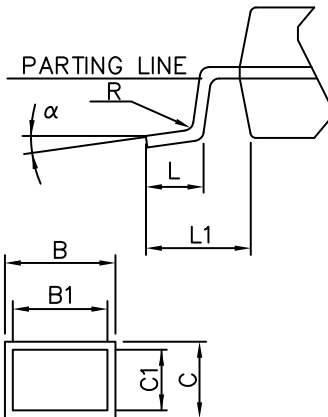
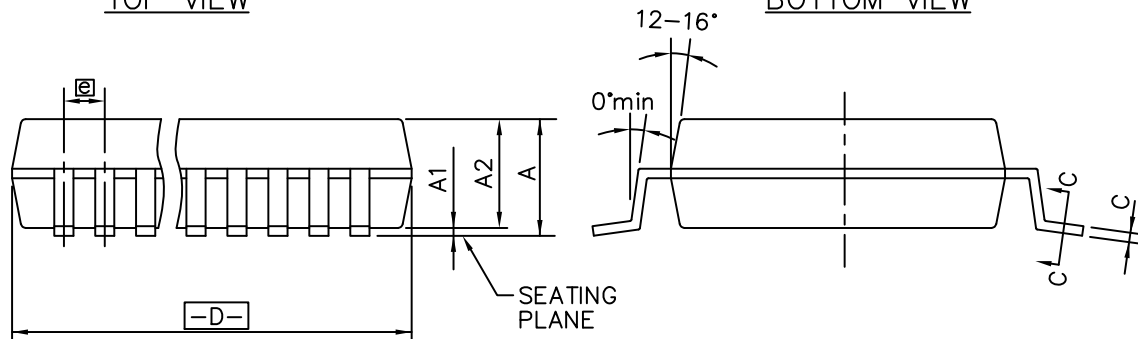
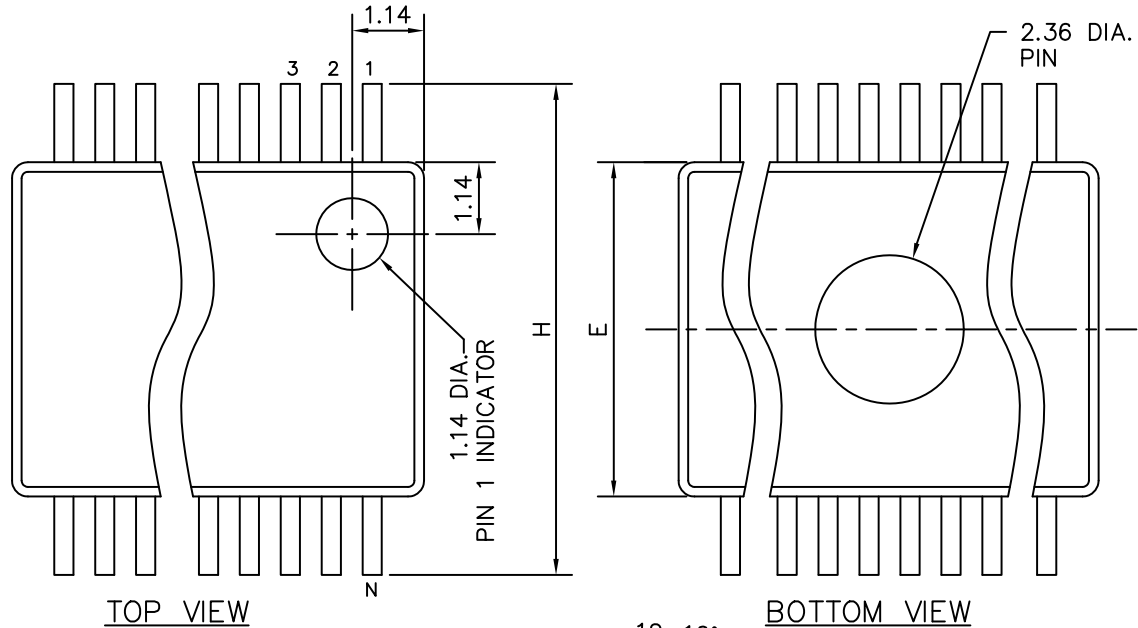


TABLE IN MILLIMETERS

| SYMBOL         | COMMON DIMENSIONS |      |      | NOTE | 1     |       |       |  | 2  |
|----------------|-------------------|------|------|------|-------|-------|-------|--|----|
|                | MIN.              | NOM. | MAX. |      | MIN.  | NOM.  | MAX.  |  |    |
| A              | 1.73              | 1.86 | 1.99 |      | 2.87  | 3.00  | 3.13  |  | 8  |
| A <sub>1</sub> | 0.05              | 0.13 | 0.21 | AA   | 6.07  | 6.20  | 6.33  |  | 14 |
| A <sub>2</sub> | 1.68              | 1.73 | 1.78 | AB   | 6.07  | 6.20  | 6.33  |  | 16 |
| B              | 0.25              | —    | 0.38 | AC   | 7.07  | 7.20  | 7.33  |  | 20 |
| B <sub>1</sub> | 0.25              | 0.30 | 0.33 | AD   | 8.07  | 8.20  | 8.33  |  | 24 |
| C              | 0.09              | —    | 0.20 | AE   | 10.07 | 10.20 | 10.33 |  | 28 |
| C <sub>1</sub> | 0.09              | 0.15 | 0.16 | AF   | 10.07 | 10.20 | 10.33 |  | 30 |
| D              | SEE VARIATIONS    |      |      | 1    |       |       |       |  |    |
| E              | 5.20              | 5.30 | 5.38 |      |       |       |       |  |    |
| e              | 0.65 BSC          |      |      |      |       |       |       |  |    |
| H              | 7.65              | 7.80 | 7.90 |      |       |       |       |  |    |
| L              | 0.63              | 0.75 | 0.95 |      |       |       |       |  |    |
| L <sub>1</sub> | 1.25 REF.         |      |      |      |       |       |       |  |    |
| N              | SEE VARIATIONS    |      |      | 2    |       |       |       |  |    |
| α              | 0°                | 4°   | 8°   |      |       |       |       |  |    |
| R              | 0.09              | 0.15 | —    |      |       |       |       |  |    |

**NOTE:**

MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.20mm on D PER SIDE.

**SECTION C-C**

|                         |                    |                                                                                                                                                                                  |
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