

MOSFET - Power, Single N-Channel, D²PAK7

80 V, 1.34 mΩ, 290 A

NVBGS1D2N08H

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualification
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	80	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	$T_C = 25^{\circ}\text{C}$	I_D	290	A
		$T_C = 100^{\circ}\text{C}$		205	
Power Dissipation $R_{\theta JC}$ (Note 2)		$T_C = 25^{\circ}\text{C}$	P_D	259	W
		$T_C = 100^{\circ}\text{C}$		130	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	43	A
		$T_A = 100^{\circ}\text{C}$		31	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		$T_A = 25^{\circ}\text{C}$	P_D	5.7	W
		$T_A = 100^{\circ}\text{C}$		2.9	
Pulsed Drain Current	$T_A = 25^{\circ}\text{C}$, $t_p = 100\text{ }\mu\text{s}$		I_{DM}	900	A
Operating Junction and Storage Temperature Range			T_J , T_{stg}	-55 to +175	$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	199	A
Single Pulse Drain-to-Source Avalanche Energy ($I_L = 32\text{ A}_{pk}$)			E_{AS}	1500	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 2)	$R_{\theta JC}$	0.58	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	26.2	

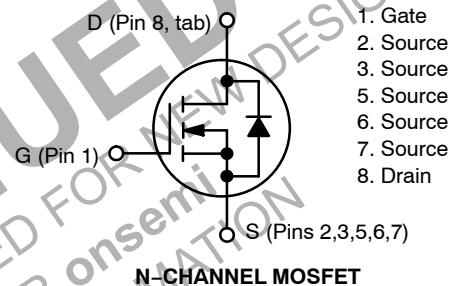
1. Surface-mounted on FR4 board using a 1 in² pad size, 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.



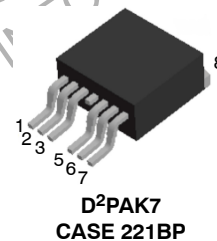
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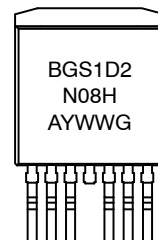
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
80 V	1.34 mΩ @ 10 V	290 A



N-CHANNEL MOSFET



MARKING DIAGRAM



BGS1D2N08H = Specific Device Code

A = Assembly Location

Y = Year

WW = Work Week

G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NVBGS1D2N08H	D ² PAK7 (Pb-Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NVBGS1D2N08H

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\text{ }\mu\text{A}$, ref to 25°C		56		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		250	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 650\text{ }\mu\text{A}$	2.0	2.9	4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 650\text{ }\mu\text{A}$, ref to 25°C		-7.5		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		1.1	1.34	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 50\text{ A}$		213		S
Gate-Resistance	R_G			0.5		Ω

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, f = 1\text{ MHz}$	10830			pF
Output Capacitance	C_{OSS}		1605			
Reverse Transfer Capacitance	C_{RSS}		45			
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 40\text{ V}; I_D = 50\text{ A}$	160			nC
Threshold Gate Charge	$Q_{G(TH)}$		28			
Gate-to-Source Charge	Q_{GS}		43			
Gate-to-Drain Charge	Q_{GD}		33			
Plateau Voltage	V_{GP}		4.3			V

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 64\text{ V}, I_D = 50\text{ A}, R_G = 6\text{ }\Omega$	40			ns
Rise Time	t_r		34			
Turn-Off Delay Time	$t_{d(OFF)}$		134			
Fall Time	t_f		45			

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}$	$T_J = 25^\circ\text{C}$		0.8	1.3	V
			$T_J = 125^\circ\text{C}$		0.65		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 50\text{ A}$		78			ns
Reverse Recovery Charge	Q_{RR}			122			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS

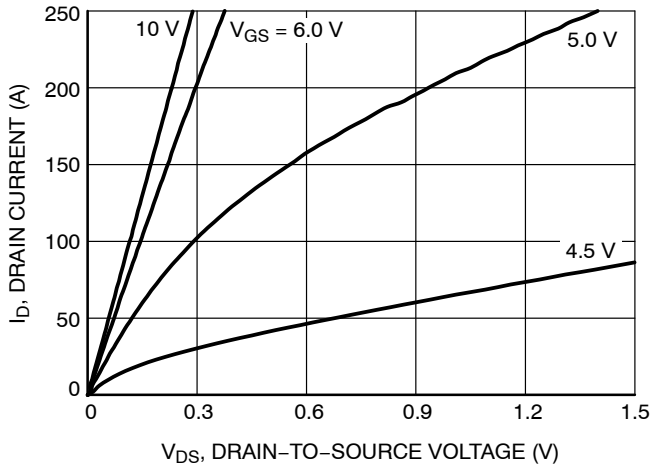


Figure 1. On-Region Characteristics

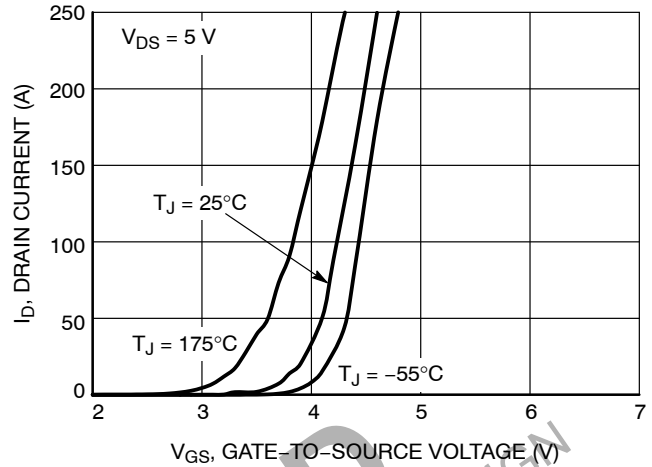


Figure 2. Transfer Characteristics

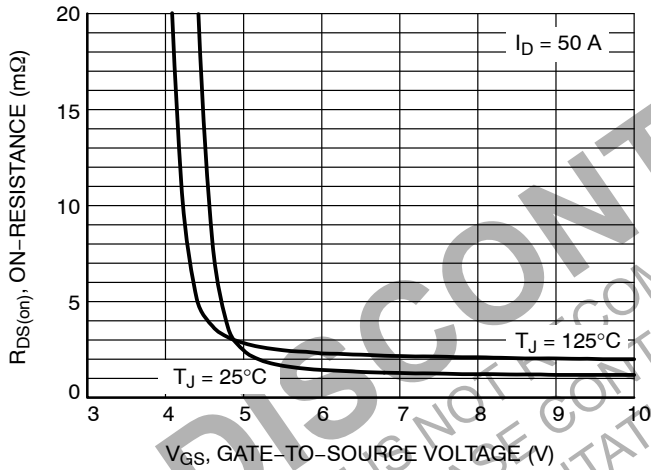


Figure 3. On-Resistance vs. Gate-to-Source Voltage

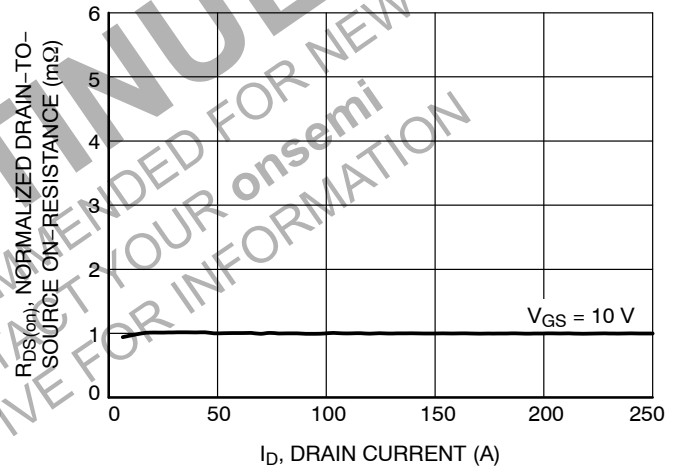


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

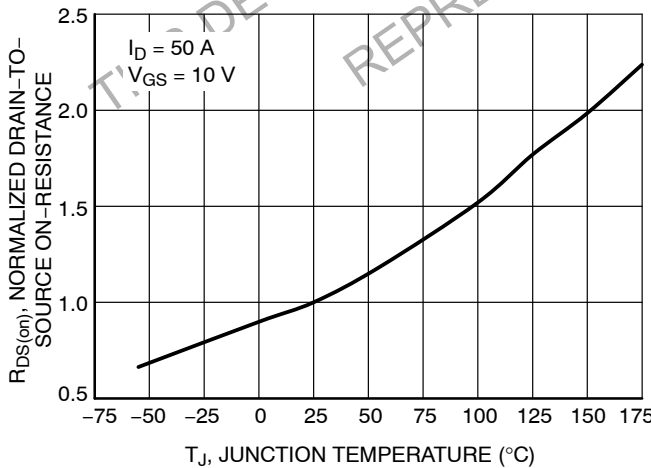


Figure 5. On-Resistance Variation with Temperature

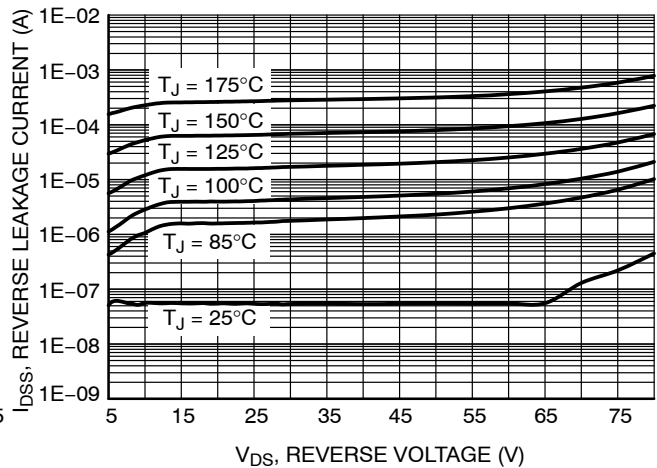


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

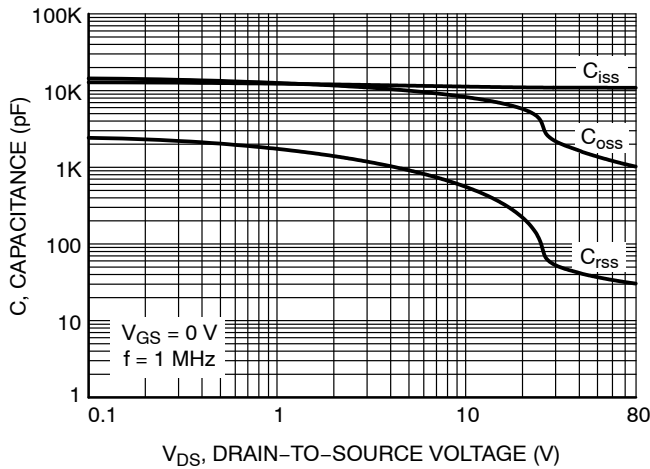


Figure 7. Capacitance Variation

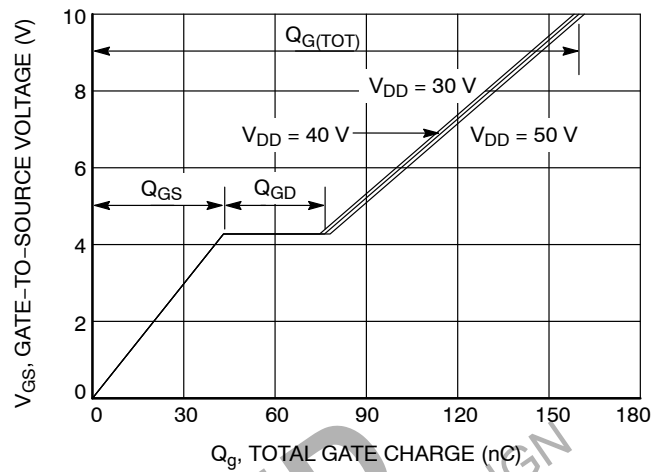


Figure 8. Gate-to-Source vs. Total Charge

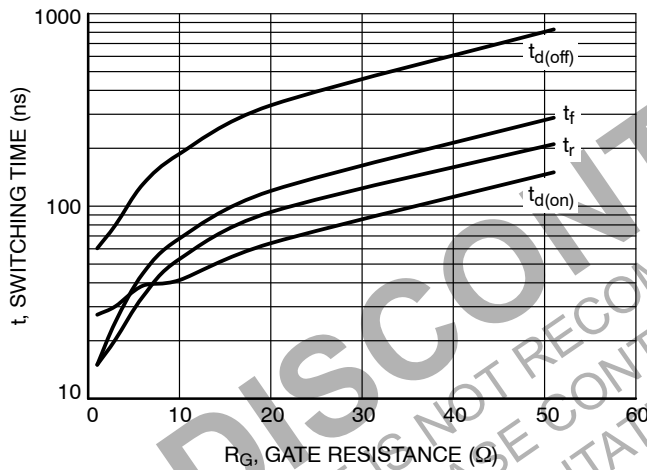


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

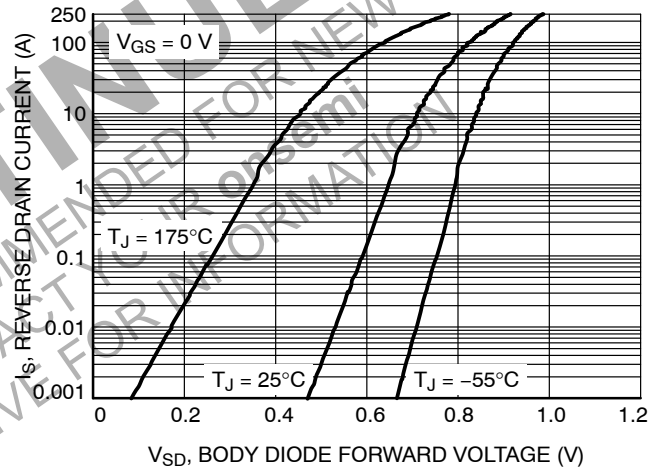


Figure 10. Diode Forward Voltage vs. Current

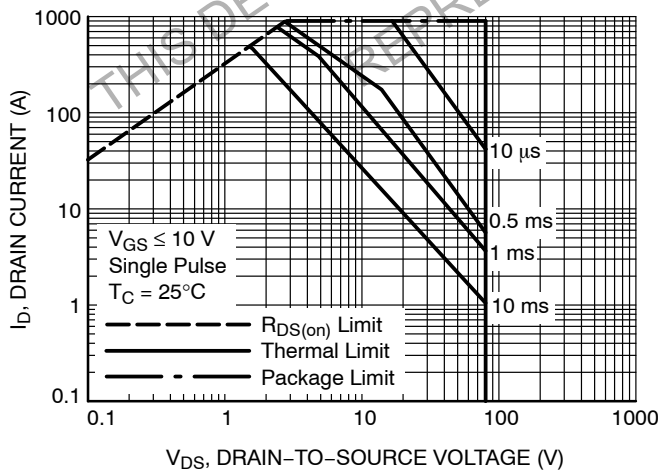


Figure 11. Maximum Rated Forward Biased Safe Operating Area

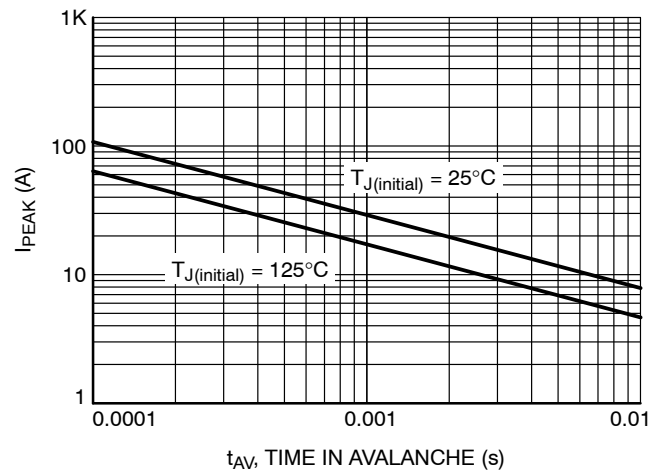


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

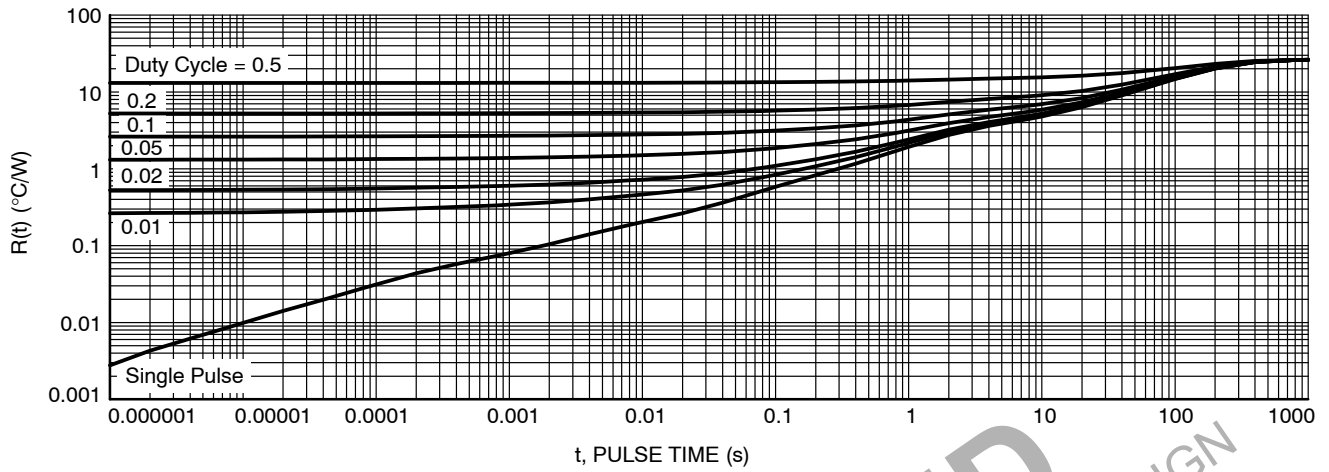


Figure 13. Transient Thermal Impedance

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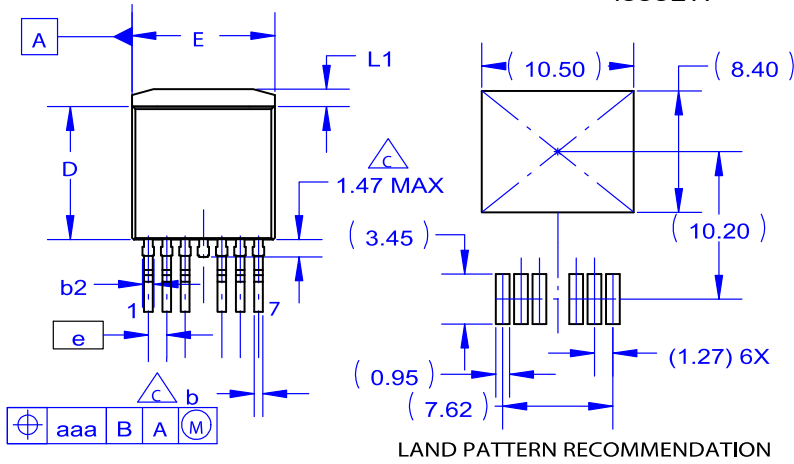
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PACKAGE DIMENSIONS

D2PAK7 (TO-263-7LD) 15.4x9.9x4.5

CASE 221BP

ISSUE A



NOTES:

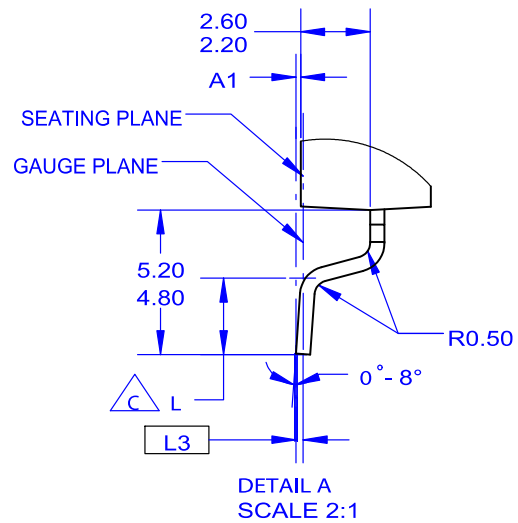
A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.
B. ALL DIMENSIONS ARE IN MILLIMETERS.

△ OUT OF JEDEC STANDARD VALUE.

D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.

E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
F. LAND PATTERN RECOMMENDATION PER IPC, TO127P1524X465-8N.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	0.00	0.10	0.20
b2	0.60	0.70	0.80
b	0.50	0.60	0.70
c	0.40	0.50	0.60
c2	1.20	1.30	1.40
D	9.00	9.20	9.40
D1	7.30	7.80	8.20
E	9.70	9.90	10.20
E1	7.15	8.05	8.55
e	~	1.27	~
H	15.10	15.40	15.70
L	2.44	2.64	2.84
L1	1.00	1.20	1.40
L3	~	0.25	~
aaa	~	~	0.25



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