User's Guide

ISOW1432 Isolated RS-485/RS-422 Transceiver With Integrated DC-DC Converter Evaluation Module

ABSTRACT

This user's guide describes the evaluation module (EVM) for an isolated RS-485 transceiver with integrated DC-DC converter. This EVM helps designers evaluate the device performance for fast development and analysis of data transmission systems using the ISOW1432 device in a 20-pin DFM package.

CAUTION

This evaluation module is made available for isolator parameter performance evaluation only and is not intended for isolation voltage testing. To prevent damage to the EVM, any voltage applied as supply to LDO inputs must be maintained within 0 V to 12 V range and voltage applied to device device supply or data input/output pins must be maintained within 0 V to 5.5 V range as specified in datasheet section "Recommonded Operating Conditions".

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1 Introduction

ISOW1432 is a galvanically-isolated differential line transceiver with a built-in isolated DC-DC converter for TIA/EIA RS-485 and RS-422 applications. Both signal and power paths are isolated per UL1577 and are qualified for reinforced isolation per VDE, CSA and CQC. These devices do not require any external components other than bypass capacitors to realize an isolated RS-485 port. The low-emissions, isolated DC/DC converter ensures the final system is capable of meeting CISPR 32 radiated emissions limit lines with just two ferrite beads.

The device is ideal for long distance communications. Isolation breaks the ground loop between the communicating nodes, allowing for a much larger common-mode voltage range. It supports a maximum datarate of 12 Mbps. It can operate from a single supply voltage of 3 V to 5.5 V by connecting V_{IO} and V_{DD} together on PCB. If lower logic levels are required, these devices support 1.71 V to 5.5 V logic supply (V_{IO}) that can be independent from the power converter supply (V_{DD}) of 3 V to 5.5 V. These devices support a wide operating ambient temperature range from –40°C to 105°C and are available in 20-pin DFM (SOIC footprint compatible package) offering a minimum of 8 mm creepage and clearance.

ISOW1432DFMEVM can be used to evaluate different system parameters of the devices. Test signals and sequences can be applied to the device and different performance characteristics can be observed such as propagation delay, power consumption, and different bus and driver conditions. Users can evaluate these parameters in their own lab environment.

The EVM has footprints named *DNI* for additional components that are not needed to test the standard functionality. Add components to these footprints for evaluation and to get specific system requirements. Refer to this users guide for the basic functionality that can be assessed with the EVM.

2 Functional Block Diagram and Pin Configuration of ISOW1432

2.1 Functional Block Diagram and Pin Configuration

Figure 2-1 shows functional block diagram of isolated full-duplex RS-485 transceiver with integrated DC-DC converter, ISOW1432. Figure 2-2 shows the pin configuration of the ISOW1432 in the 20-pin DFM package.

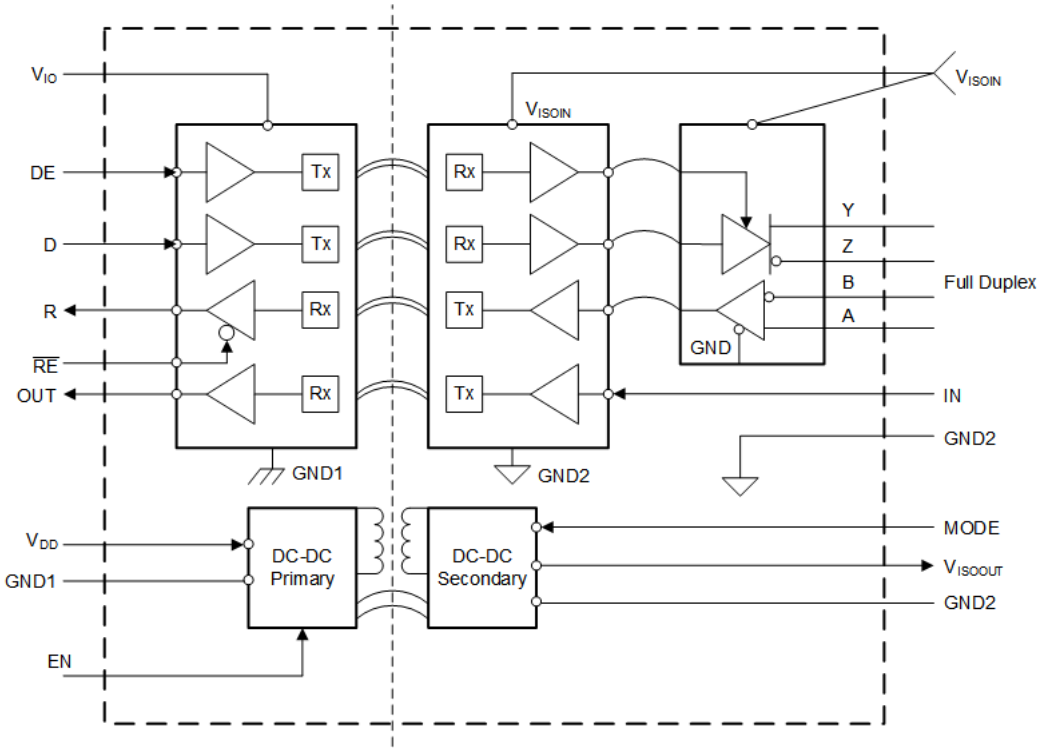


Figure 2-1. ISOW1432 Functional Block Diagram

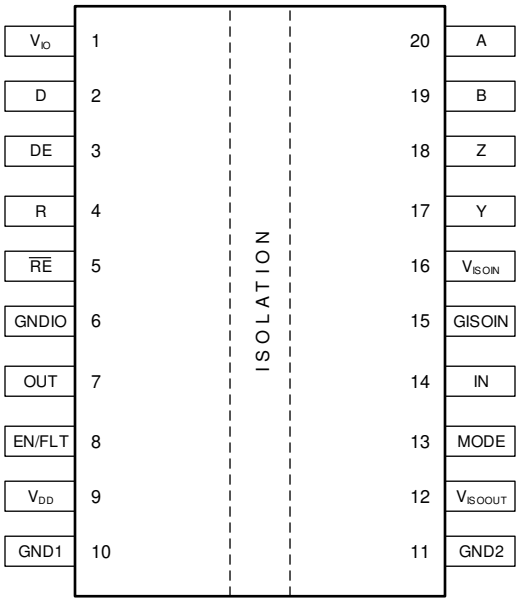


Figure 2-2. ISOW1432 Pin Configuration

3 EVM Schematic

Figure 3-1, Figure 3-2 and Figure 3-3 show the ISOW1432DFMEVM schematic.

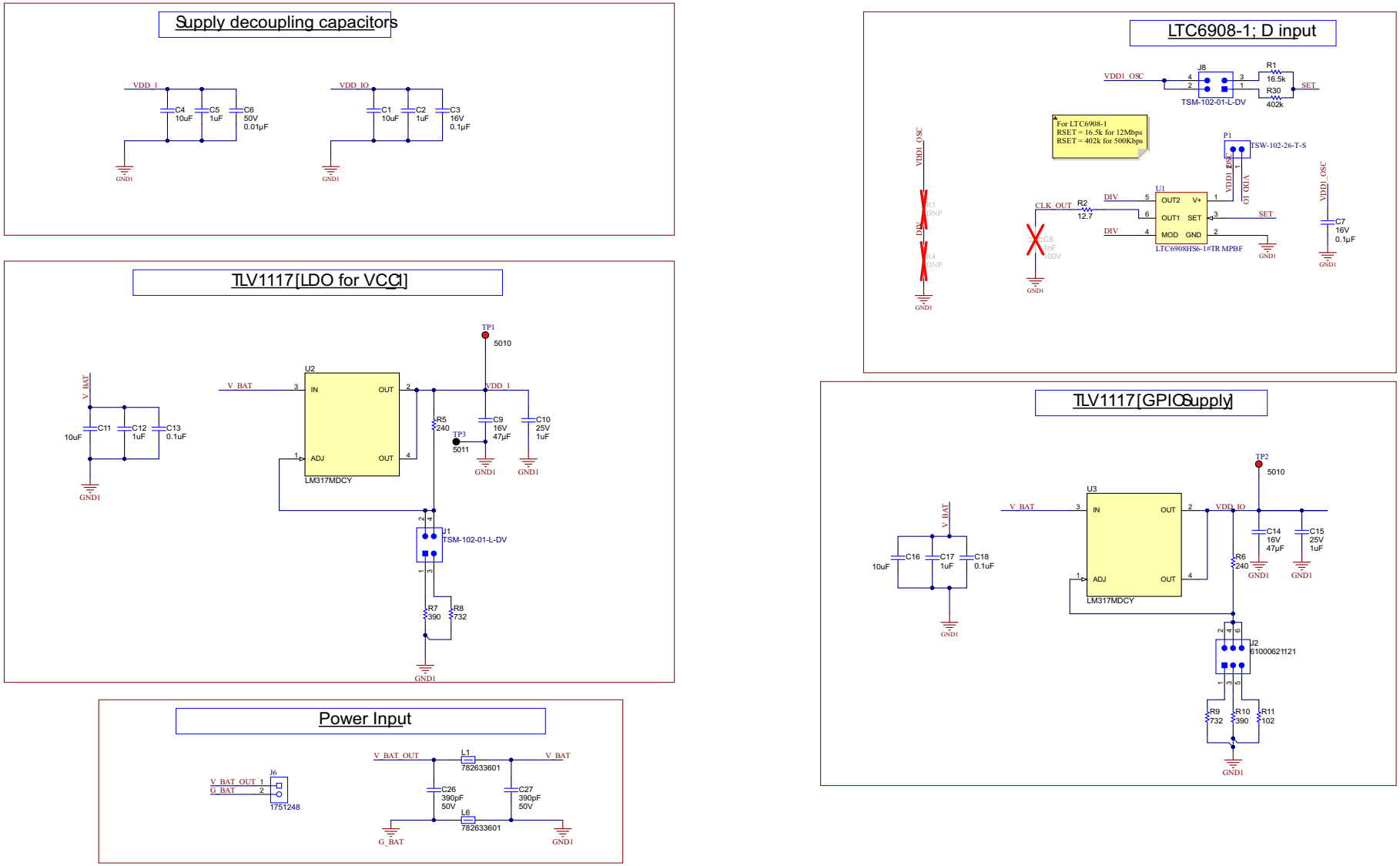


Figure 3-1. ISOW1432DFMEVM Schematic - Power

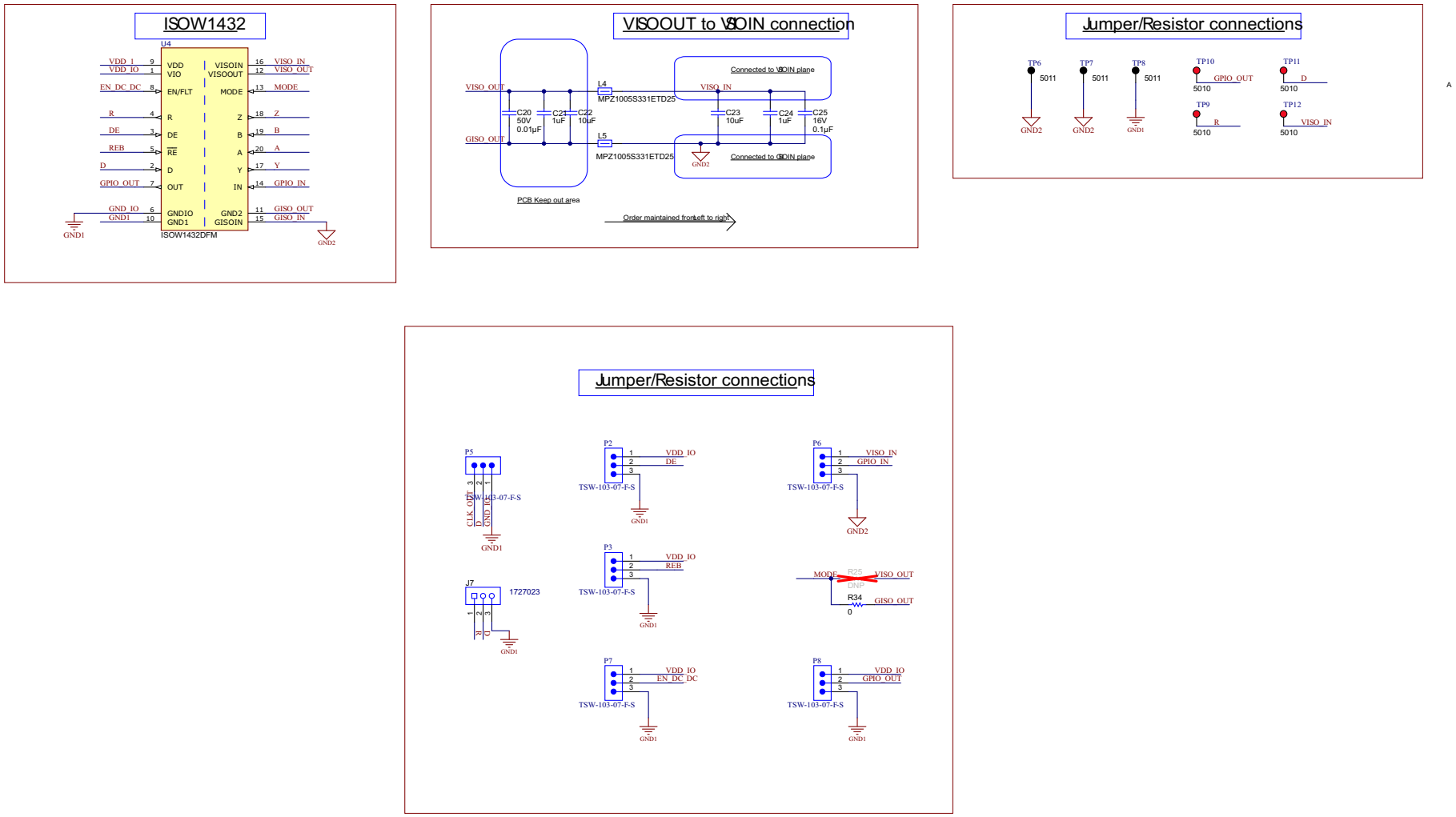
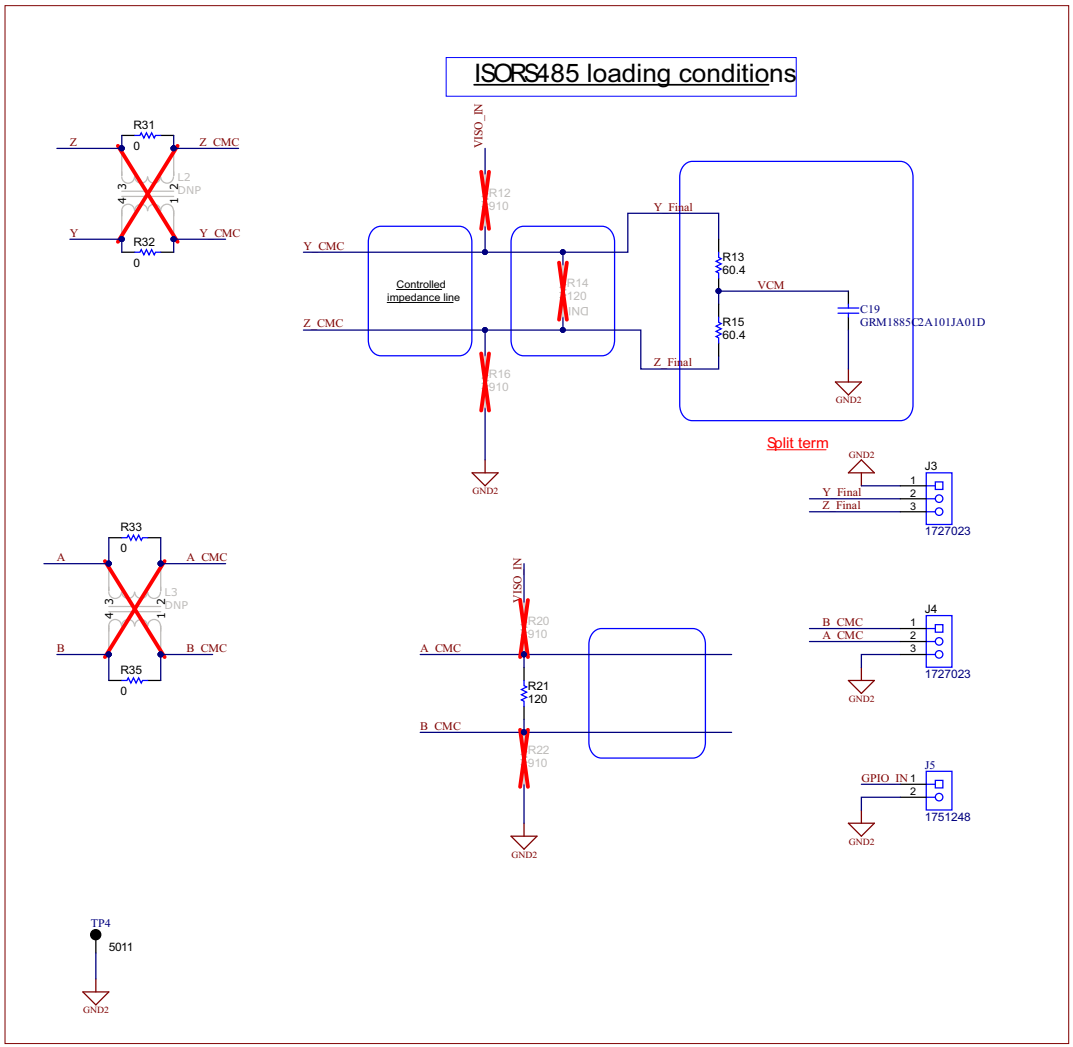


Figure 3-2. ISOW1432DFMEVM Schematic - Isolator



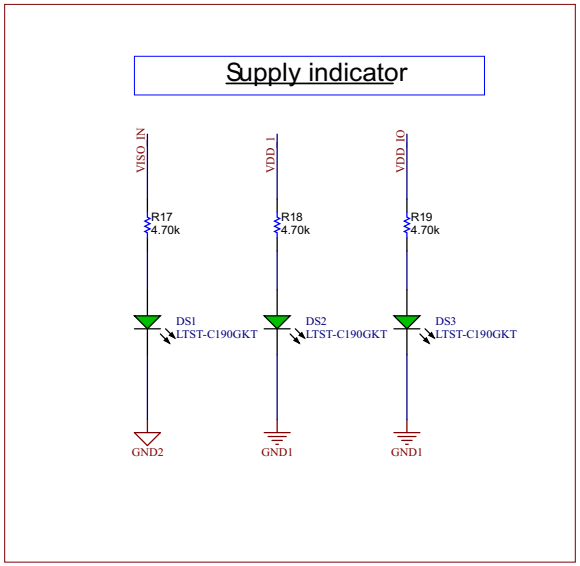


Figure 3-3. ISOW1432DFMEVM Schematic - RS-485 Bus

4 EVM 3D Diagram and PCB Layout

Figure 4-1 shows 3D diagram of ISOW1432DFMEVM. Figure 4-2 and Figure 4-3 show the PCB layout of ISOW1432DFMEVM, respectively.

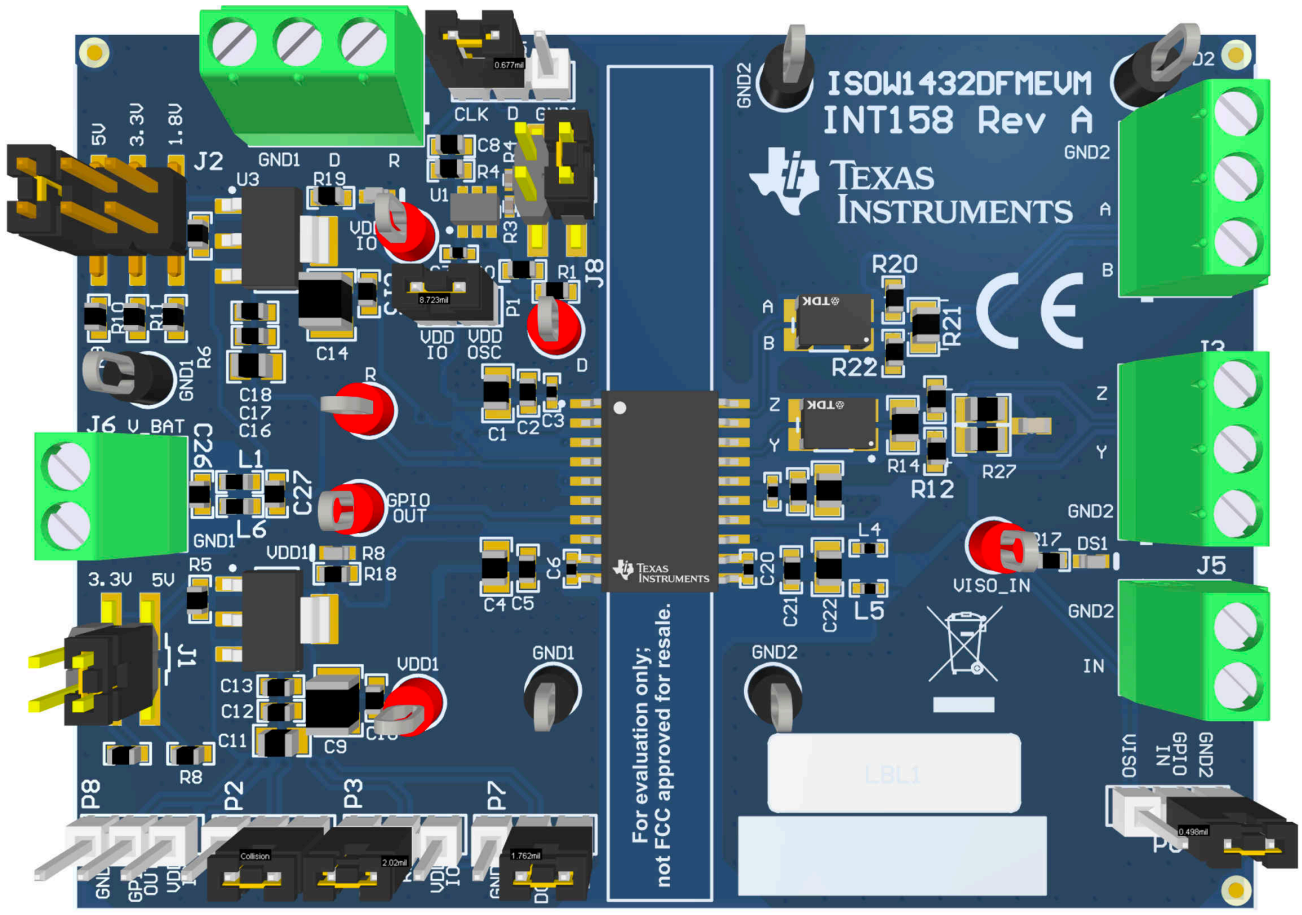


Figure 4-1. ISOW1432DFMEVM PCB 3D diagram

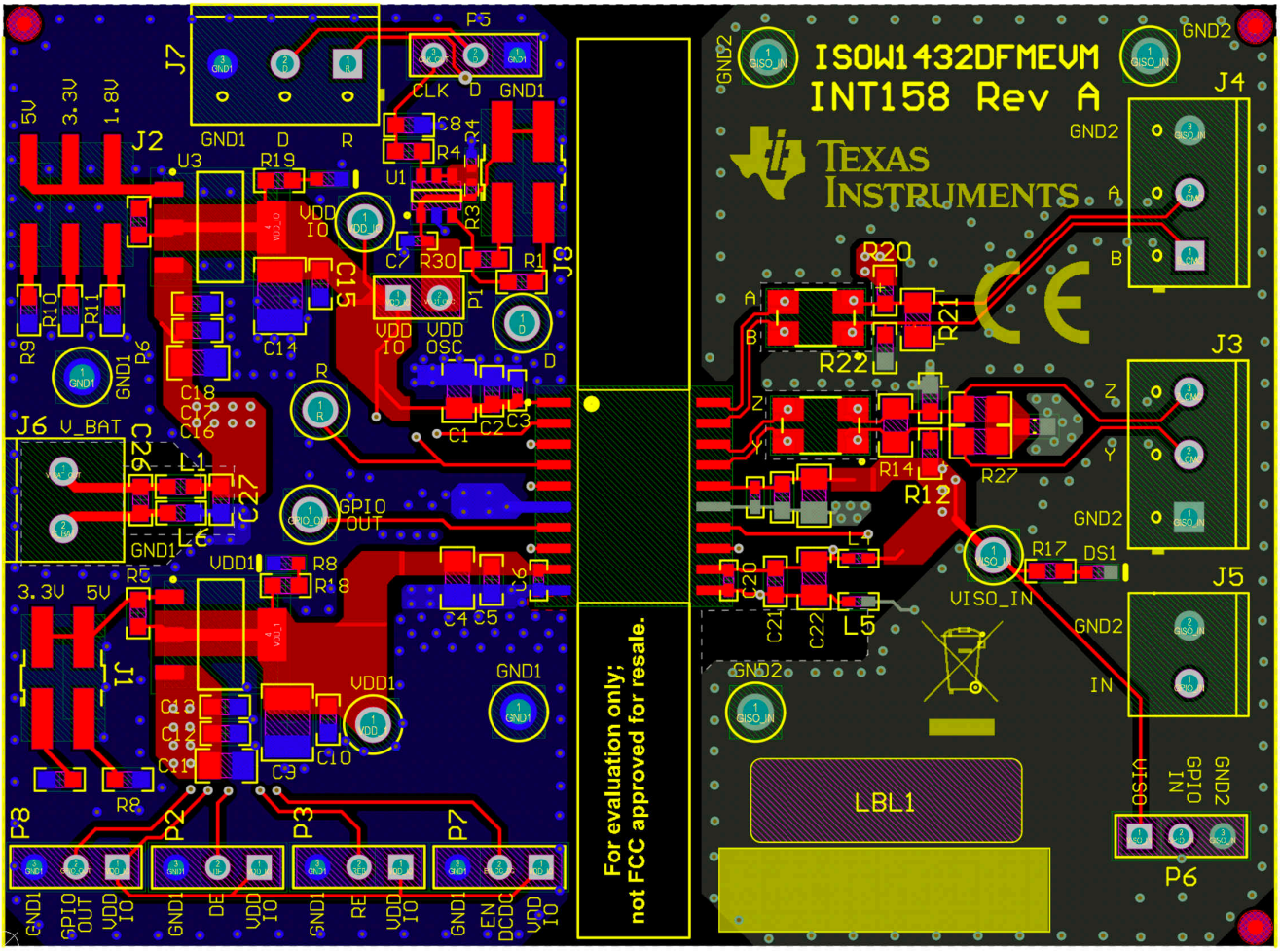


Figure 4-2. ISOW1432DFMEVM PCB Layout - Top Layer

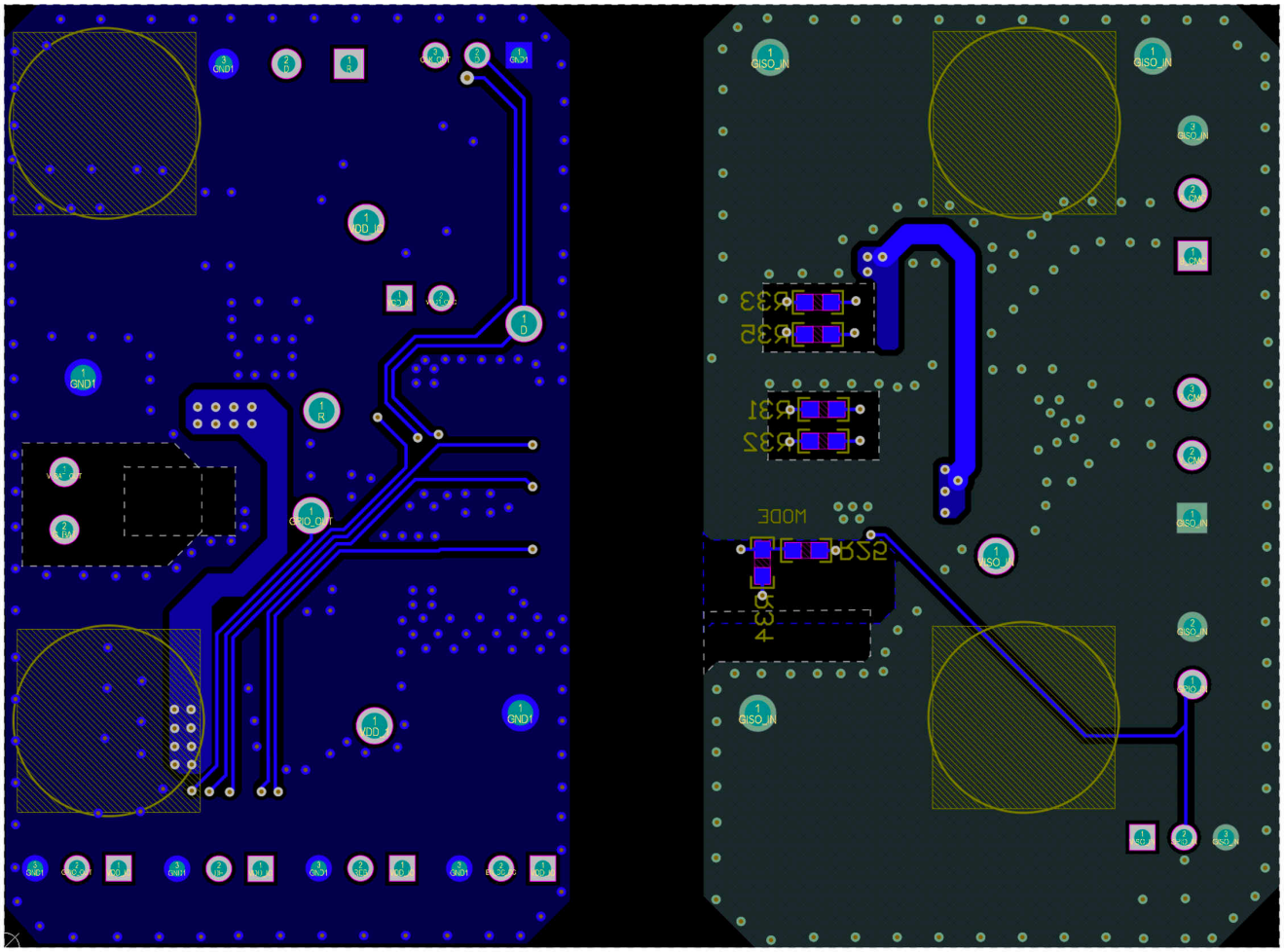


Figure 4-3. ISOW1432DFMEVM PCB Layout - Bottom Layer

5 Bill of Materials

Table 5-1 shows the bill of materials for ISOW1432DFMEVM.

Table 5-1. Bill of Materials

Item	Designator	Description	Manufacturer	PartNumber
1	C1, C4, C11, C16, C22, C23	CAP, CERM, 10 uF, 35 V, +/- 10%, X5R, 0805	MuRata	GRM21BR6YA106KE43L
2	C2, C5, C12, C17, C21, C24	CAP, CERM, 1 uF, 50 V, +/- 10%, X5R, 0603	Samsung Electro-Mechanics	CL10A105KA8NNNC
3	C3, C7, C25	CAP, CERM, 0.1 µF, 16 V,+/- 10%, X7R, 0402	Walsin	CL05B104KO5NNNC
4	C6, C20	CAP, CERM, 0.01 µF, 50 V,+/- 10%, X7R, 0402	Walsin	0402B103K500CT
5	C9, C14	CAP, CERM, 47 µF, 16 V,+/- 10%, X5R, 1210	Samsung Electro-Mechanics	CL32A476KOJNNNE
6	C10, C15	CAP, CERM, 1 uF, 50 V, +/- 10%, X5R, 0603	Samsung Electro-Mechanics	CL10A105KA8NNNC
7	C13, C18	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	AVX	06033C104JAT2A
8	C19	CAP 100pF 50V ±5% 0603	MuRata	GCG1885G1H101JA01D
9	C26, C27	CAP, CERM, 390 pF, 100 V, +/- 10%, X7R, 0603	MuRata	GCM1885C2A391JA16D
10	DS1, DS2, DS3	LED Uni-Color Green, 100 mW, 5 V, -55 to 85 degC, 2-Pin SMD, RoHS, Tape and Reel		LTST-C190GKT
11	H1, H2, H3, H4	Bumpon, Hemisphere, 0.44 X 0.20, Clear	3M	SJ-5303 (CLEAR)
12	J1, J8	Header, 2.54mm, 2x2, Gold, SMT	Samtec	TSM-102-01-L-DV
13	J2	Header, 2.54mm, 3x2, Gold, SMT	Wurth Elektronik	61000621121
14	J3, J4, J7	Terminal Block Receptacle, 3x1, 3.81mm, R/A, TH	Phoenix Contact	1727023
15	J5, J6	Conn Term Block, 2POS, 3.5mm, TH	Phoenix Contact	1751248
16	L1, L6	Ferrite Bead, 600 ohm @ 100 MHz, 1 A, 0603	Wurth Elektronik	782633601
17	L4, L5	Ferrite Bead, 330 ohm @ 100 MHz, 0.7 A, 0402	TDK	MPZ1005S331ETD25
18	LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Brady	THT-14-423-10
19	P1		Samtec	TSW-102-26-T-S
20	P2, P3, P5, P6, P7, P8		Samtec	TSW-103-07-F-S
21	R1	RES, 16.5 k, 1%, 0.1 W, 0603	Yageo	RC0603FR-0716K5L
22	R2	RES, 12.7, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060312R7FKEA
23	R5, R6	RES, 240, 1%, 0.1 W, 0603	Yageo	RC0603FR-07240RL
24	R7, R10	RES, 390, 1%, 0.1 W, 0603	Yageo	RC0603FR-07390RL
25	R8, R9	RES, 732, 1%, 0.1 W, 0603	Yageo	RC0603FR-07732RL
26	R11	RES, 102, 1%, 0.1 W, 0603	Yageo	RC0603FR-07102RL
27	R13, R15	RES, 60.4, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	Vishay-Dale	CRCW080560R4FKEA
28	R17, R18, R19	RES, 4.70 k, 1%, 0.1 W, 0603	Yageo	RC0603FR-074K7L
29	R21	RES, 120, 1%, 0.4 W, 0805	Rohm	ESR10EZPF1200
30	R30	RES, 402 k, 1%, 0.1 W, 0603	Yageo	RC0603FR-07402KL
31	R31, R32, R33, R34, R35	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Stackpole Electronics Inc	RMCF0603ZT0R00
32	SH-J3, SH-J4, SH-J5, SH-J6, SH-J8	Shunt, 100mil, Gold plated, Black	Samtec	SNT-100-BK-G
33	TP1, TP2, TP9, TP10, TP11, TP12	Test Point, Multipurpose, Red, TH	Keystone	5010
34	TP3, TP4, TP6, TP7, TP8	Test Point, Multipurpose, Black, TH	Keystone	5011
35	U1	Micropower, Regulated Charge Pump with Shutdown, 2.7 to 5.5 V Vin, 5 V Vout, 6-pin SOT23 (S6-6), -40 to 85 degC, Pb-Free	Linear Technology	LTC6908HS6-1#TRMPBF
36	U2, U3	3/4 Pin 500mA Adjustable Positive Voltage Regulator, DCY0004A (SOT-223-4)	Texas Instruments	LM317MDCY

Table 5-1. Bill of Materials (continued)

Item	Designator	Description	Manufacturer	PartNumber
37	U4	Reinforced 5-kVRMS Isolated RS-485/RS-422 Transceiver With Integrated Low Emissions DC-DC Converter	Texas Instruments	ISOW1432DFM
38	C8	CAP, CERM, 1000 pF, 100 V, +/- 10%, X7R, 0603	MuRata	GRM188R72A102KA01D
39	L2, L3, R3, R4	100µH @ 100kHz 2 Line Common Mode Choke Surface Mount 5.8 kOhms @ 10MHz 150mA DCR 2Ohm, 0402 (1005 Metric) Chip Resistor	TDK	
40	R12, R16, R20, R22	RES, 910, 1%, 0.1 W, 0603	Yageo	RC0603FR-07910RL
41	R14	RES, 120, 1%, 0.4 W, 0805	Rohm	ESR10EZPF1200
42	R25	RES, 49.9, 1%, 0.1 W, 0603	Yageo	RC0603FR-0749R9L
43	SH-J1, SH-J2, SH-J7, SH-J9	Shunt, 100mil, Gold plated, Black	Samtec	SNT-100-BK-G

6 EVM Setup and Operation

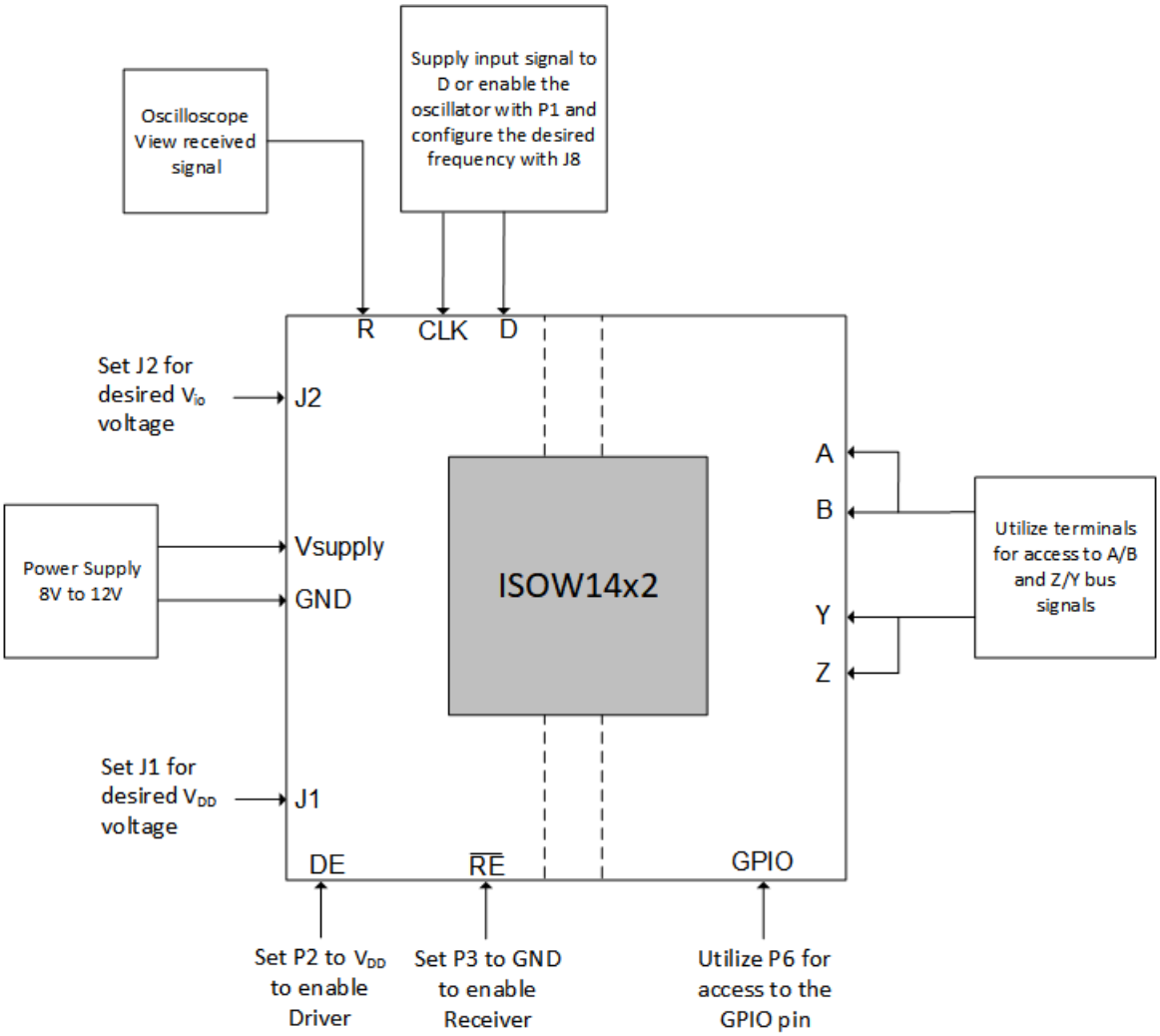
Figure 6-1 shows the basic setup of the EVM with only a single power supply needed to evaluate isolator performance.

Use voltages that are within the range given in the device data sheet. The LDOs on the EVM will provide V_{DD} as configured by their jumpers. The supply voltage to the EVM should ideally be between 8 V and 12 V. ISOW1432 will generate the isolated power for V_{ISOOUT} that is connected to V_{ISOOIN} on the EVM.

The EVM features an on-board oscillator device that can be used to provide a clock signal to D pin of ISOW1432. The oscillator is bridged to the D input through the Jumper P1 and can be configured to output 12 Mbps or 500 kbps by changing the configuration of J8. Utilizing the on-board oscillator is recommended if conducting any emissions testing on the EVM.

There are two LDOs on the EVM to provide V_{DD} and V_{IO} voltages separately. One can change the LDO output voltage by reconfiguring the jumpers on J1 and J2. J1 controls the output voltage of the LDO supplying V_{DD} and can be 3.3 V or 5 V. J2 controls the output voltage of the LDO supplying Vio and can be 1.8 V, 3.3 V, or 5 V.

J4 and J3 are the terminals that provide access to the A/B and Z/Y bus lines, respectively. These can be used to connect to other RS-485 devices.



A. Normal transceiver operation requires both the driver and the receiver sections to be active. Set the receiver enable pin ($\overline{RE}$) to logic low and the driver enable pin (DE) to logic high to enable both the driver and receiver.

Figure 6-1. Basic EVM Setup

Table 6-1 shows the information on jumper configuration for basic tests.

Table 6-1. Jumper Configuration

Connection	Label	Description
J1	3.3 V, 5 V	Connect this jumper to choose the desired V_{DD} voltage of either 3.3 V or 5 V.
J2	1.8 V, 3.3 V, 5 V	Connect this jumper to choose the desired V_{IO} voltage of 1.8 V, 3.3 V, or 5 V.
J8	J8	Connect this jumper to choose the desired oscillator switching frequency
P1	VDD IO, VDD OSC	Connect this jumper to power on and enable the oscillator.
P2	VDD IO, DE, GND1	Connect this jumper between the middle pin and GND1 to tie the DE pin low. The driver input is disabled when the DE pin is low. Connect this jumper between the middle pin and VDD IO to tie the DE pin high. The driver input is enabled when the DE pin is high. Tie the DE pin to VDD IO for full operation tests.
P3	VDD IO, $\overline{RE}$, GND1	Connect this jumper between the middle pin and GND1 to tie the $\overline{RE}$ pin low. The receiver is enabled when the $\overline{RE}$ pin is low. Tie the $\overline{RE}$ pin to GND1 for full operation tests. Connect this jumper between the middle pin and VDD IO to tie the $\overline{RE}$ pin high. The receiver is disabled when the $\overline{RE}$ pin is high.
P7	VDD IO, EN, GND1	Connect this jumper between the middle pin and GND1 to disable the DC-DC converter. Leave jumper off or conencted to VDD IO to enable DC-DC converter.

7 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265