User's Guide

TPS62120 Buck Converter Evaluation Module User's Guide

ABSTRACT

This user's guide describes the characteristics, operation, and use of the TPS62120 evaluation module (EVM). The TPS62120EVM-640 is a fully assembled and tested circuit for evaluating the performance of the TPS62120 high-input voltage step-down converter. This document includes schematic diagrams, a printed circuit board (PCB) layout, bill of materials, and test data. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the TPS62120EVM-640 unless otherwise noted.

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Trademarks

1 Introduction

The TPS62120 is a high-efficiency, synchronous step-down, dc-dc converter optimized for low-power applications. The wide operating input voltage range of 2 V to 15 V supports energy harvesting and battery-powered as well 9-V or 12-V line-powered applications.

The TPS62120EVM-640 is a fully assembled and tested platform for evaluating the operation and performance of the TPS62120 converter. The TPS62120EVM-640 has an input voltage range from 2.0 V up to 15 V, and the output voltage is adjustable with an external feedback divider network in the range of 1.2 V to 5.5 V. The maximum output current of the EVM circuit is 75 mA.

1.1 Features

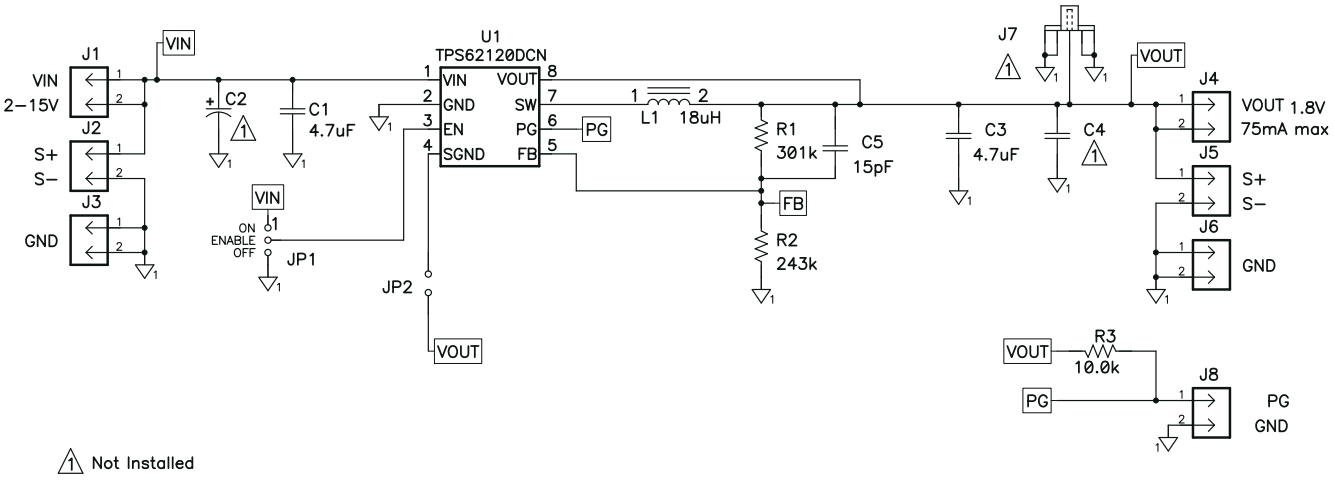
- High input voltage range: 2.0 V up to 15 V
- Adjustable output voltage: 1.2 V up to 5.5 V
- Up to 75-mA output current
- Up to 800-kHz switching frequency

1.2 Applications

- Ultralow-power microcontroller supply
- Energy harvesting
- Industrial measurement

2 TPS62120EVM Schematic

TPS62120EVM Schematic illustrates the TPS62120EVM-640 schematic.



For reference only; see Table 7-1 for specific values.

Figure 2-1. TPS62120EVM Schematic

3 Connector and Test Point Descriptions

3.1 Enable Jumpers/Switches (RefDes) TPS62120

3.1.1 J1 VIN

This header is the positive connection to the input power supply. The power supply must be connected between J1 and J3 (GND). The leads to the input supply should be twisted and kept as short as possible. The input voltage must be between 2.0 V and 15.0 V.

3.1.2 J2 S+/S–

J2 S+/S– are the sense connection for the input of the converter. Connect a voltmeter, sense connection of a power supply, or oscilloscope to this header.

3.1.3 J3 GND

This header is the return connection to the input power supply. Connect the power supply between J3 and J11 (VIN). The leads to the input supply should be twisted and kept as short as possible. The input voltage must be between 2.0 V and 15.0 V.

3.1.4 J4 VOUT

This header is the positive output of the step-down converter. The output voltage of the TPS62120 is adjustable, with the feedback resistors R1 and R2. On the EVM, the output voltage can be adjusted in the range of 1.2 V to 5.5 V.

Note: A feed-forward capacitor is required. Refer to the TPS62120 data sheet (SLVSAD5) for detailed information.

3.1.5 J5 S+/S–

J5 S+/S– are the sense connection for the output of the converter. Connect a voltmeter, sense connection of an electronic load, or oscilloscope to this header.

3.1.6 J6 GND

J6 is the return connection of the converter. A load can be connected between J4and J6 (VOUT). The converter is able to support a load current of up to 75 mA.

3.1.7 JP1 EN

This jumper enables/disables the TPS62120 on the EVM. The shorting jumper JP1 between the center pin and ON turns on the unit. Shorting the jumper between the center pin and OFF turns the unit off.

3.1.8 JP2 SGND

JP2 connects the output capacitor of the TPS62120 to the open drain output SGND. SGND is low when the TPS62120 is in shutdown mode, thus discharging the output capacitor. If the TPS62120 is enabled, the open drain output SGND is high impedance.

3.1.9 J7 VOUT (SMA)

The J7 SMA connector is connected to the output voltage of the TPS62120. The noise spectrum of the output voltage can be easily analyzed with a spectrum analyzer.

By default, J7 is not assembled on the EVM.

3.1.10 J8 PG/GND

J8 pin 1 is connected to the Power Good (PG) output of the TPS62120. This open drain output is pulled up to VOUT with R3. PG output goes high when the FB voltage rises above 95% (typ) of its nominal value. PG goes low when the FB voltage drops below 90% (typ) of its nominal value.

4 Test Configuration

4.1 Hardware Setup

Figure 4-1 illustrates a typical hardware test configuration.

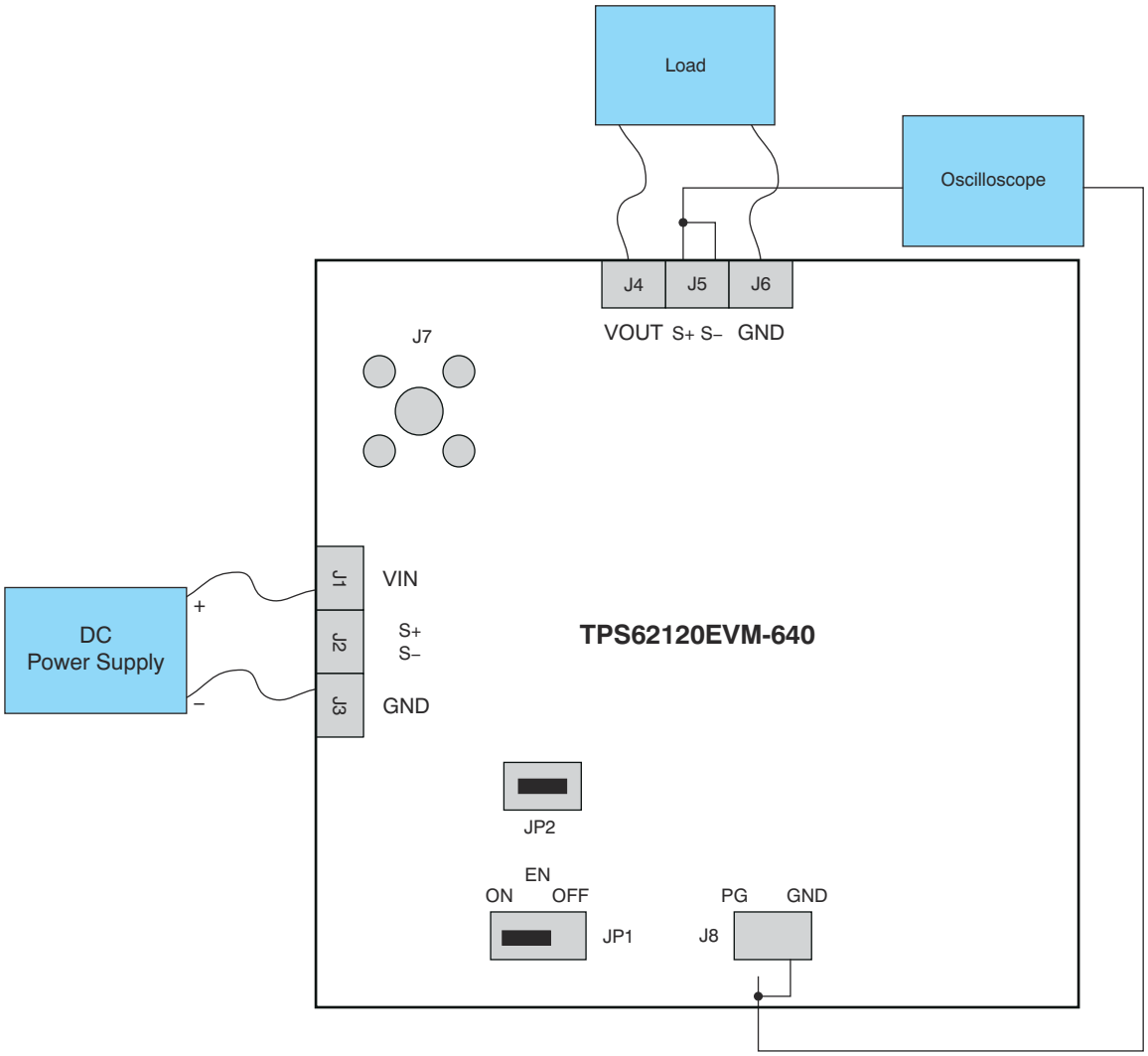


Figure 4-1. Hardware Board Connection

4.2 Procedure

Follow these procedures when configuring the EVM for testing.

CAUTION

Many of the components on the TPS62120EVM-640 are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap, bootstraps, or mats at an approved ESD workstation. An electrostatic smock and safety glasses should also be worn.

1. Work at an ESD workstation. Make sure that any wrist straps, bootstraps, or mats are connected and reference the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Connect a dc power supply between J1 and J3 on the TPS62120EVM. Note that the input voltage should range from 2.0 V to 15 V. Keep the wires from the input power supply to EVM as short as possible and twisted.
3. Connect a dc voltmeter or oscilloscope to the output sense connection (J5) of the EVM.
4. A load of up to 75 mA can be connected between J4 and J6 on the TPS62120EVM.
5. To enable the converter, connect the shorting bar on JP1 between EN and ON on the TPS62120EVM.

5 TPS62120EVM Test Data

Figure 5-1 through Figure 5-9 present typical performance graphs for the TPS62120EVM. Actual performance data can be affected by measurement techniques and environmental variables; therefore, these curves are presented for reference and may differ from actual results obtained by some users.

5.1 Efficiency

Figure 5-1 shows the typical efficiency performance for the TPS62120EVM.

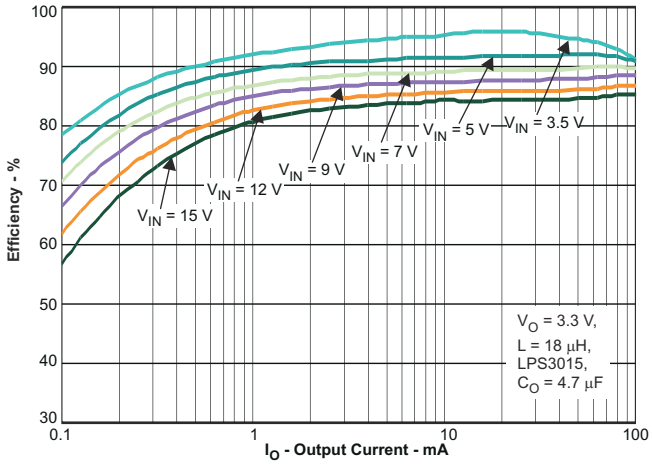


Figure 5-1. TPS62120EVM Efficiency versus Load Current

5.2 Start-Up

Figure 5-2 through Figure 5-5 show the typical start-up performance for different TPS62120EVM boards.

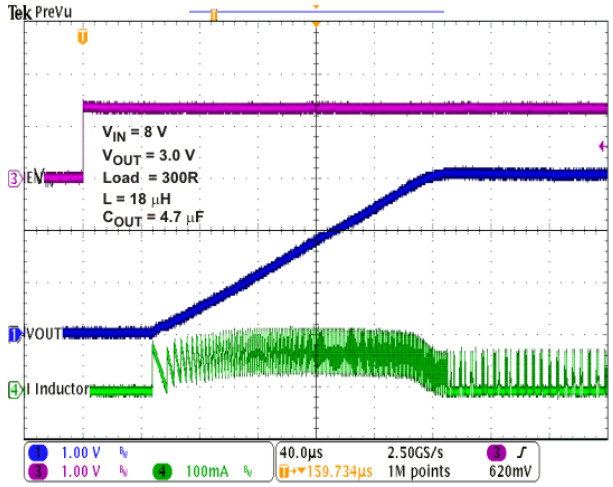


Figure 5-2. TPS62120EVM Startup into 300-Ω Load(V_{IN} = 8.0 V, V_{OUT} = 3.0 V)

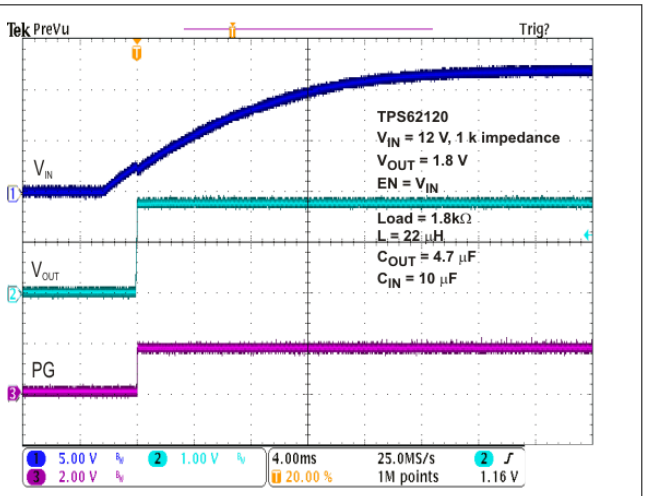


Figure 5-3. TPS62120EVM Start-Up from a High-Impedance Source(V_{IN} = 12.0 V, V_{OUT} = 3.0 V)

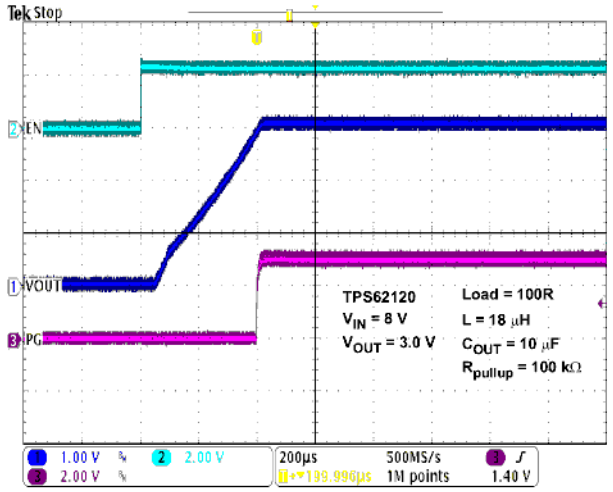


Figure 5-4. Power Good Output During Start-Up

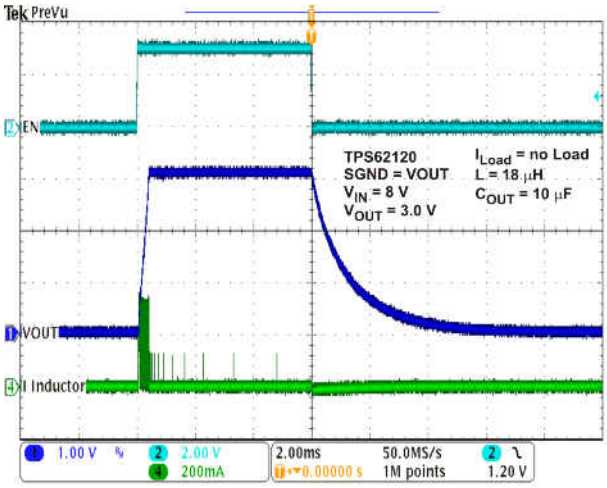


Figure 5-5. Output Discharge with SGND Pin Connected to VOUT

5.3 Load Transient Response

Figure 5-6 illustrates the load transient response for the TPS62120.

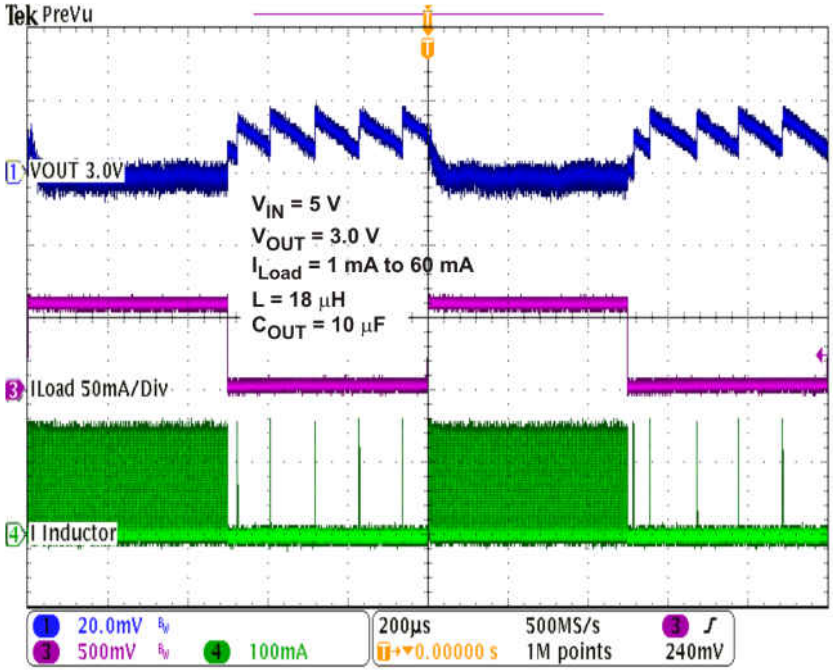


Figure 5-6. TPS62120 Load Transient Response(V_{IN} = 8.0 V, V_{OUT} = 1.8 V)

5.4 Typical Operation, 60 mA

Figure 5-7 illustrates the typical output voltage ripple for the TPS62120 with a 60-mA load.

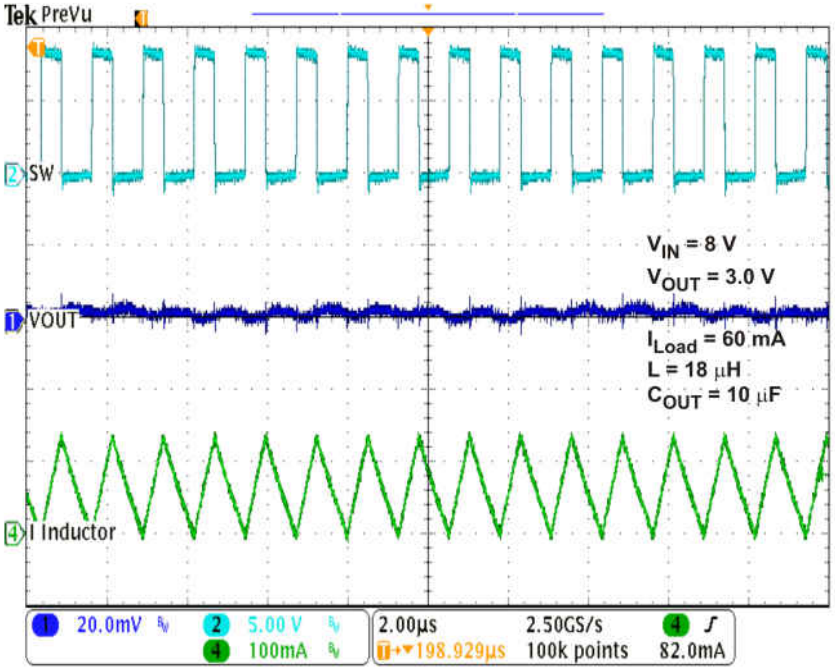


Figure 5-7. TPS62120EVM Output Ripple, 60-mA Load(V_{IN} = 8.0 V, V_{OUT} = 3.0 V)

5.5 Typical Operation, 10 mA

Figure 5-8 illustrates the typical output voltage ripple for the TPS62120 with a 10-mA load.

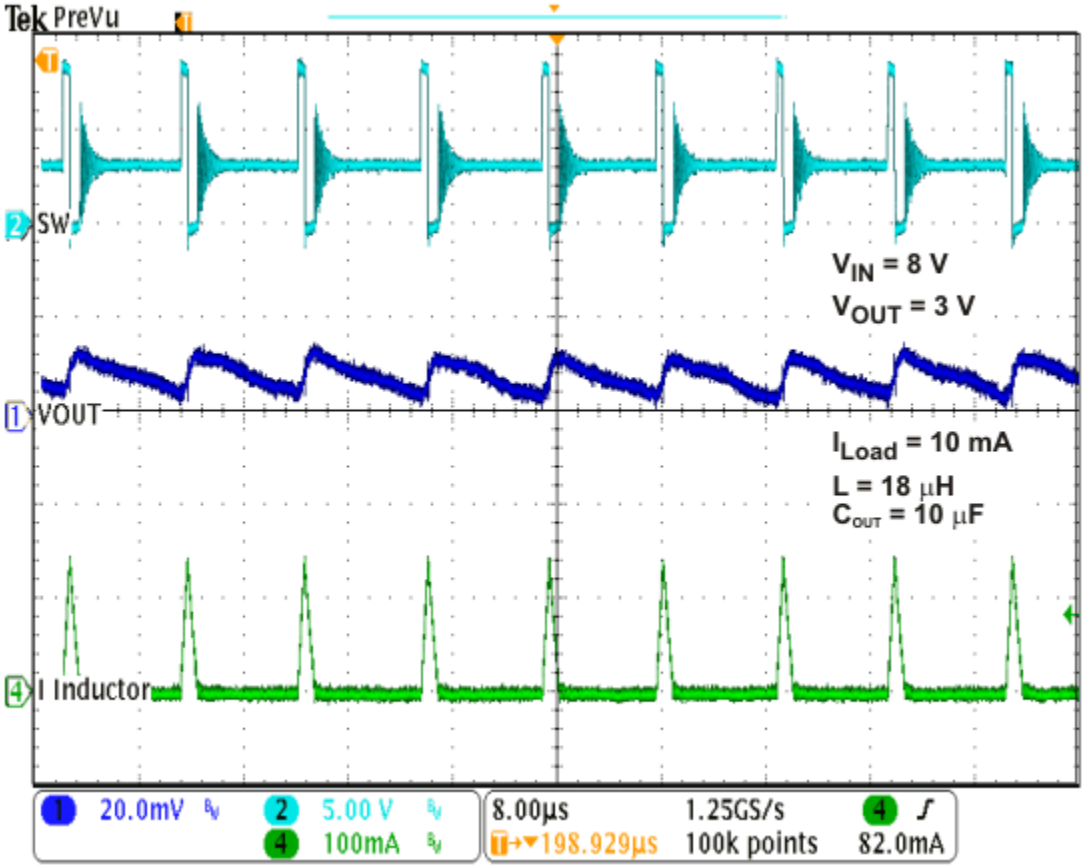


Figure 5-8. TPS62120EVM Output Ripple, 10-mA Load(V_{IN} = 8.0 V, V_{OUT} = 3.0 V)

5.6 Current Limit Operation

Figure 5-9 shows the current limit operation of the TPS62120.

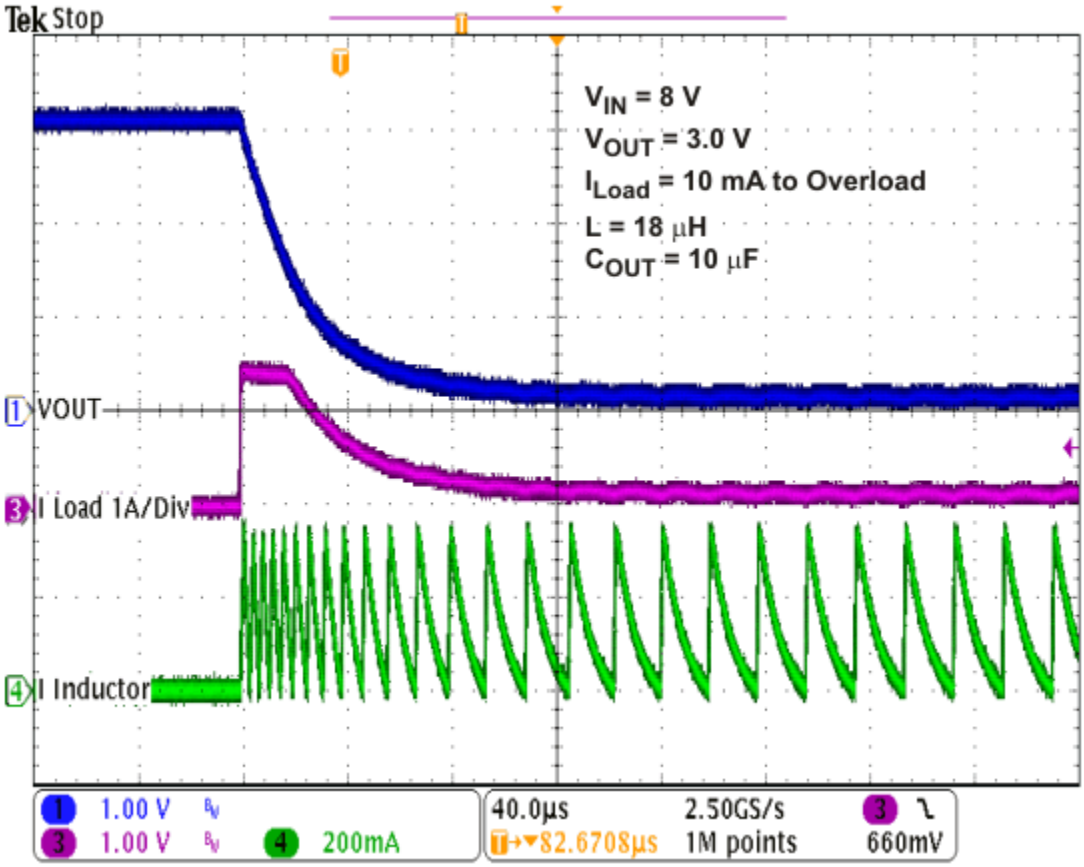


Figure 5-9. Current Limit Operation

6 TPS62120EVM Assembly Drawings and Layout

Figure 6-1 through Figure 6-3 show the design of the show the design of the TPS62120EVM-640 printed circuit board. The EVM has been designed using a four-layer, 1-ounce copper-clad PCB.

Note

Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing TPS62120EVM-640 PCBs.

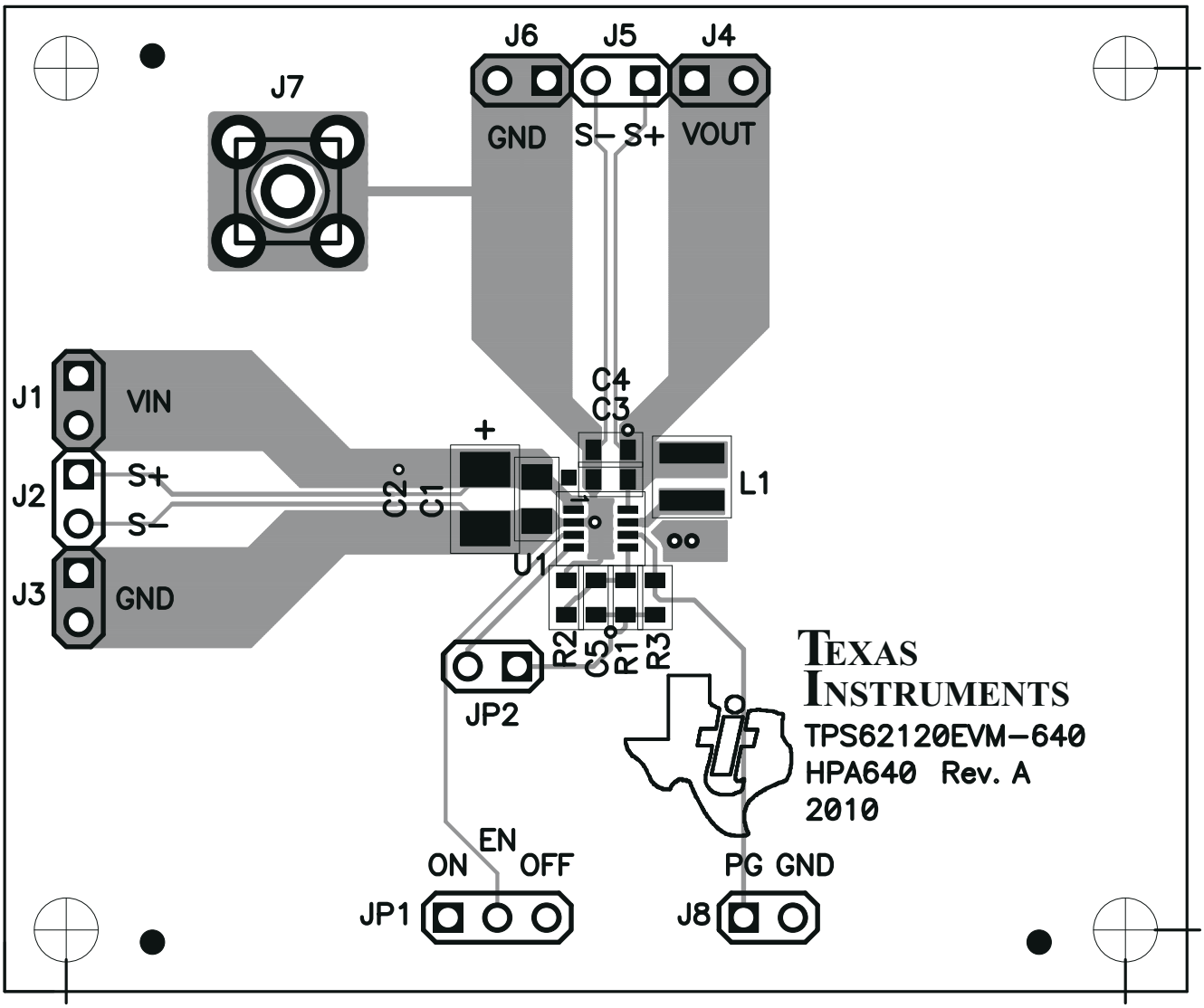


Figure 6-1. TPS62120EVM Component Placement (Top View)

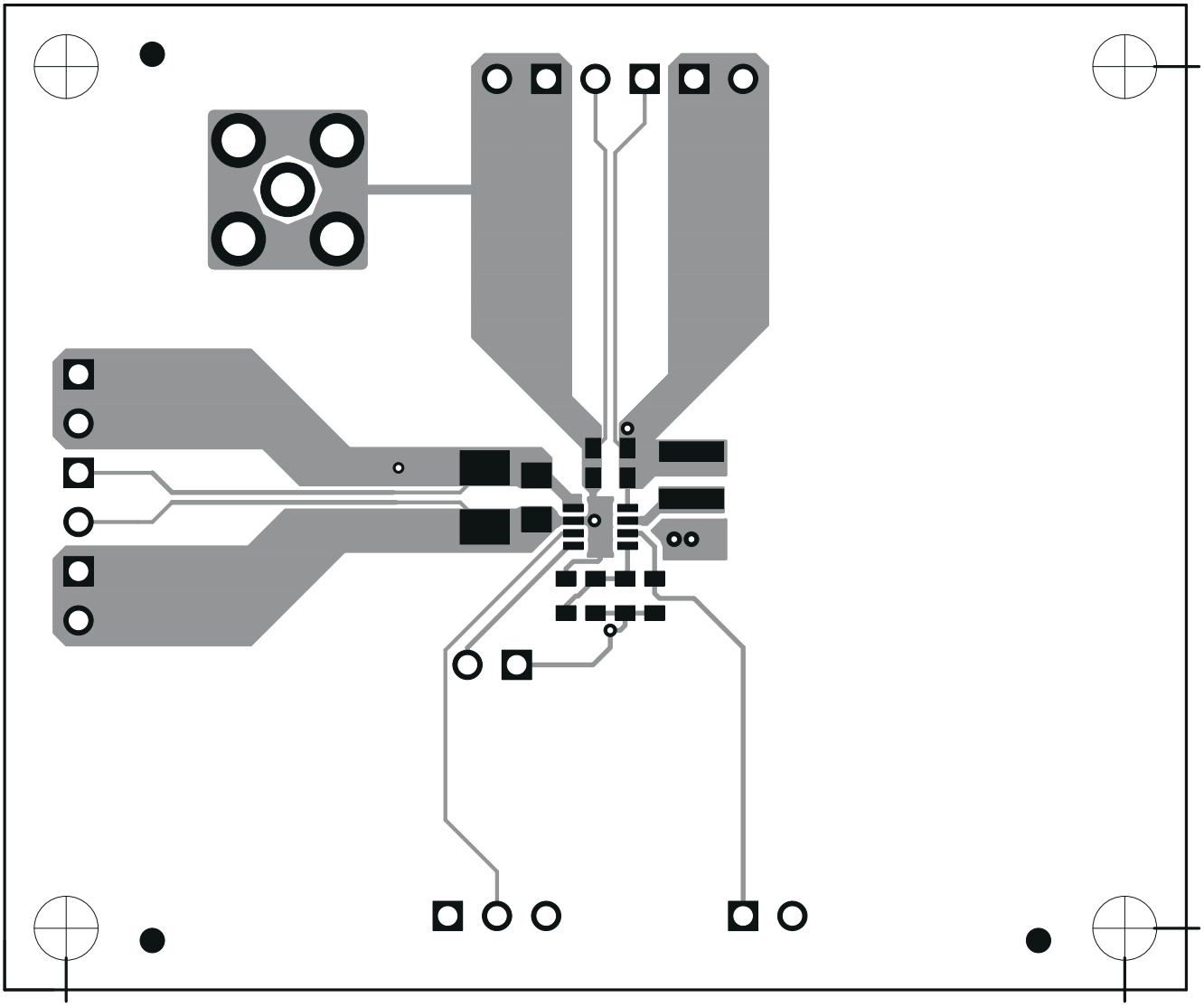


Figure 6-2. TPS62120EVM Top-Side Copper (Top View)

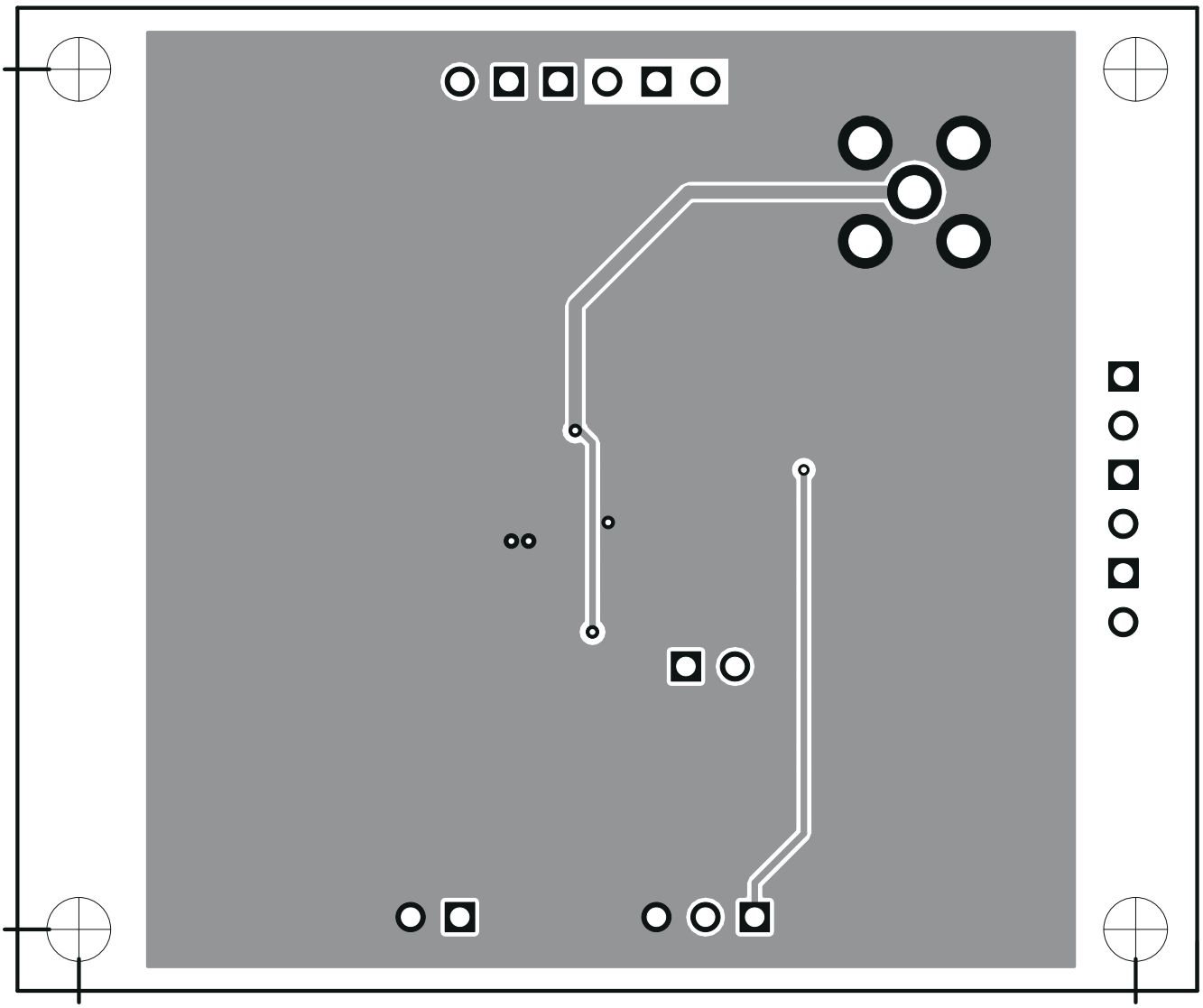


Figure 6-3. TPS62120EVM Bottom-Side Copper (Bottom View)

7 Bill of Materials

Table 7-1 lists the bill of materials for the TPS62120EVM.

Table 7-1. TPS62120EVM-640 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	4.7 µF	Capacitor, Ceramic, 25 V, X5R, 20%	0805	GRM21BR61E475MA12L	muRata
1	C3	4.7 µF	Capacitor, Ceramic, Low Inductance, 6.3 V, X5R, 20%	0603	GRM188R60J475ME19D	muRata
1	C5	15 pF	Capacitor, Ceramic, 50 V, C0G-NP0, 5%	0603	Std	Std
1	L1	18 µH	Inductor, SMT, 0.56 A, 750 mΩ	0.118 x 0.118 inch	LPS3015-183ML	Coilcraft
1	R1	301k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	243k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	10.0 kΩ	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	U1	TPS62120DRV	IC, 15-V, 75-mA High-Efficiency Buck Converter with Snooze Mode	SSOP	TPS62120DCN	TI

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2010) to Revision A (June 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 2
- Updated user's guide title..... 2

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