User's Guide
SLVU424–December 2010

TLV62065EVM-719

This user's guide describes the characteristics, operation, and use of the TLV62065 evaluation module (EVM). The TLV62065EVM-719 is a fully assembled and tested platform for evaluating the performance of the TLV62065 2.0-A step-down converter. This document includes schematic diagrams, printed circuit board (PCB) layout, bill of materials, and test data. Throughout this document, the abbreviations *EVM*, *TLV62065EVM*, and the term *evaluation module* are synonymous with the TLV62065EVM-719 unless otherwise noted.

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1 Introduction

The TLV62065EVM-719 is a fully assembled and tested PCB for evaluating the TLV62065 1.6-A step-down converter.

1.1 Features

- Input voltage range: 2.9 V to 5.5 V
- Adjustable output voltage: 0.8 V to VIN
- Up to 2.0-A output current
- Power Save mode / 3-MHz fixed PWM mode

1.2 TLV62065 Applications

The TLV62065 step-down converters are ideal for these applications:

- POL
- Notebooks, pocket personal computers
- Portable media players
- DSP supply

2 TLV62065EVM Schematic

Figure 1 shows the TLV62065EVM schematic.

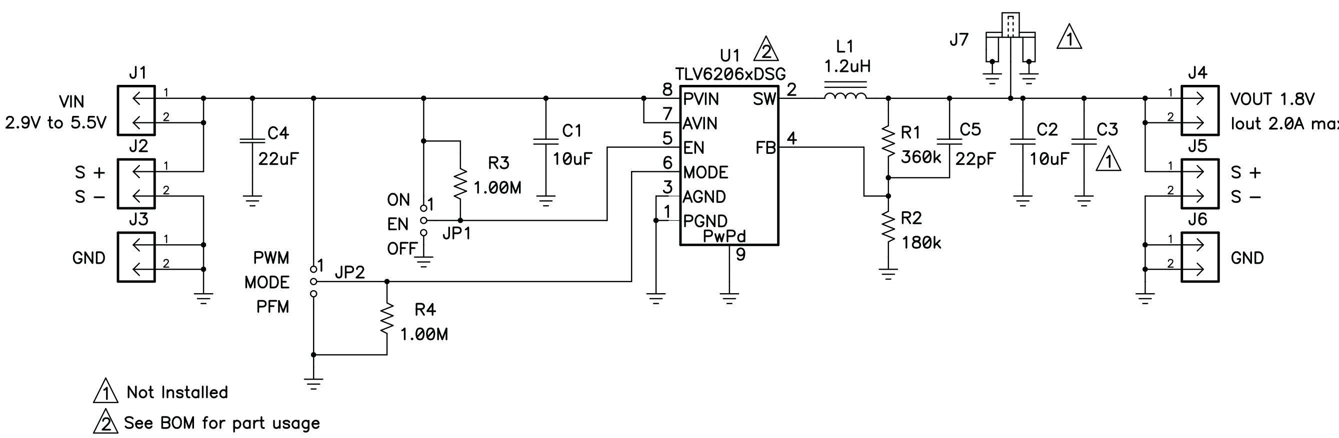


Figure 1. TLV62065EVM Schematic

NOTE: Figure 1 is provided for reference only. See the bill of materials (Table 1) for specific component values.

3 Connector and Test Point Descriptions

3.1 *Enable Jumpers/Switches: TLV62065EVM*

3.1.1 J1, VIN

This header is the positive connection to the input power supply. The power supply must be connected between J1 and J3 (GND). Twist the leads to the input supply, and keep them as short as possible. The input voltage must be between 2.9 V and 5.5 V.

3.1.2 J2, S+/S–

J2 S+/S– are the sense connections for the input of the converter. Connect a voltmeter, or the sense connection of a power supply or oscilloscope, to this header.

3.1.3 J3, GND

This header is the return connection to the input power supply. Connect the power supply between J3 and J1 (VIN). Twist the leads to the input supply, and keep them as short as possible. The input voltage must be between 2.9 V and 5.5 V.

3.1.4 J4, VOUT

This header is the positive output of the step-down converter. The output voltage of the TLV62065 is adjustable with feedback resistors R1 and R2. On the EVM, the output voltage is set to 1.8 V by default.

NOTE: A feed-forward capacitor (C5) is required. Refer to the TLV62065 data sheet (SLVSAC4) for detailed information.

3.1.5 J5, S+/S–

J5 S+/S– are the sense connections for the output of the converter. Connect a voltmeter, or the sense connection of an electronic load or oscilloscope, to this header.

3.1.6 J6, GND

J6 is the return connection of the converter. A load can be connected between J6 and J4 (V_{OUT}). The converter is capable of carrying a load current up to 2.0 A.

3.1.7 JP1, EN

This jumper enables/disables the TLV62065 on the EVM. Shorting jumper JP1 between the center pin and *On* turns on the unit. Shorting the jumper between center pin and *Off* turns off the unit. A 1-MΩ pullup resistor is connected between VIN and EN. Removing jumper JP1 turns on the converter.

3.1.8 JP2, MODE

This jumper enables/disables the power-saving mode under light loads. Shorting jumper JP2 between the center pin and PWM disables the power-saving mode. If the power-save mode is disabled, the converter operates in forced PWM mode over the entire load current range. Shorting the jumper between the center pin and PFM enables the power-saving mode. The device operates in power-saving mode under light load conditions. See the TLV62065 data sheet (SLVSAC4) for a detailed description of this configuration. A 1-MΩ pulldown resistor is connected between GND and MODE. By removing JP2, the converter operates in power-saving mode under light-load conditions.

3.1.9 J7, VOUT (SMA)

This SMA connector is connected to the output voltage of the TLV62065. It can be used to easily analyze the noise spectrum of the output voltage with a spectrum analyzer. By default, J7 is not assembled on the EVM.

4 Test Configuration

4.1 Hardware Setup

Figure 2 illustrates a typical hardware test configuration.

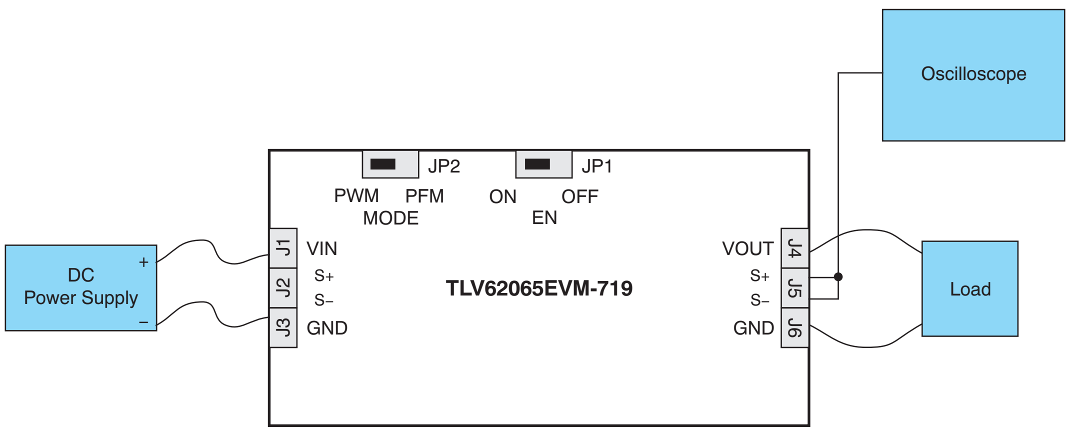


Figure 2. Hardware Board Connection

4.2 Testing Procedure

Follow these procedures when configuring the EVM for testing.

CAUTION

Many of the components on the TLV62065EVM-719 are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD-handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap, bootstraps, or mats at an approved ESD workstation. An electrostatic smock and safety glasses also are recommended.

1. Connect a dc power supply between J1 and J3 on the TLV62065EVM. Note that the input voltage must be between 2.9 V and 5.5 V. Keep the wires from the input power supply to the EVM as short as possible and twisted.
2. Connect a dc voltmeter or oscilloscope to J5, the output sense connection of the EVM.
3. A load can be connected between J4 and J6 on the TLV62065EVM.
4. To enable the converter, connect the shorting bar on JP1 between EN and ON located on the TLV62065EVM.
5. The TLV62065EVM has a feature to allow the user to switch between Power-Save mode under light loads and forced PWM mode; this feature is enabled or disabled with jumper JP2.

5 TLV62065EVM Test Data

Figure 3 through Figure 15 present typical performance curves for the TLV62065EVM. Actual performance data can be affected by measurement techniques and environmental variables; therefore, these curves are presented for reference and may differ from actual results obtained by some users.

5.1 Efficiency

Figure 3 and Figure 4 show the typical efficiency performance for the TLV62065EVM.

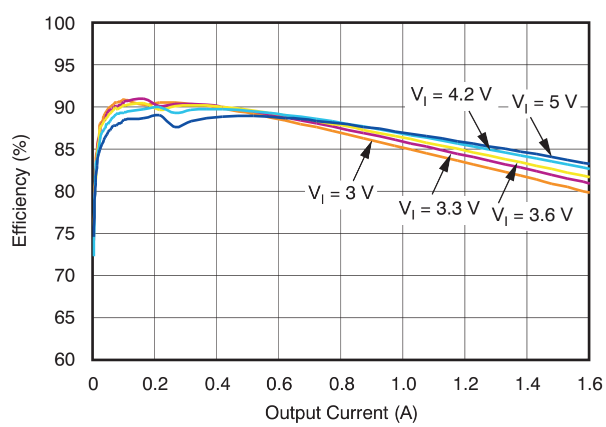


Figure 3. TLV62065 Efficiency vs Load Current, PFM Mode

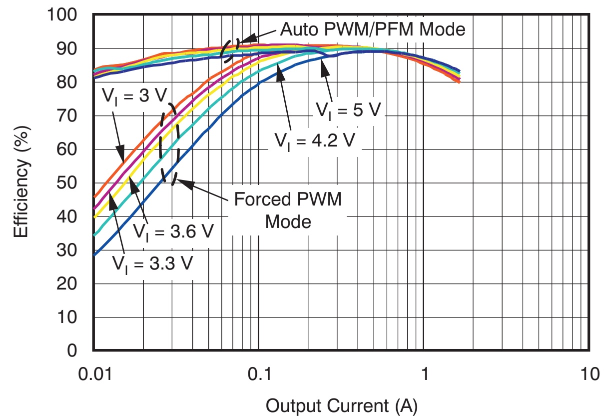
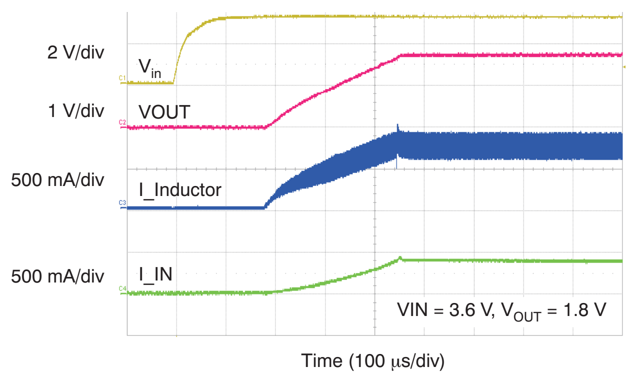


Figure 4. TLV62065 Efficiency vs Load Current

5.2 *Start-up*

Figure 5 and Figure 6 show the typical start-up performance for the TLV62065EVM.



Conditions: VIN = 3.6 V, V_{OUT} = 1.8 V

Figure 5. TLV62065 Start-up Into 2.2-Ω Load

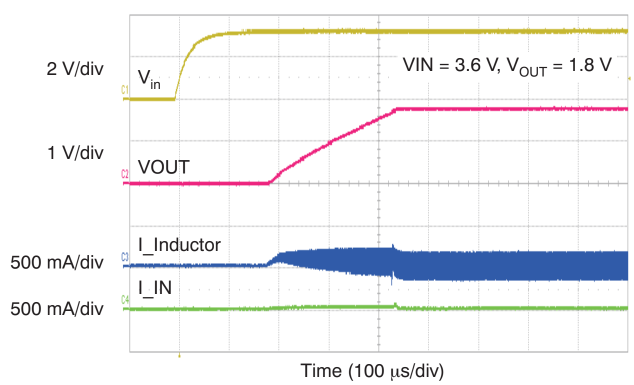
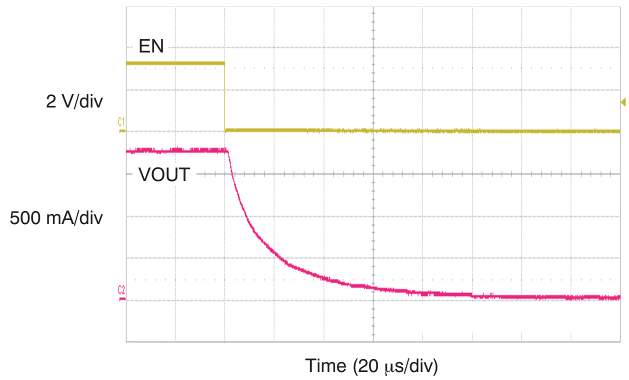


Figure 6. TLV62065 Start-up With No Load

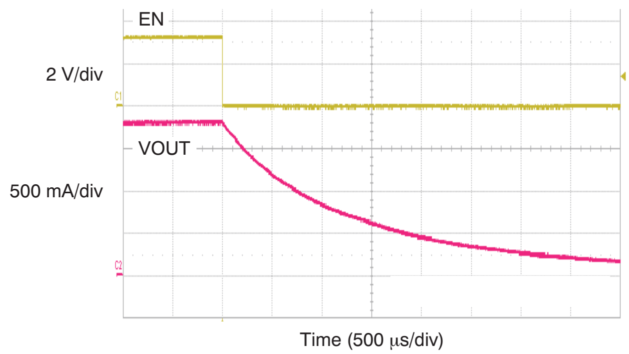
5.3 Shutdown

Figure 7 and Figure 8 illustrate the typical shutdown behavior for the TLV62065EVM.



Conditions: VIN = 3.6 V, V_{OUT} = 1.8 V

Figure 7. TLV62065 Shutdown Into 2.2-Ω Load



Conditions: VIN = 3.6 V, V_{OUT} = 1.8 V

Figure 8. TLV62065 Shutdown With No Load

5.4 Output Voltage Ripple

Figure 9 and Figure 10 show the typical output voltage ripple for the TLV62065EVM in PFM and PWM modes, respectively.

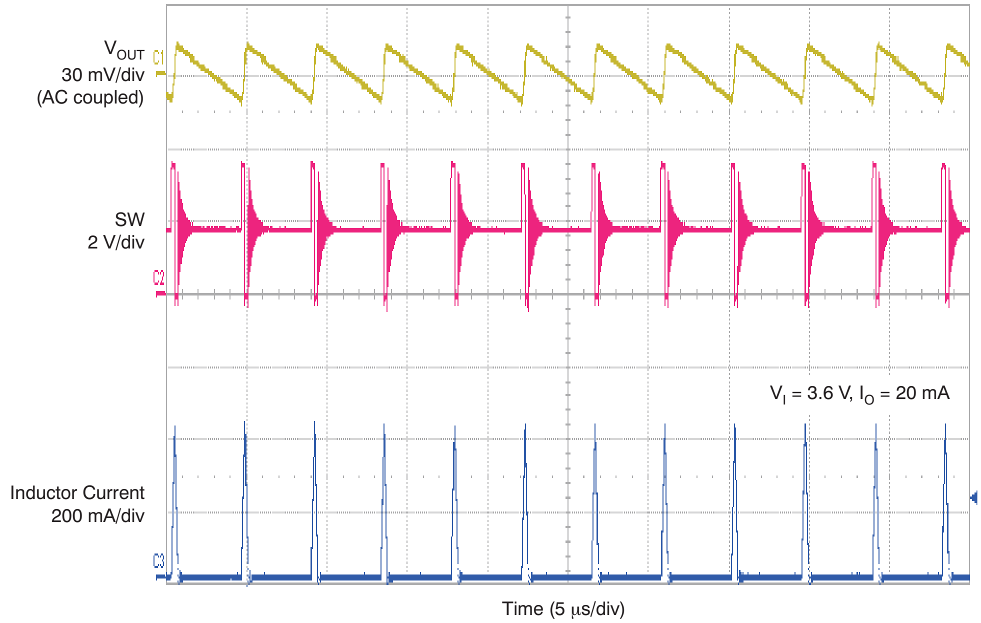


Figure 9. TLV62065 Output Voltage Ripple, PFM Mode

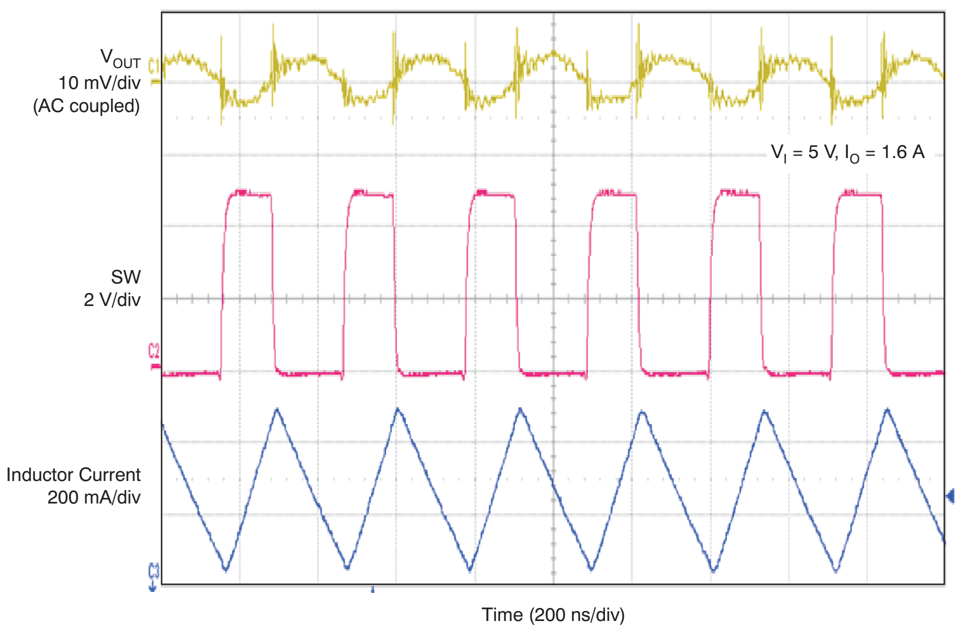


Figure 10. TLV62065 Output Voltage Ripple, PWM Mode

5.5 Input Voltage Ripple

Figure 11 shows the typical input voltage ripple for the TLV62065EVM at 3.6 V in and 1.6 A load.

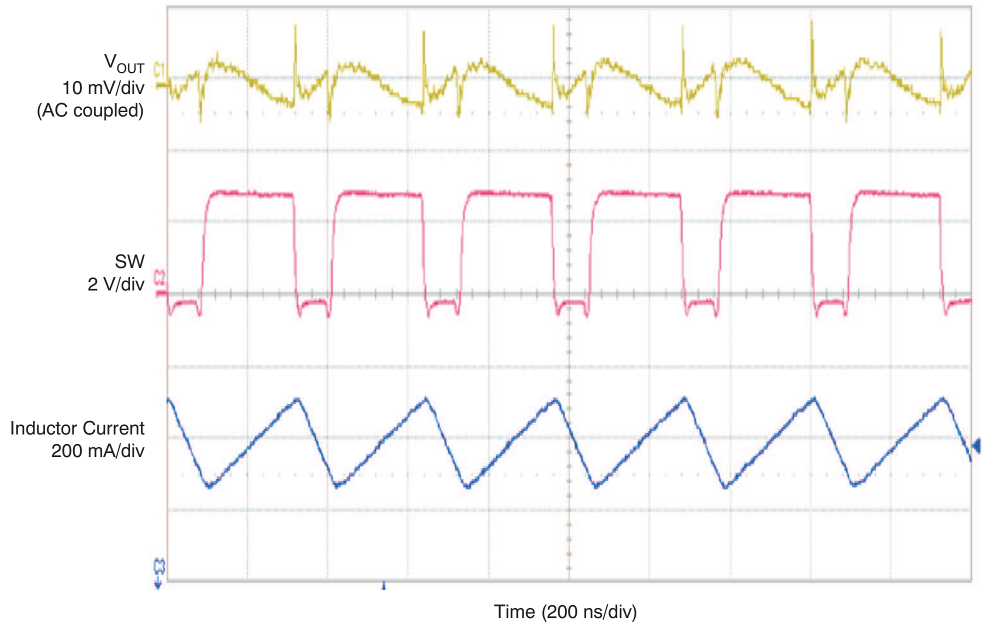
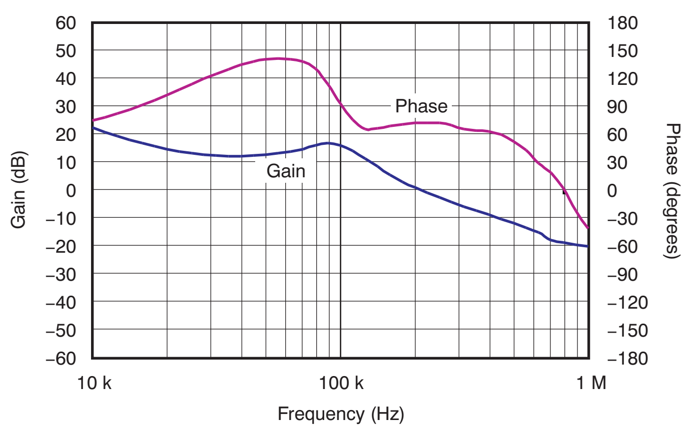


Figure 11. TLV62065 Input Voltage Ripple

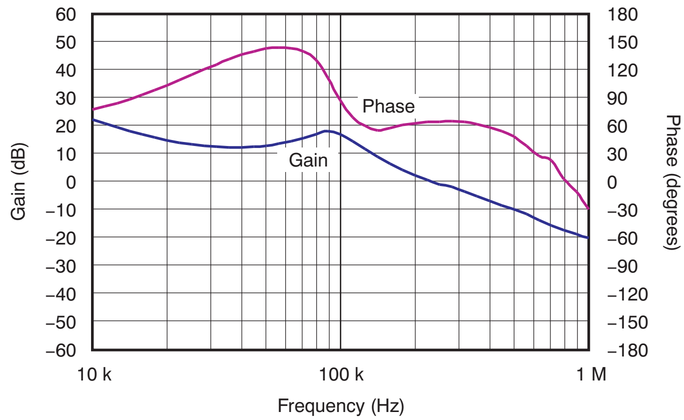
5.6 Control Loop Bode Diagrams

Figure 12 and Figure 13 illustrate typical TLV62065EVM gain and phase performance versus frequency at VIN = 3.6 V and 5 V, respectively.



Conditions: VIN = 3.6 V, VOUT = 1.8 V, I_{OUT} = 1.6 A; bandwidth: 213 kHz, phase margin: 73°

Figure 12. TLV62065 Gain and Phase vs Frequency



Conditions: VIN = 5 V, VOUT = 1.8 V, I_{OUT} = 1.6 A; bandwidth: 241 kHz, phase margin: 66°

Figure 13. TLV62065 Gain and Phase vs Frequency

5.7 *Transient Performance*

Figure 14 and Figure 15 show the load transient response of the TLV62065EVM in PFM and PWM modes, respectively.

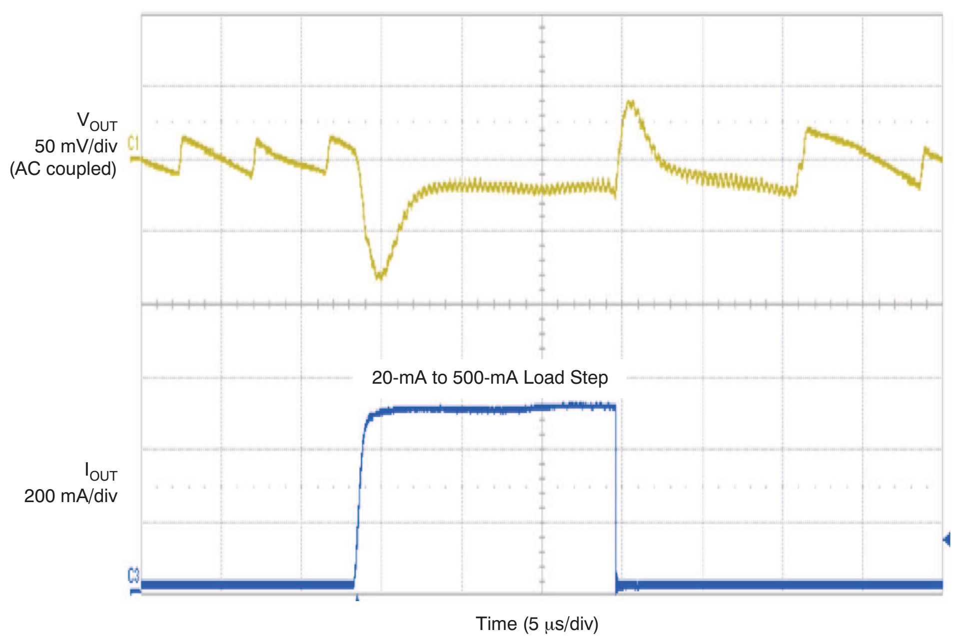


Figure 14. TLV62065 Transient Response, PFM Mode

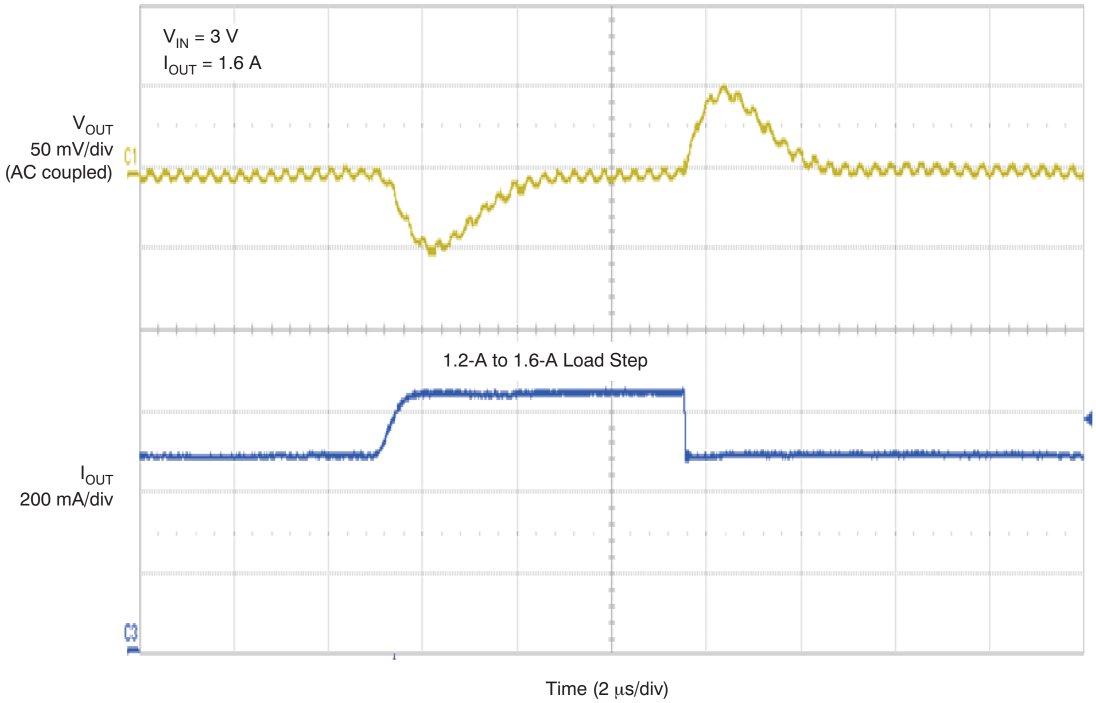


Figure 15. TLV62065 Transient Response, PWM Mode

6 TLV62065EVM Assembly Drawings and Layout

Figure 16 through Figure 20 show the design of the TLV62065EVM-719 printed circuit board. This EVM has been designed using a four-layer, 1-ounce, copper-clad PCB (1.8 in × 1.5 in, or 4.57 cm × 3.81 cm) with all components in an active area on the top side of the board. All active traces are routed on the top and bottom layers to allow the user to easily view, probe, and evaluate the TLV62065 device in a practical, double-sided application environment. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space-constrained systems.

NOTE: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing TLV62065EVM-719 PCBs.

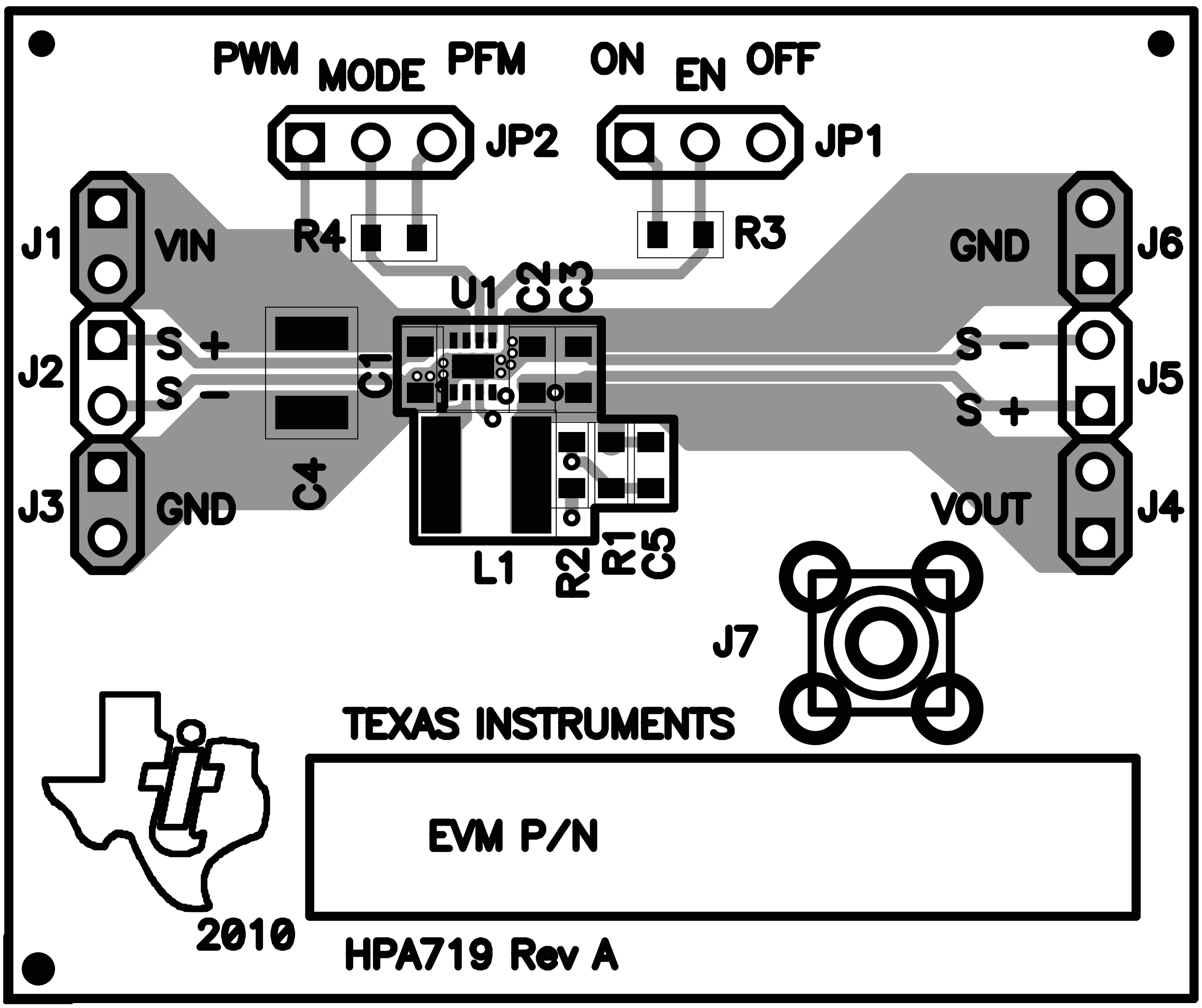


Figure 16. TLV62065EVM Component Placement, Top View

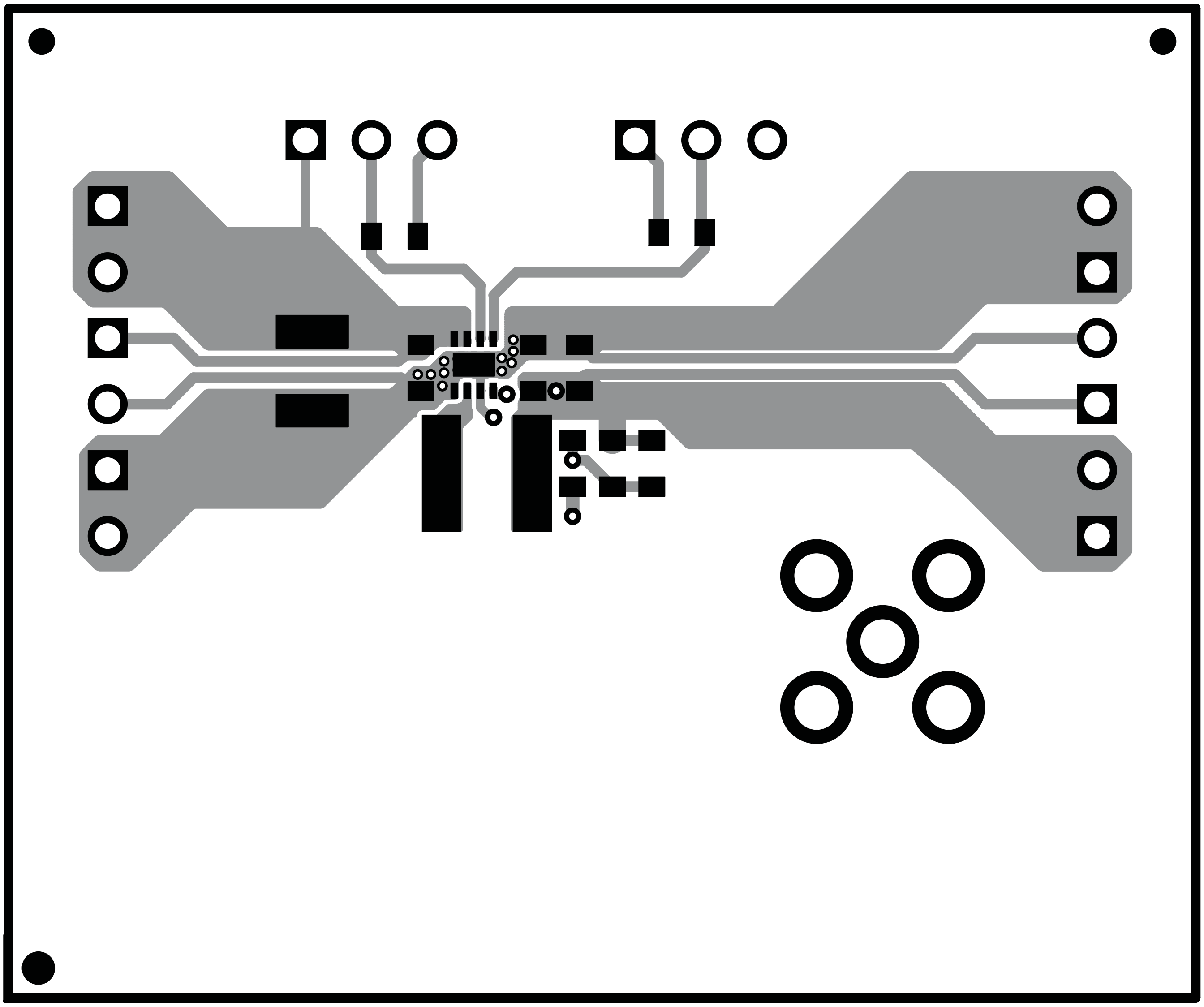


Figure 17. TLV62065EVM Top-Side Copper, Top View

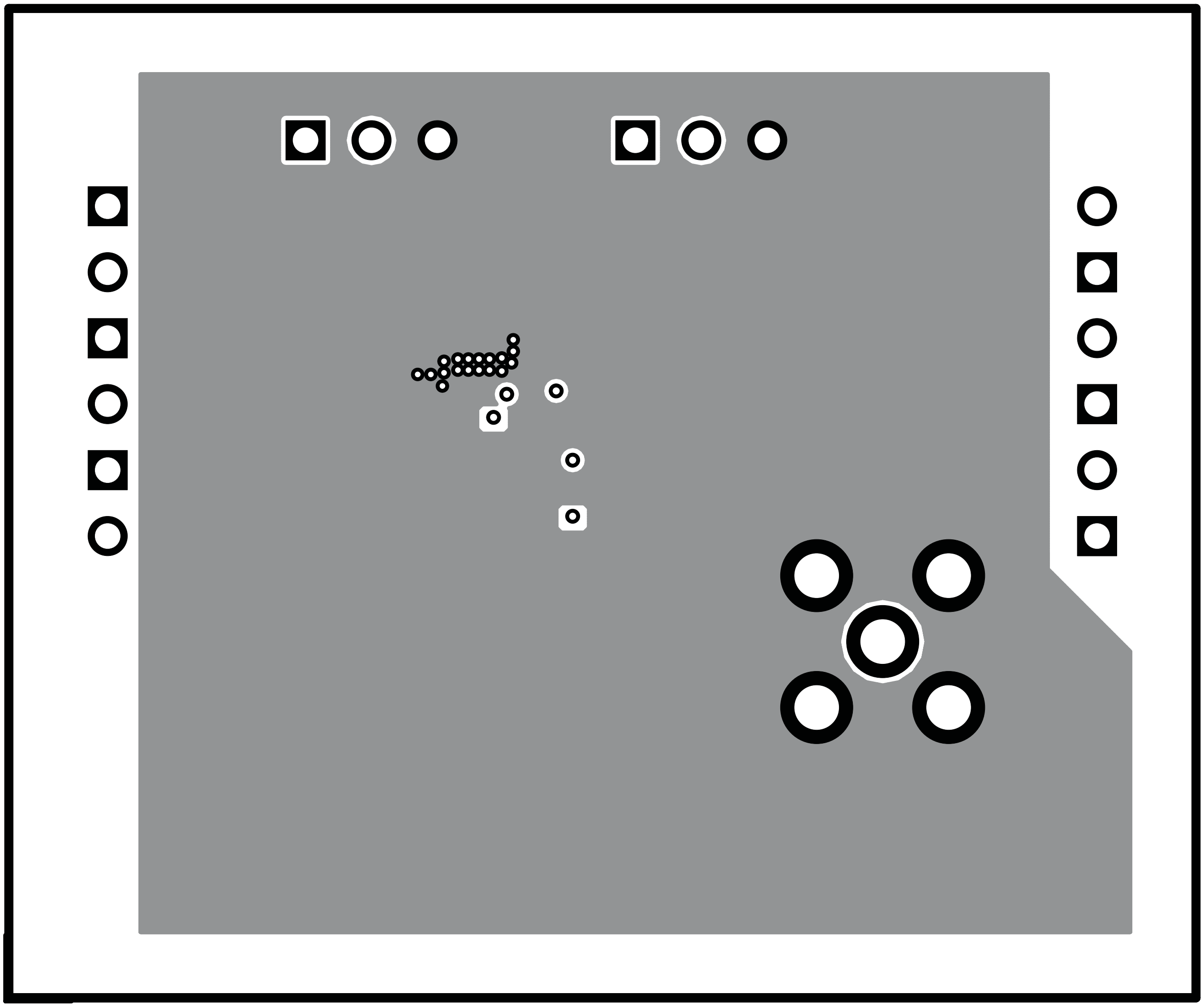


Figure 18. TLV62065EVM Internal Layer 1, X-Ray View From Top

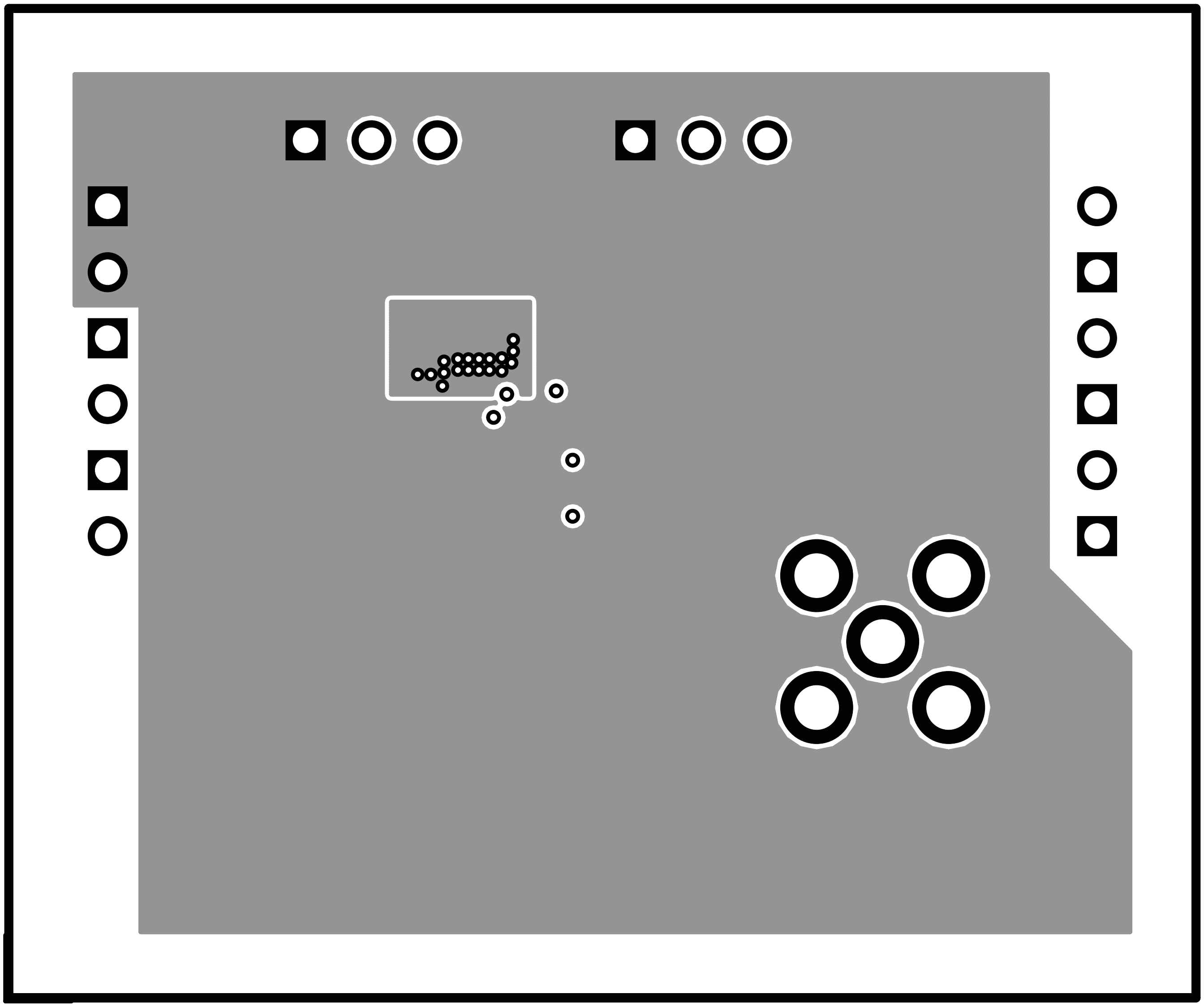


Figure 19. TLV62065EVM Internal Layer 2, X-Ray View From Top

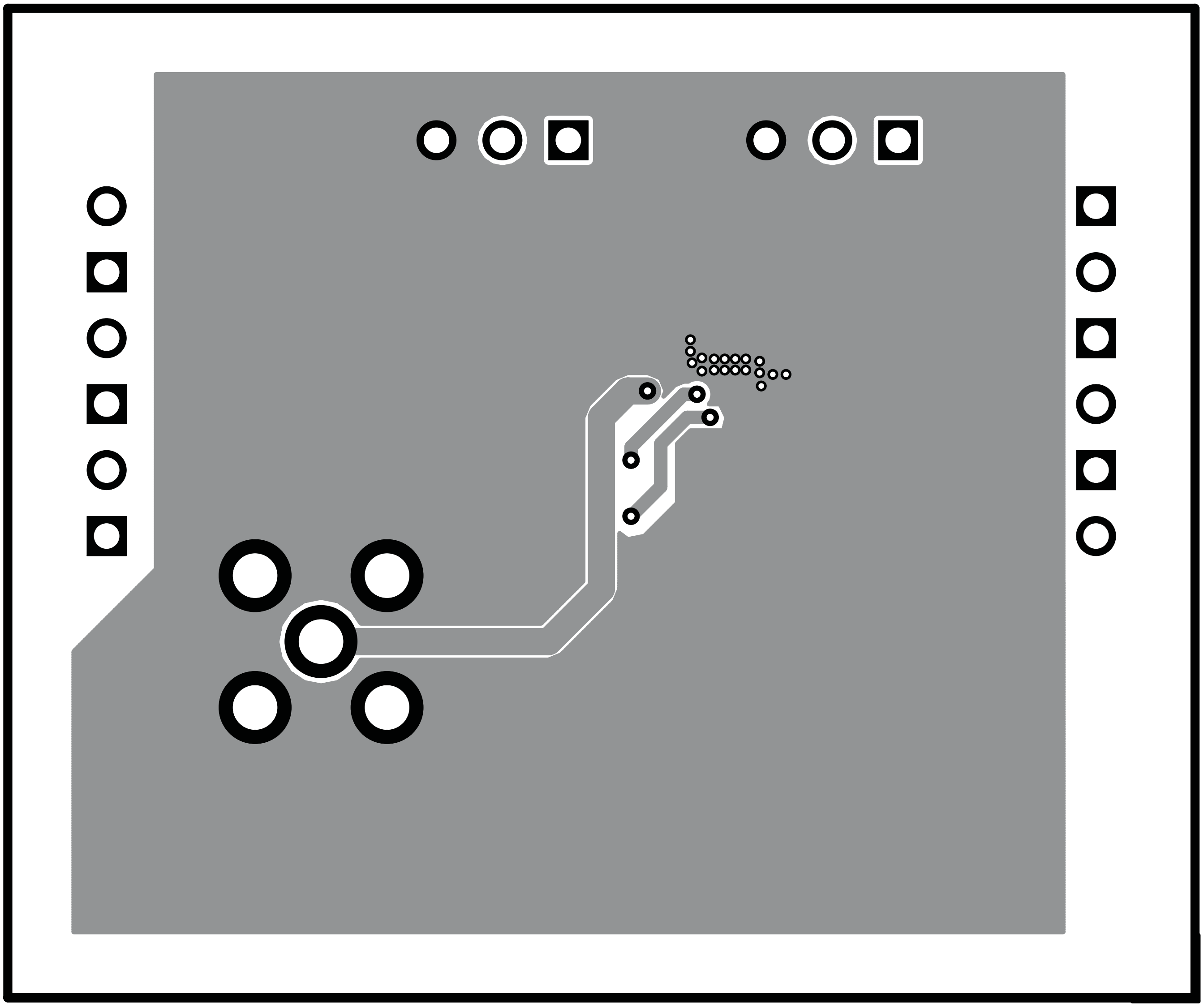


Figure 20. TLV62065EVM Bottom-Side Copper, Bottom View

7 Bill of Materials

Table 1 lists the bill of materials for the TLV62065EVM.

Table 1. TLV62065EVM Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
2	C1, C2	10 µF	Capacitor, ceramic, 6.3 V, X5R, 20%	0603	GRM188R60J106ME47D	muRata
0	C3	Open	Capacitor, ceramic, 6.3 V, X5R, 20%	0603	Std	Std
1	C4	22 µF	Capacitor, ceramic, 10 V, X5R, 20%	1210	GRM32ER71A226K	muRata
1	C5	22 pF	Capacitor, ceramic, 50 V, NPO, 5%	0603	Std	Std
0	J7	Open	Connector, SMA , Straight, PC mount	0.210 in^2	901-144-8RFX	AMP
1	L1	1.2 µH	Inductor, SMT, 3.1 A, ±30%	4x4 mm	NRG4026T-1R2N	Taiyo Yuden
1	R1	360 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	R2	180 kΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
2	R3, R4	1.00 MΩ	Resistor, chip, 1/16W, 1%	0603	Std	Std
1	U1	TLV62065DSG	IC, step-down converter, 3 MHz, 1.6 A, low-cost	SON-8	TLV62065DSG	TI

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 2.9 V to 5.5 V and the output voltage range of 0.8 V to 5.5 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +60°C. The EVM is designed to operate properly with certain components above +60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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