User's Guide

TPS54429E Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains background information for the TPS54429E as well as support documentation for the TPS54429EEVM-608 evaluation module. Also included are the performance specifications, schematic and the bill of materials for the TPS54429EEVM-608.

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Trademarks

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1 Introduction

The TPS54429E is a single, adaptive on-time D-CAP2™ mode synchronous buck converter requiring a very low external component count. The D-CAP2™ control circuit is optimized for low-ESR output capacitors such as POSCAP, SP-CAP or ceramic types and features fast transient response with no external compensation. The switching frequency is internally set at a nominal 700 kHz. The high-side and low-side switching MOSFETs are incorporated inside the TPS54429E package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFETs allows the TPS54429E to achieve high efficiencies and helps keep the junction temperature low at high output currents. The TPS54429E also has an auto-skip Eco-mode™ to enable higher efficiency at light loads. The TPS54429E dc/dc synchronous converter is designed to provide up to a 4.5-A output from an input voltage source of 7 V to 18 V. The output voltage range is from 0.76-V to 5.5-V voltage and output current range for the evaluation module are given in Table 1-1.

Table 1-1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Voltage and Current Range
TPS54429EEVM-608	VIN = 7 V to 18 V	VOUT = 1.05 V, 0 A to 4.5 A

2 Performance Specification Summary

A summary of the TPS54429EEVM-608 performance specifications is provided in Table 2-1. Specifications are given for an input voltage of VIN = 12 V and an output voltage of 1.05 V, unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

Table 2-1. TPS54429E EVM and Performance Specifications Summary

Specifications		Test Conditions	Min	Typ	Max	Unit
Input voltage range (VIN)			7	12	18	V
CH1	Output voltage			1.05		V
	Operating frequency	VIN = 12 V, I_O = 1 A		700		kHz
	Output current range		0		4.5	A
	Overcurrent limit	VIN = 12 V, L_O = 1.5 µH		5.9		A
	Output ripple voltage	VIN = 12 V, I_O = 4 A		10		mV_{PP}

3 Modifications

These evaluation modules are designed to provide access to the feature of the TPS54429E. Some modification can be made to this module.

3.1 Output Voltage Setpoint

To change the output voltage of the EVMs, it is necessary to change the value of resistor R1. Changing the value of R1 can change the output voltage above 0.765 V. The value of R1 for a specific output voltage can be calculated using Equation 1 and Equation 2.

For output voltage from 0.76 V to 2.5 V:

$$V_O = 0.765 \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

For output voltage over 2.5 V:

$$V_O = (0.763 + 0.0017 \times V_O) \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

Table 3-1 lists the R1 value for some common output voltages. For higher output voltages of 1.8 V or above, a feedforward capacitor (C2) may be required to improve phase margin and is recommended for auto skip Eco-mode™ stability. Pads for this component (C2) are provided on the printed-circuit board. Note that the values given in Table 3-1 are standard values and not the exact value calculated using Table 3-1.

Table 3-1. Output Voltages

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	C2 (pF)	L1 (µH)
1.0	6.81	22.1		1.5
1.05	8.25	22.1		1.5
1.2	12.7	22.1		1.5
1.5	23.2	22.1		1.5
1.8	30.1	22.1	10 - 22	2.2
2.5	49.9	22.1	10 - 22	2.2
3.3	73.2	22.1	10 - 22	2.2
5.0	121	22.1	10 - 22	3.3

4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54429EEVM-608. The section also includes test results typical for the evaluation modules and efficiency, output load regulation, output line regulation, load transient response, output voltage ripple, input voltage ripple, start-up and switching frequency.

4.1 Input / Output Connections

The TPS54429EEVM-608 is provided with input/output connectors and test points as shown in Table 4-1. A power supply capable of supplying 3 A must be connected to J1 through a pair of 20 AWG wires. The load must be connected to J2 through a pair of 20 AWG wires. The maximum load current capability is 4.5 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP7 is used to monitor the output voltage with TP8 as the ground reference.

Table 4-1. Connection and Test Points

Reference Designator	Function
J1	V_{IN} (see Table 1-1 for V_{IN} range)
J2	V_{OUT}, 1.05 V at 4.5 A maximum
JP1	EN control. Connect EN to OFF to disable, connect EN to ON to enable.
TP1	V_{IN} test point at V_{IN} connector
TP2	GND test point at V_{IN}
TP3	EN test point
TP4	Analog ground test point
TP5	Switch node test point
TP6	Power-good test point
TP7	Output voltage test point
TP8	Ground test point at output connector

4.2 Start-Up Procedure

1. Make sure the jumper at JP1 (Enable control) is set from EN to OFF.
2. Apply appropriate VIN voltage to VIN and PGND terminals at J1.
3. Move the jumper at JP1 (Enable control) to cover EN and ON. The EVM enables the output voltage.

4.3 Efficiency

Figure 4-1 shows the efficiency for the TPS54429EEVM-608 at an ambient temperature of 25°C. The input voltage is 12 V.

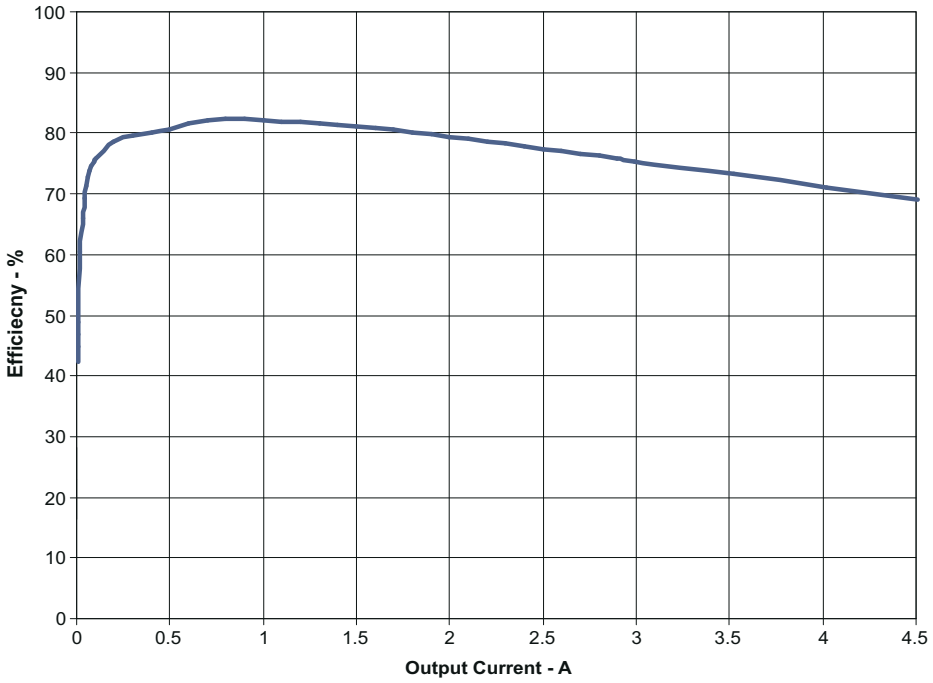

Figure 4-1. TPS54429EEVM-608 Efficiency

4.4 Light Load Efficiency

Figure 4-2 shows the efficiency at light loads for the TPS54429EEVM-608 at an ambient temperature of 25°C. The input voltage is 12 V.

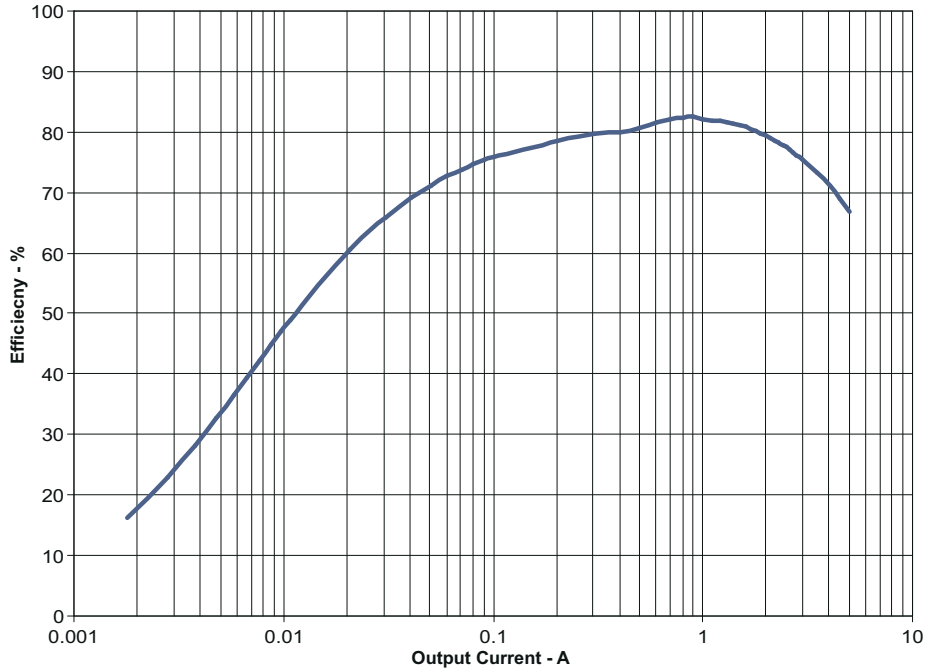

Figure 4-2. TPS54429EEVM-608 Light Load Efficiency

4.5 Load Regulation

The load regulation for the TPS54429EEVM-608 is shown Figure 4-3. The input voltage is 12 V.

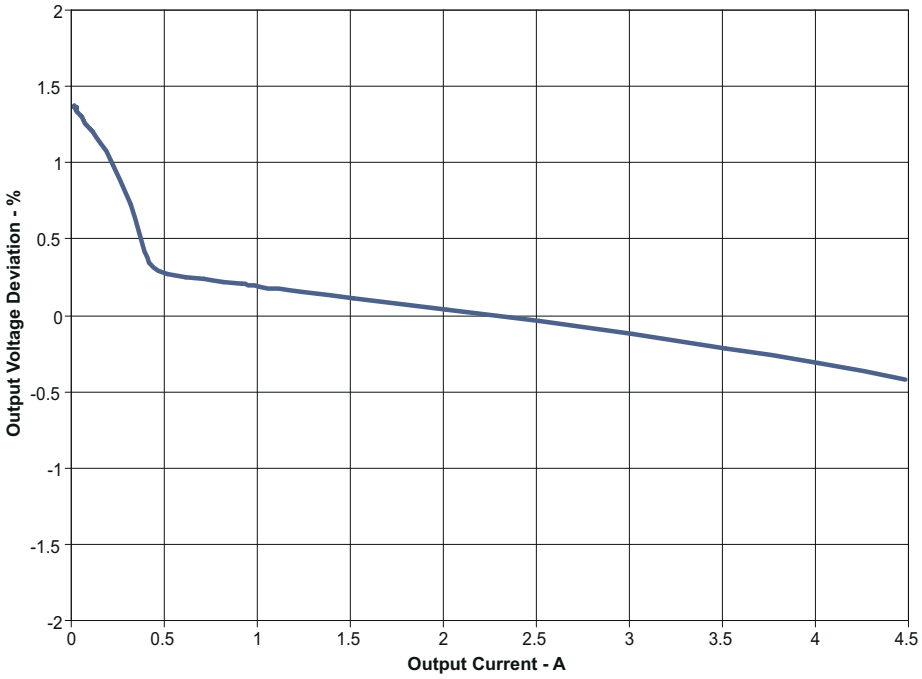

Figure 4-3. TPS54429EEVM-608 Load Regulation

4.6 Line Regulation

The line regulation for the TPS54429EEVM-608 is shown Figure 4-4. the load current is 2.25 A.

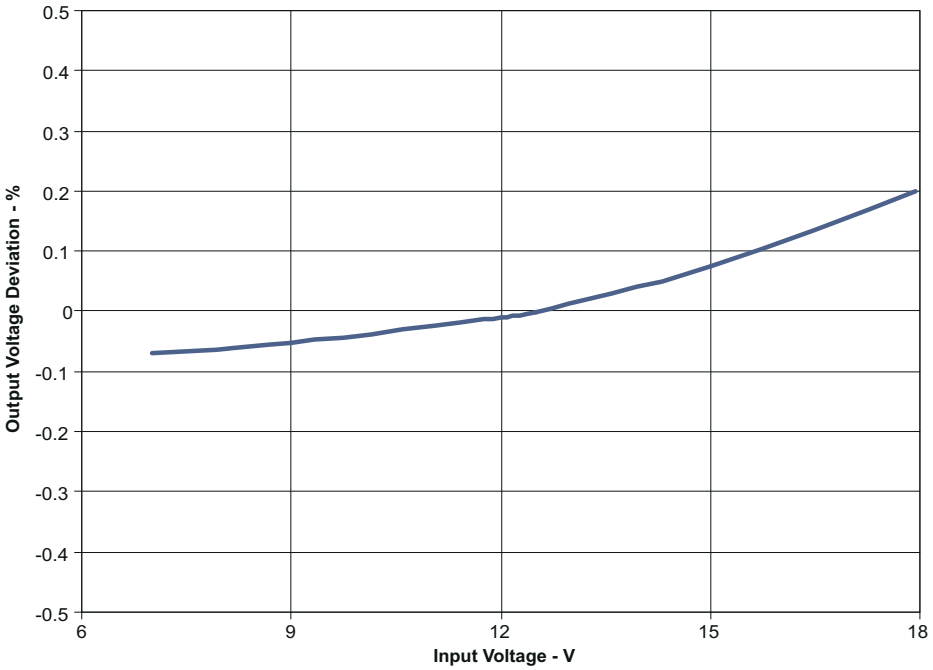

Figure 4-4. TPS54429EEVM-608 Line Regulation

4.7 Load Transient Response

The TPS54429EEVM-608 response to load transient is shown in Figure 4-5. The current step is from 1.25 A to 3.25 A. Total peak-to-peak output voltage variation is as shown.

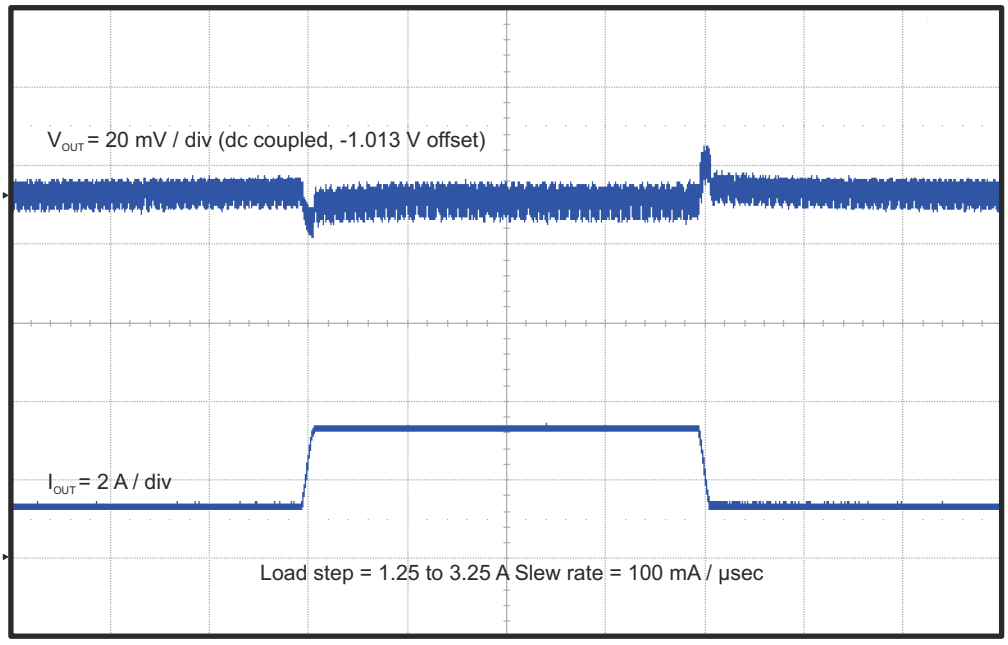

Figure 4-5. TPS54429EEVM-608 Load Transient Response

4.8 Output Voltage Ripple

The TPS54429EEVM-608 output voltage ripple is shown in Figure 4-6. The output current is the rated full load of 4.5 A.

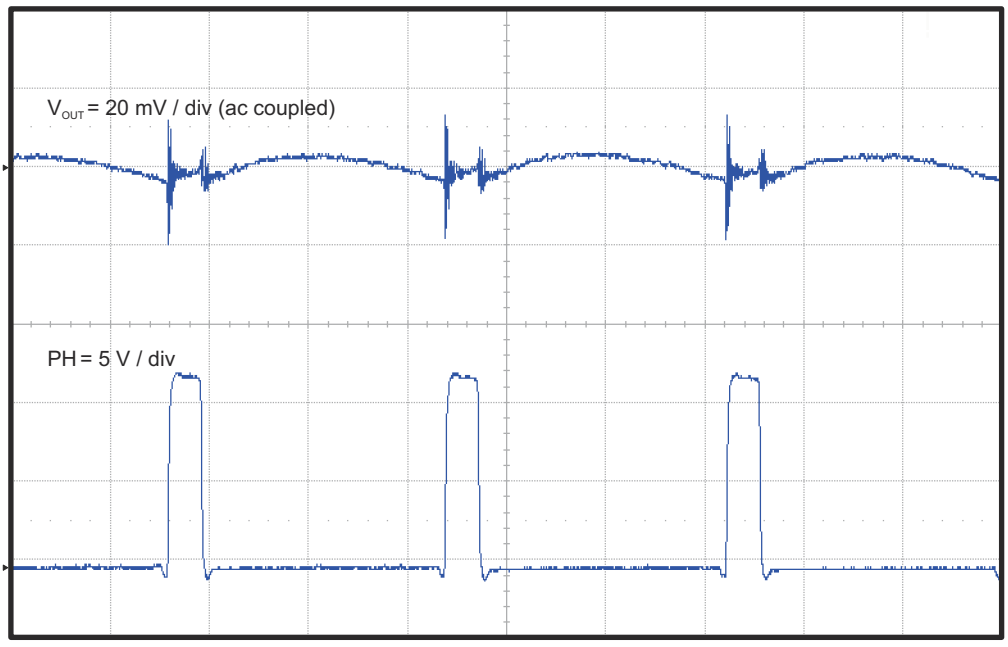

Figure 4-6. TPS54429EEVM-608 Output Voltage Ripple

4.9 Input Voltage Ripple

The TPS54429EEVM-608 input voltage ripple is shown in Figure 4-7. The output current is the rated full load of 4.5 A.

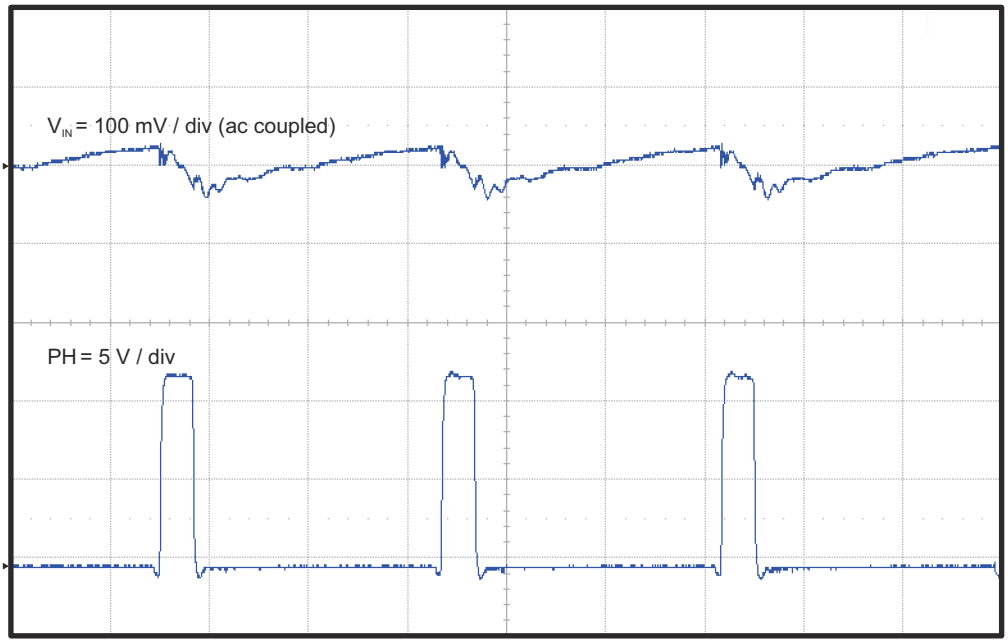

Figure 4-7. TPS54429EEVM-608 Input Voltage Ripple

4.10 Start-Up

The TPS54429EEVM-608 start-up waveform relative to V_{IN} is shown in Figure 4-8.

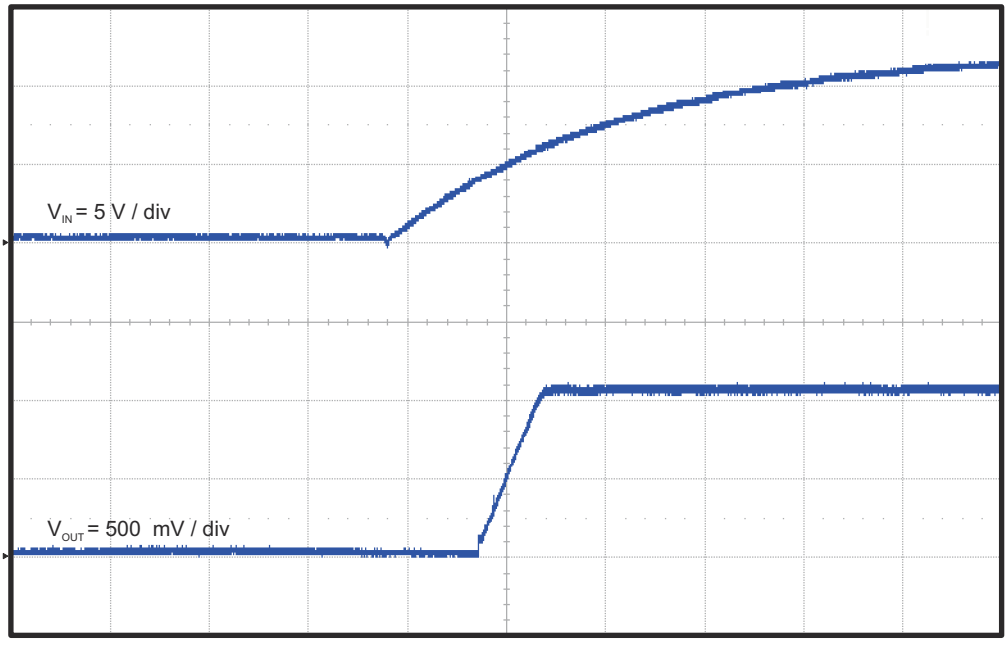

Figure 4-8. TPS54429EEVM-608 Start-Up

The TPS54429EEVM-608 start-up waveform relative to enable (EN) is shown in Figure 5-1.

4.11 Eco-mode™ Operation

The waveforms Figure 5-2, Figure 5-3 and Figure 5-4in show the Eco-mode™ operation of the TPS54429E. In Figure 5-2, the circuit is switching normally with the inductor current always positive.

5 Test Setup and Results

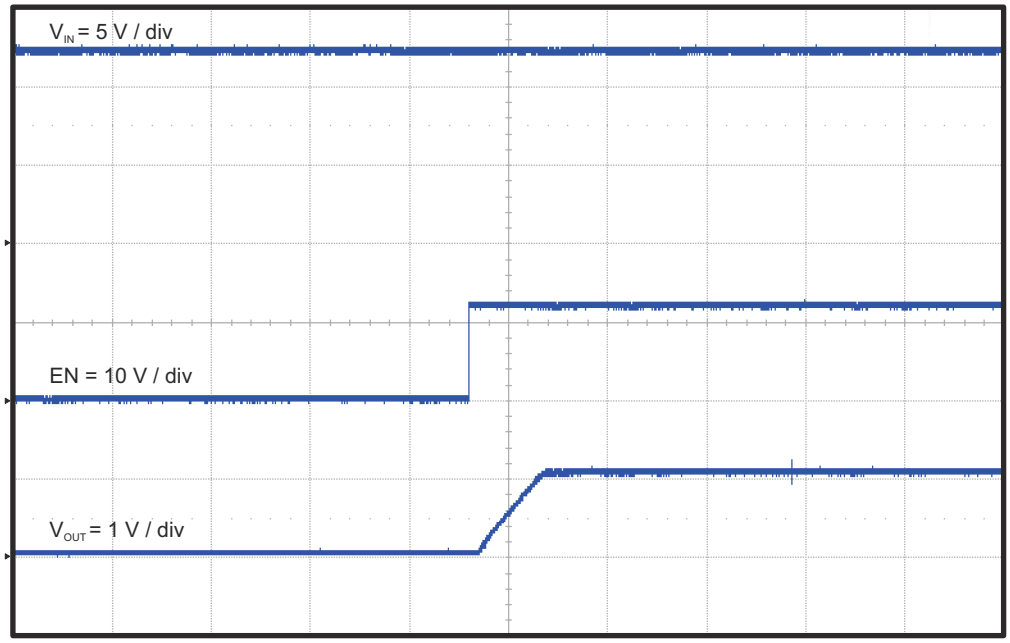

Figure 5-1. TPS54429EEVM-608 Start-Up Relative to Enable

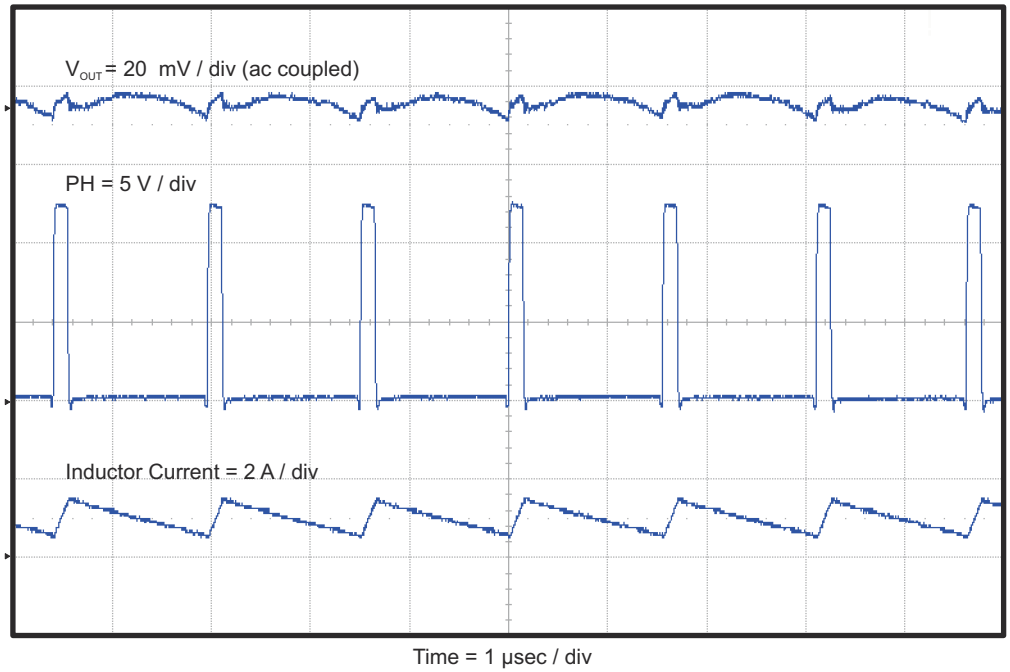

Figure 5-2. TPS54329EEVM-608 Normal Switching

When the inductor current falls to zero, Eco-mode™ operation begins. The TPS54329E enters a power-saving skip mode. Switching resumes when the fedback voltage at VFB falls below an internally set threshold. Figure 5-3 shows the switching activity as the circuit is just entering Eco-mode™ operation. The effective switching period increases slightly as the pulse-skipping time is short.

In Figure 5-4, the load current is reduced further, and the skip time is longer.

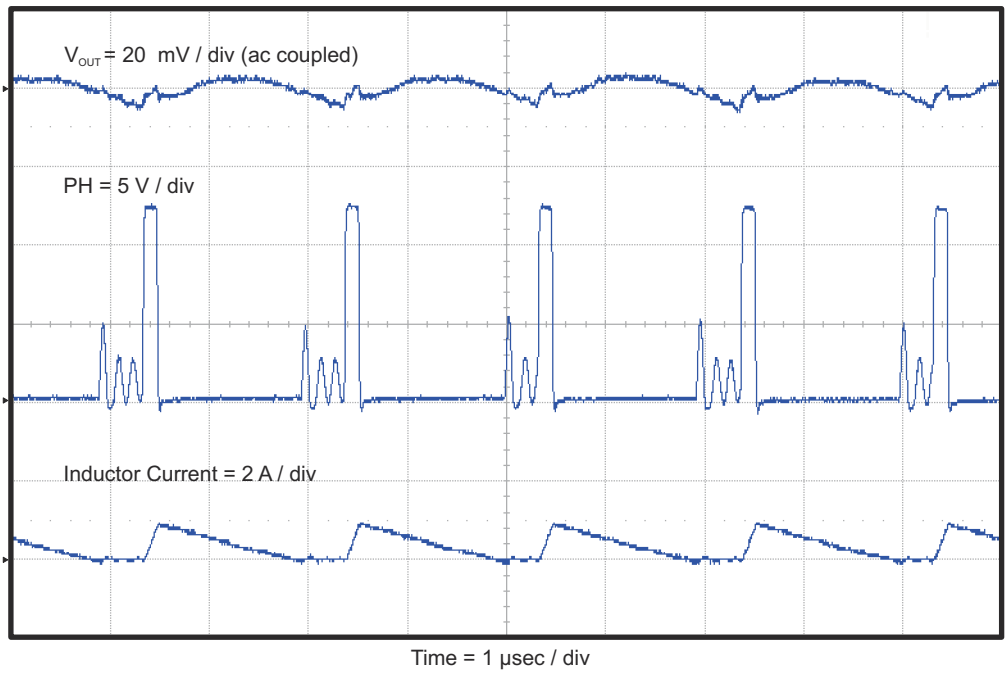

Figure 5-3. TPS54429EEVM-608 Entering Eco-mode™ Operation

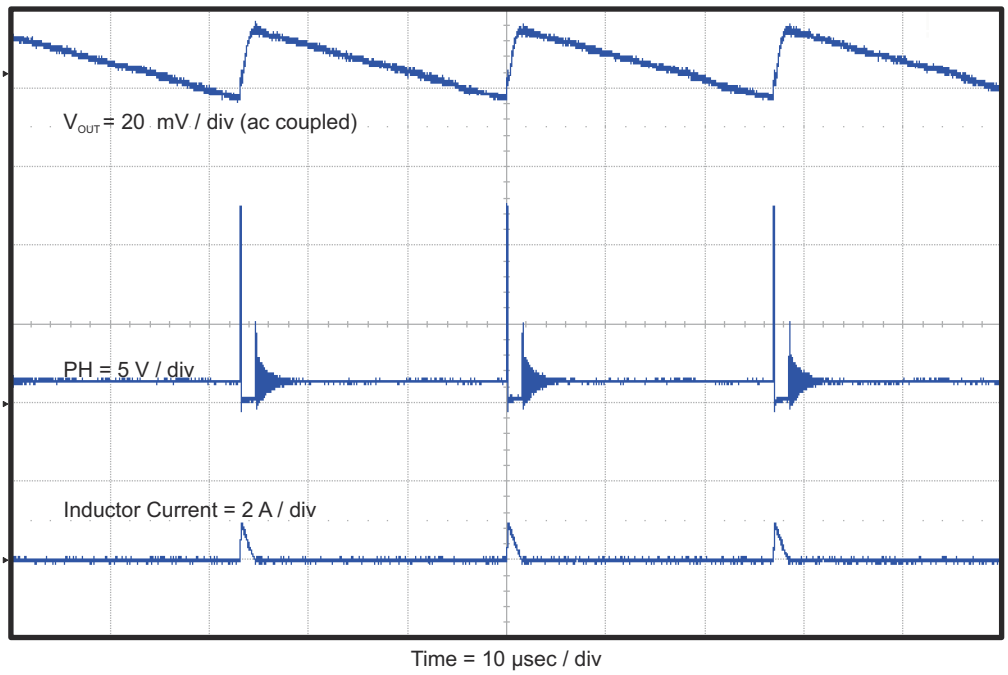

Figure 5-4. TPS54429EEVM-608 Fully in Eco-mode™ Operation

6 Board Layout

This section provides description of the TPS54429EEVM-608, board layout, and layer illustrations.

6.1 Layout

The board layout for the TPS54429EEVM-608 and is shown in Figure 6-1 through Figure 6-6. The top layer contains the main power traces for VIN, VO, and ground. Also on the top layer are connections for the pins of the TPS54429E and a large area filled with ground. Most of the signal traces are also located on the top side. The input decoupling capacitor are located as close to the integrated circuit as possible. The input and output connectors, test points, and most of the components are located on the top side. R4, the power-good pullup, is located on the back side. Analog ground and power ground are connected at a single point on the top layer near pin 5 of the TPS54429E. The internal layer 1 is a split plane containing analog and power grounds. The internal layer 2 is primarily power ground. Also, a fill area of VIN and a trace routing VIN enables the control jumper JP1. The bottom layer is primarily analog ground. Traces also connect VIN, the power-good signal, and a feedback trace from VOUT connects to the voltage setpoint divider network.

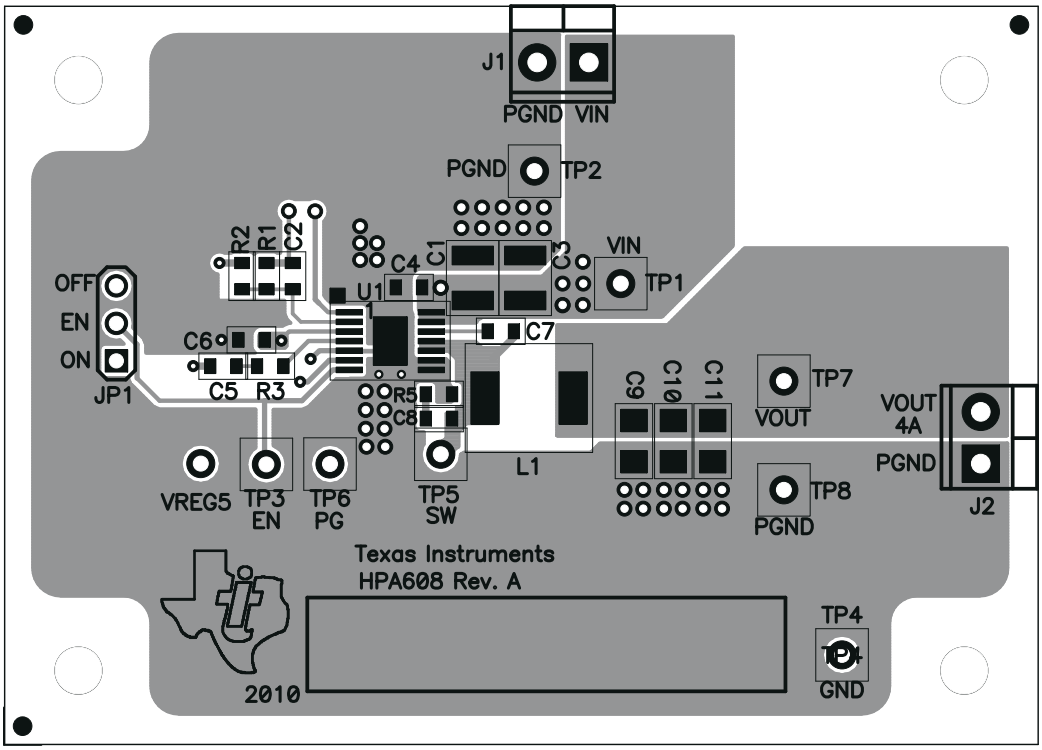

Figure 6-1. Top Assembly

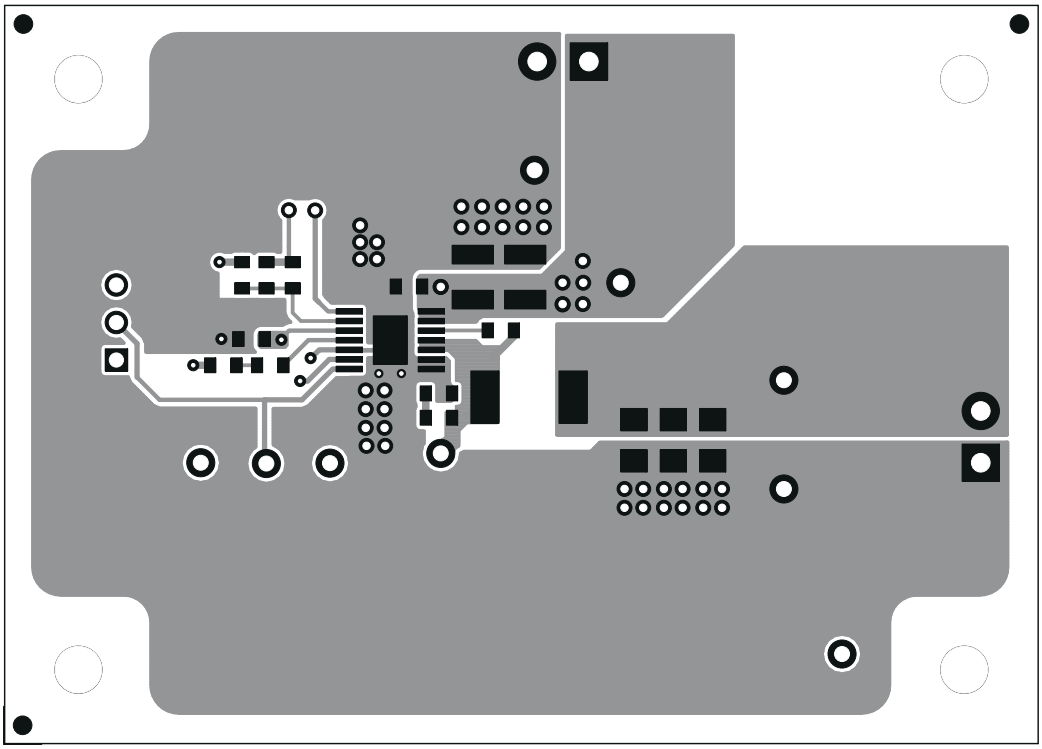

Figure 6-2. Top Layer

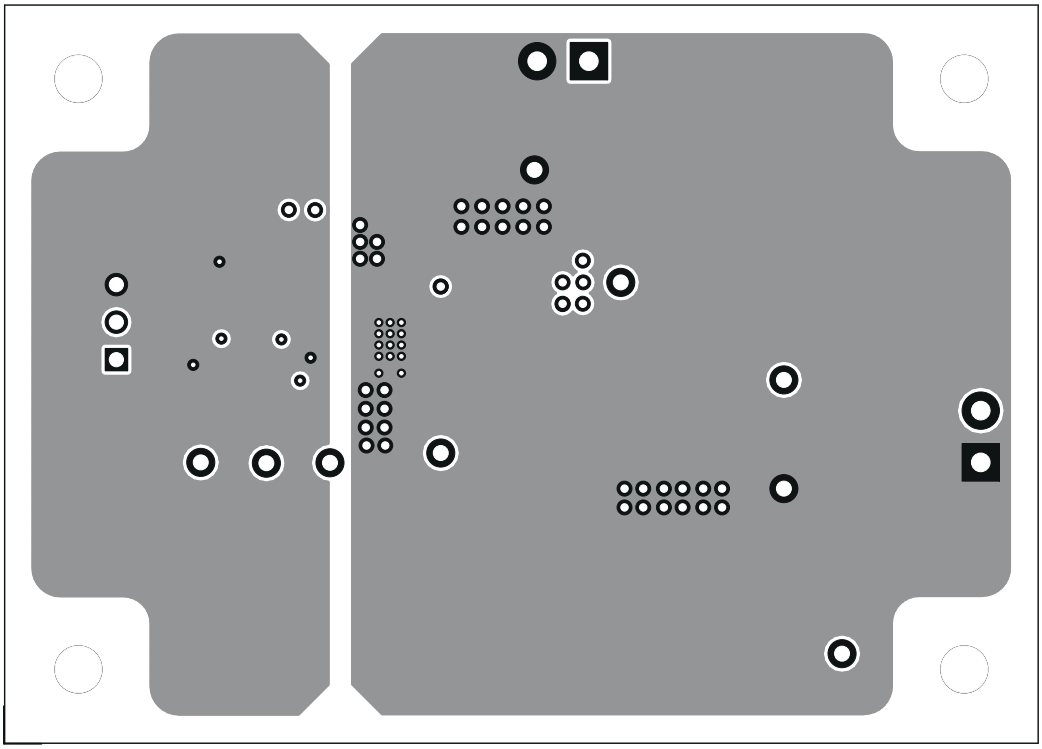

Figure 6-3. Internal Layer 1

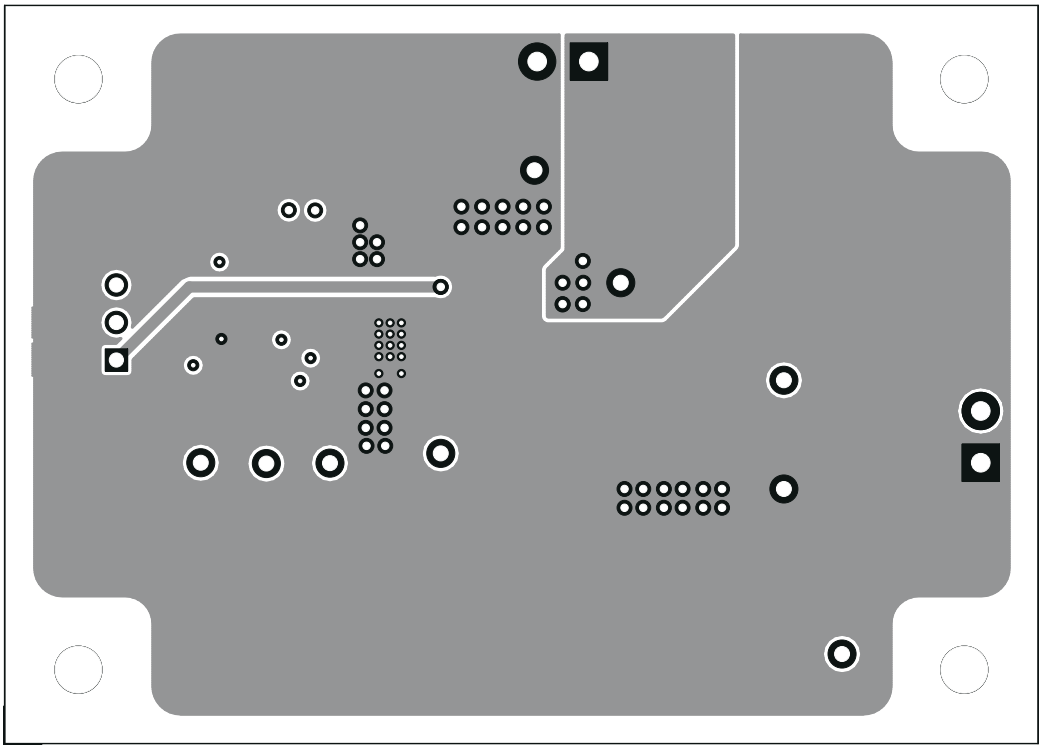

Figure 6-4. Internal Layer 2

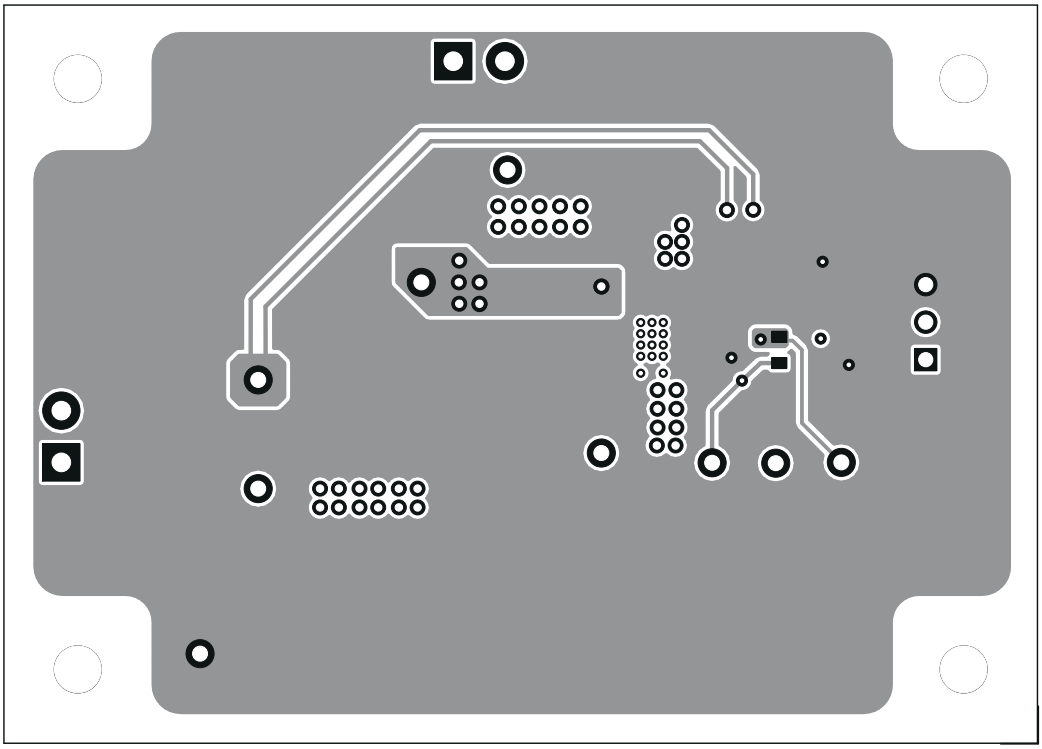

Figure 6-5. Bottom Layer as Seen From Back Side

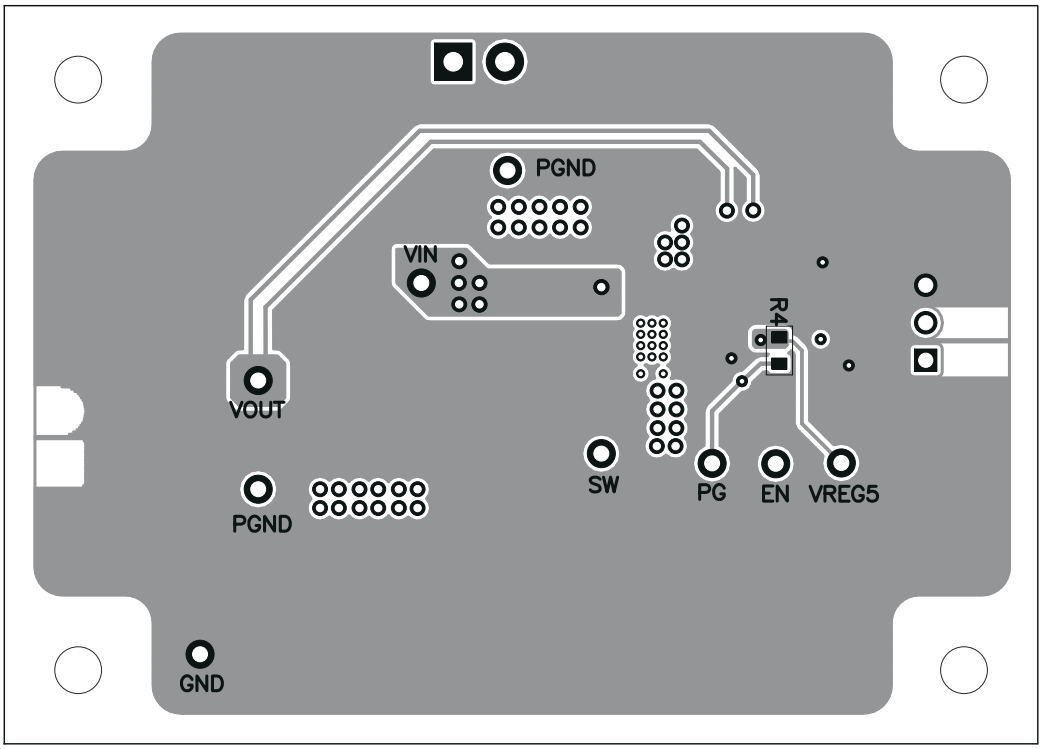

Figure 6-6. Bottom Assembly as Seen From Back Side

7 Schematic, Bill of Materials, and Reference

This section presents the TPS54429EEVM-608 schematic, bill of materials, and reference.

7.1 Schematic

Figure 7-1 is the schematic for the TPS54429EEVM.

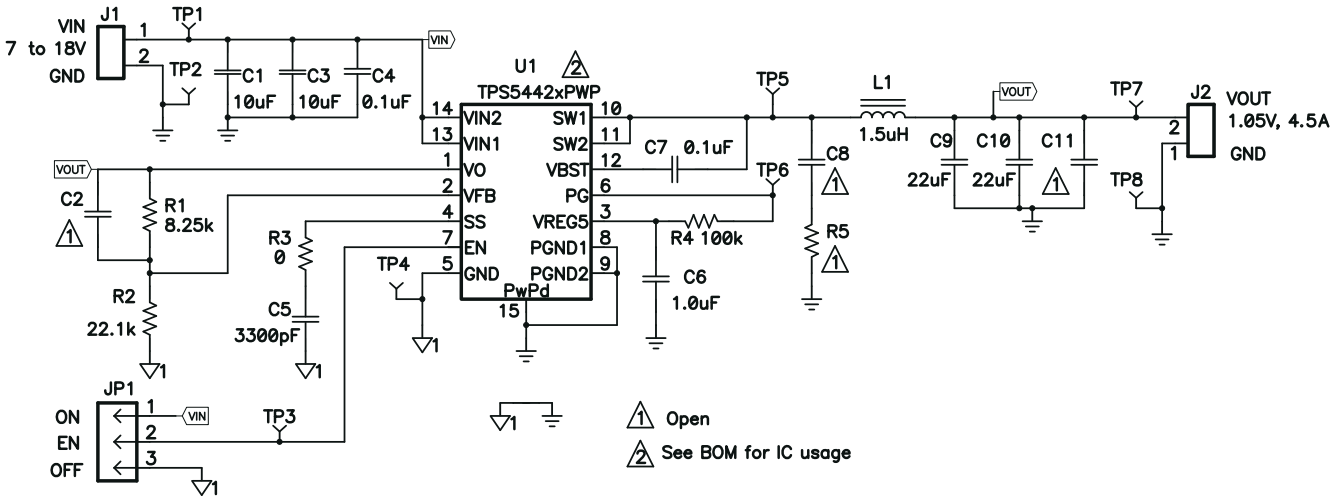

Figure 7-1. TPS54429EEVM-608 Schematic Diagram

7.2 Bill of Materials

Table 7-1. Bill of Materials

RefDes	QTY	Value	Description	Size	Part Number	MFR
C1, C3	2	10uF	Capacitor, Ceramic, 25V, X5R, 20%	1210	C3225X5R1E106M	TDK
C11	0	Open	Capacitor, Ceramic	1206	Std	Std
C2, C8	0	Open	Capacitor, Ceramic	0603	Std	Std
C4, C7	2	0.1uF	Capacitor, Ceramic, 50V, X7R, 10%			
C5	1	3300pF	Capacitor, Ceramic, 25V, X7R , 10%	0603	Std	Std
C6	1	1.0uF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
C9, C10	2	22uF	Capacitor, Ceramic, 6.3V, X5R, 20%	1206	C3216X5R0J226M	TDK
J1, J2	2	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED555/2DS	Sullins
JP1	1	PEC03SAAN	Header, Male 3-pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
L1	1	1.5uH	Inductor, SMT, 11A, 9.7 milliohm	0.256 x 0.280 inch	SPM6530T-1R5M100	TDK
R1	1	8.25k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R2	1	22.1k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R3	1	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R4	1	100k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
R5	0	Open	Resistor, Chip, 1/16W, 1%	0603	Std	Std
TP1, TP3, TP5, TP6, TP7	5	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
TP2, TP5, TP8	3	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
U1	1	TPS54429EPWP	IC, 4.5-A Output Single Sync. Step-Down		TPS54429EPWP	TI
–	1		Shunt, 100-mil, Black	0.100	929950-00	3M
–	1		PCB, 2.76 In x 1.97 In x 0.062 In		HPA608	Any

7.3 Reference

Texas Instruments, *TPS54429E, 7V to 18V Input, 4.5-A Synchronous Step-Down SWIFT™ Converter with Eco-Mode™ Data Sheet*

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2011) to Revision A (August 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	3
• Updated the user's guide title.	3

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