TSDxxC Bidirectional TVS Diodes in SOD-323 Package

1 Features

- IEC 61000-4-2 ESD protection:
  - ±30kV contact discharge
  - ±30kV air gap discharge
- IEC 61000-4-5 surge protection:
  - 6.5-30A (8/20μs)
- Low IO capacitance < 7pF (typical)
- Ultra low leakage current: 10nA (maximum)
- Industrial temperature range: –55°C to +150°C
- Industry standard SOD-323 leaded package (2.65mm × 1.3mm)

2 Applications

- I/O Protection
- Power Line Protection
- USB VBUS
- Appliances
- Medical & Healthcare
- Retail Automation

3 Description

The TSDxxC are a family of bidirectional TVS protection diodes designed for clamping harmful transients such as ESD and surge. The TSDxxC devices are rated to dissipate ESD strikes up to ±30kV (contact and air gap discharge) which exceeds the maximum level specified in the IEC 61000-4-2 international standard (Level 4).

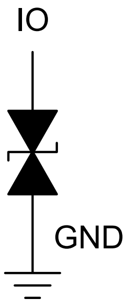
Combining the robust clamping performance and low capacitance of these devices, TSDxxC are excellent TVS diodes to protect both data lines and power lines in many different applications.

The TSDxxC family is offered in the industry standard, leaded SOD-323 package to enable easy solderability.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
TSDxxC	DYF (SOD-323, 2)	2.65mm × 1.3mm

(1) For more information, see Section 9.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram

Table of Contents

4 Pin Configuration and Functions

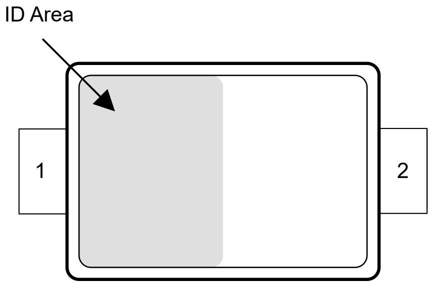


Figure 4-1. DYF Package, 2-Pin SOD-323 (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	IO	I/O	Protected Channel. If used as IO, connect pin 2 to ground
2	IO	I/O	Protected Channel. If used as IO, connect pin 1 to ground

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

Parameter		DEVICE	MIN	MAX	UNIT
P_{PP}	IEC 61000-4-5 (t_p 8/20µs) Peak Pulse Power at 25°C	TSD05C		400	W
P_{PP}	IEC 61000-4-5 (t_p 8/20µs) Peak Pulse Power at 25°C	TSD12C		390	W
		TSD15C			
		TSD18C			
		TSD24C			
		TSD36C		400	W
I_{PP}	IEC 61000-4-5 (t_p 8/20µs) Peak Pulse Current at 25°C	TSD05C		30	A
I_{PP}	IEC 61000-4-5 (t_p 8/20µs) Peak Pulse Current at 25°C	TSD12C		15	A
		TSD15C		12	A
		TSD18C			
		TSD24C		9	A
		TSD36C		6.5	A
T_A	Ambient Operating Temperature		-55	150	°C
T_{stg}	Storage Temperature		-65	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings—JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001 (1)	±2500	V
		Charged device model (CDM), per JEDEC specification JS-002 (2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufactuuring with a standard ESD control proccess
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufactuuring with a standard ESD control proccess.

5.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±30000	V
		IEC 61000-4-2 air-gap discharge	±30000	

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Operating free-air temperature	-55		150	°C

5.5 Thermal Information

THERMAL METRIC (1)		TSD05C	TSD12C / TSD15C / TSD18C	TSD24C / TSD36C	UNIT
		DYF (SOD-323)	DYF (SOD-323)	DYF (SOD-323)	
		2 PINS	2 PINS	2 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	672.0	683.8	686.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	230.5	264.2	267.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	541.4	559.0	560.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	64.4	89.9	91.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	527.5	544.8	546.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Electrical Characteristics - TSD05C

At TA=25℃ (unless otherwise noted) (1)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} <50 nA, across operating temperature range	-5.5		5.5	V
V_{BR}	Break-down voltage	I_{IO} = 1 mA, IO to GND and GND to IO	7	8	9	V
I_{LEAK}	Reverse leakage current	V_{IO} = 5.5 V, IO to GND or GND to IO		5	10	nA
V_{CLAMP}	Surge clamping voltage, t_p = 8/20 µs (2)	I_{PP} = 24 A, IO to GND or GND to IO		10.7	13.8	V
		I_{PP} = 30 A, IO to GND or GND to IO		11.5	15	V
	TLP clamping voltage, t_p = 100 ns	I_{PP} = 16 A, IO to GND or GND to IO		9.3		V
R_{DYN}	Dynamic resistance (3)	IO to GND		0.15		Ω
		GND to IO				
C_L	Line capacitance	V_{IO} = 0 V; f = 1 MHz, IO to GND		4	7	pF

(1) Typical parameters are measured at 25℃
(2) Nonrepetitive current pulse 8 to 20 µs exponentially decaying waveform according to IEC 61000-4-5
(3) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10 A and I = 20 A

5.7 Electrical Characteristics - TSD12C

At TA=25℃ (unless otherwise noted) (1)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} <10 nA, across operating temperature range			12	V
V_{BRR}	Breakdown voltage	I_{IO} = 10 mA, IO to GND and GND to IO	13.2	15.6	19	V
I_{LEAK}	Reverse leakage current	V_{IO} = 12 V, IO to GND or GND to IO		5	10	nA
V_{CLAMP}	Surge clamping voltage, t_p = 8/20 µs (2)	I_{PP} = 1 A, IO to GND or GND to IO			18.5	V
		I_{PP} = 5 A, IO to GND or GND to IO			21	V
		I_{PP} = 15 A, IO to GND or GND to IO			26	V
	TLP clamping voltage, t_p = 100 ns	I_{PP} = 16 A, IO to GND or GND to IO		19.4		V
R_{DYN}	Dynamic resistance(3)	IO to GND		0.15		Ω
		GND to IO				
C_L	Line capacitance	V_{IO} = 0 V; ƒ = 1 MHz, IO to GND		6.5	8	pF

(1) Typical parameters are measured at 25℃
(2) Nonrepetitive current pulse 8 to 20 µs exponentially decaying waveform according to IEC 61000-4-5
(3) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10 A and I = 20 A

5.8 Electrical Characteristics - TSD15C

At TA=25℃ (unless otherwise noted) (1)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} <10 nA, across operating temperature range			15	V
V_{BRR}	Breakdown voltage	I_{IO} = 10 mA, IO to GND and GND to IO	19	22	25	V
I_{LEAK}	Reverse leakage current	V_{IO} = 15 V, IO to GND or GND to IO		5	10	nA
V_{CLAMP}	Surge clamping voltage, t_p = 8/20 µs (2)	I_{PP} = 1 A, IO to GND or GND to IO			25.6	V
		I_{PP} = 5 A, IO to GND or GND to IO			28	V
		I_{PP} = 12 A, IO to GND or GND to IO			33	V
	TLP clamping voltage, t_p = 100 ns	I_{PP} = 16 A, IO to GND or GND to IO		25		V
R_{DYN}	Dynamic resistance(3)	IO to GND		0.2		Ω
		GND to IO				
C_L	Line capacitance	V_{IO} = 0 V; f = 1 MHz, IO to GND		6.7	9	pF

(1) Typical parameters are measured at 25℃
(2) Nonrepetitive current pulse 8 to 20 µs exponentially decaying waveform according to IEC 61000-4-5
(3) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10 A and I = 20 A

5.9 Electrical Characteristics - TSD18C

At TA=25℃ (unless otherwise noted) (1)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} <10 nA, across operating temperature range			18	V
V_{BRR}	Breakdown voltage	I_{IO} = 10 mA, IO to GND and GND to IO	19	22	25	V
I_{LEAK}	Reverse leakage current	V_{IO} = 18 V, IO to GND or GND to IO		5	10	nA
V_{CLAMP}	Surge clamping voltage, t_p = 8/20 µs (2)	I_{PP} = 1 A, IO to GND or GND to IO			25.6	V
		I_{PP} = 5 A, IO to GND or GND to IO			28	V
		I_{PP} = 12 A, IO to GND or GND to IO			33	V
	TLP clamping voltage, t_p = 100 ns	I_{PP} = 16 A, IO to GND or GND to IO		25		V
R_{DYN}	Dynamic resistance(3)	IO to GND		0.2		Ω
		GND to IO				
C_L	Line capacitance	V_{IO} = 0 V; f = 1 MHz, IO to GND		6.7	9	pF

(1) Typical parameters are measured at 25℃
(2) Nonrepetitive current pulse 8 to 20 µs exponentially decaying waveform according to IEC 61000-4-5
(3) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10 A and I = 20 A

5.10 Electrical Characteristics - TSD24C

At TA=25℃ (unless otherwise noted) (1)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} <10 nA, across operating temperature range			24	V
V_{BR}	Breakdown voltage	I_{IO} = 10 mA, IO to GND and GND to IO	25.5	30.5	35.5	V
I_{LEAK}	Reverse leakage current	V_{IO} = 24 V, IO to GND or GND to IO		5	10	nA
V_{CLAMP}	Surge clamping voltage, t_p = 8/20 µs (2)	I_{PP} = 1 A, IO to GND or GND to IO			34	V
		I_{PP} = 5 A, IO to GND or GND to IO			43	V
		I_{PP} = 9 A, IO to GND or GND to IO			50	V
	TLP clamping voltage, t_p = 100 ns	I_{PP} = 16 A, IO to GND or GND to IO		36		V
R_{DYN}	Dynamic resistance(3)	IO to GND		0.35		Ω
		GND to IO				
C_L	Line capacitance	V_{IO} = 0 V; f = 1 MHz, IO to GND		4.3	6	pF

(1) Typical parameters are measured at 25℃
(2) Nonrepetitive current pulse 8 to 20 µs exponentially decaying waveform according to IEC 61000-4-5
(3) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10 A and I = 20 A

5.11 Electrical Characteristics - TSD36C

At TA=25℃ (unless otherwise noted) (1)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} <50 nA, across operating temperature range			36	V
V_{BR}	Breakdown voltage	I_{IO} = 10 mA, I/O to GND and GND to I/O	37.8	41.2	44.2	V
I_{LEAK}	Reverse leakage current	V_{IO} = 36 V, IO to GND or GND to IO		5	10	nA
V_{CLAMP}	Surge clamping voltage, t_p = 8/20 µs (2)	I_{PP} = 1 A, IO to GND or GND to IO			47	V
		I_{PP} = 5 A, IO to GND or GND to IO			64	V
		I_{PP} = 6.5 A, IO to GND or GND to IO			71	V
	TLP clamping voltage, t_p = 100 ns	I_{PP} = 16 A, IO to GND or GND to IO		56		V
R_{DYN}	Dynamic resistance (3)	IO to GND		0.6		Ω
		GND to IO				
C_L	Line capacitance	V_{IO} = 0 V; ƒ = 1 MHz, IO to GND		4.3	6	pF

(1) Typical parameters are measured at 25℃
(2) Nonrepetitive current pulse 8 to 20 µs exponentially decaying waveform according to IEC 61000-4-5
(3) Extraction of RDYN using least squares fit of TLP characteristics between I = 10 A and I = 20 A

5.12 Typical Characteristics

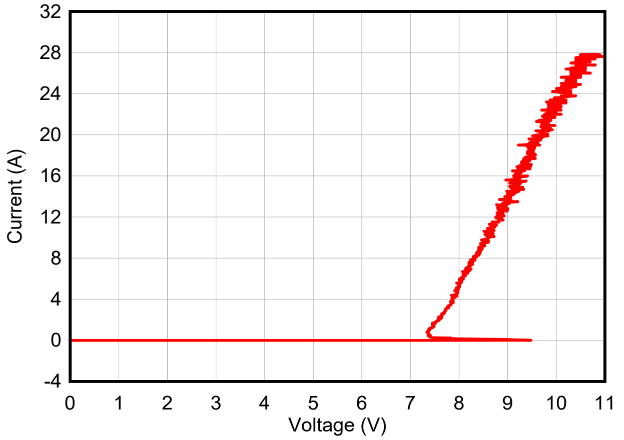


Figure 5-1. Positive TLP Curve - TSD05C

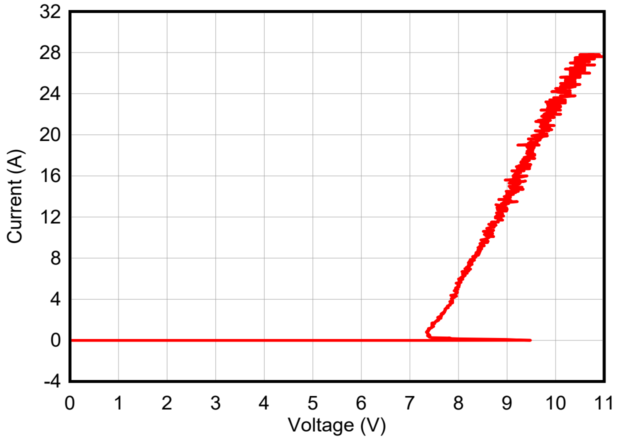


Figure 5-2. Negative TLP Curve - TSD05C

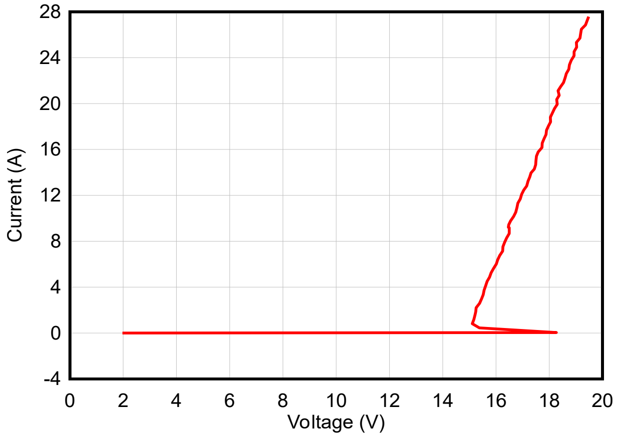


Figure 5-3. Positive TLP Curve - TSD12C

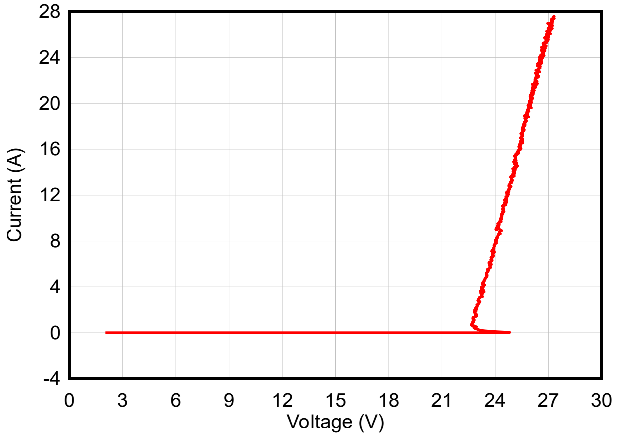


Figure 5-4. Positive TLP Curve - TSD15C

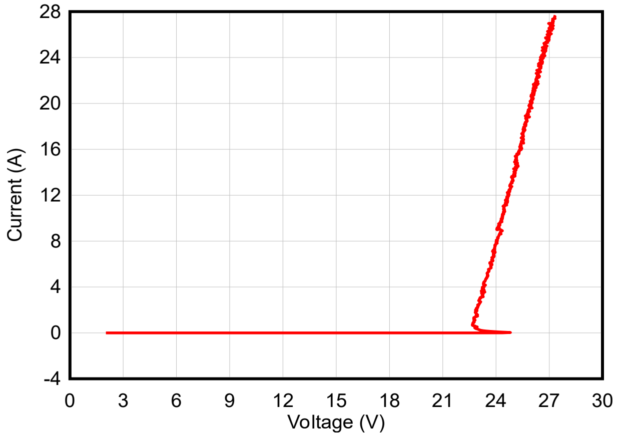


Figure 5-5. Positive TLP Curve - TSD18C

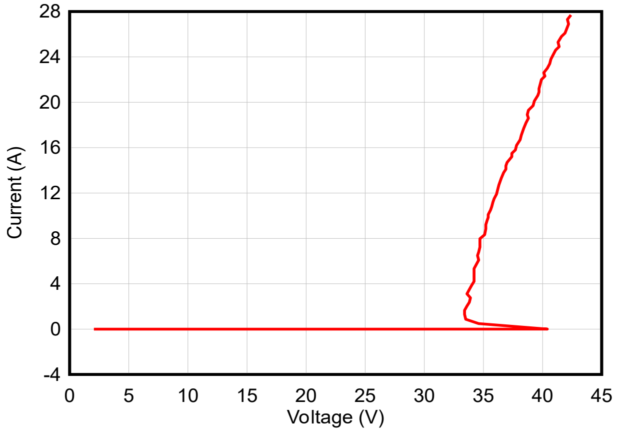


Figure 5-6. Positive TLP Curve - TSD24C

5.12 Typical Characteristics (continued)

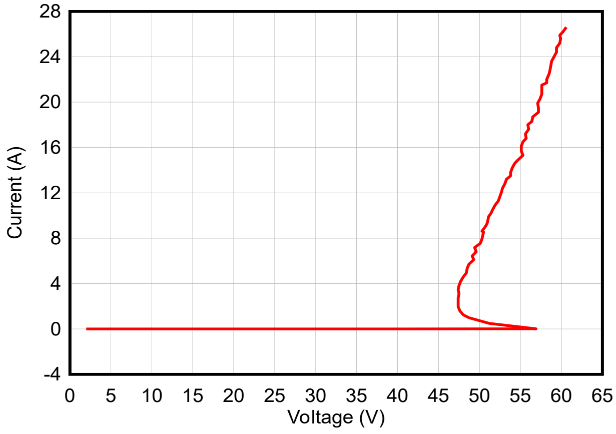


Figure 5-7. Positive TLP Curve - TSD36C

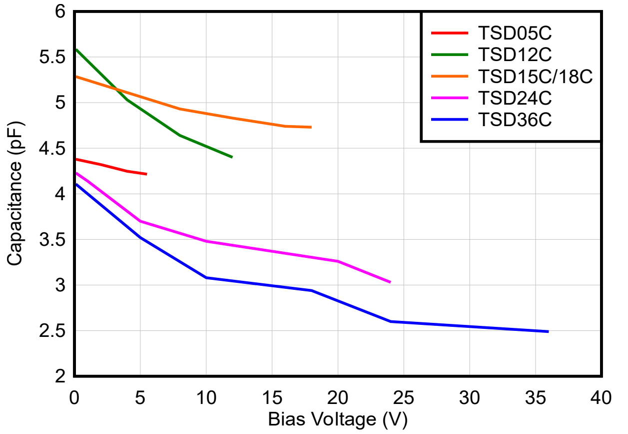


Figure 5-8. Capacitance vs Bias Voltage

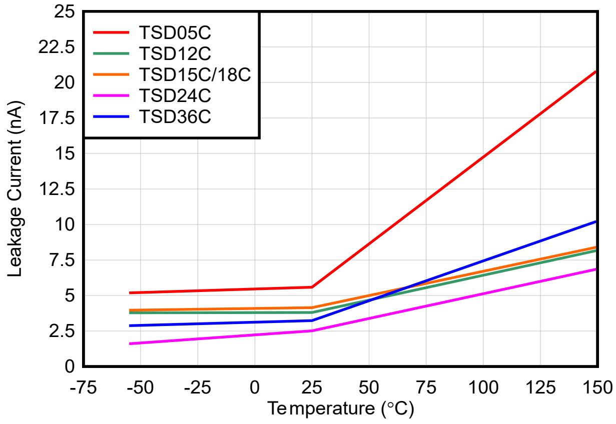


Figure 5-9. Leakage Current vs Temperature

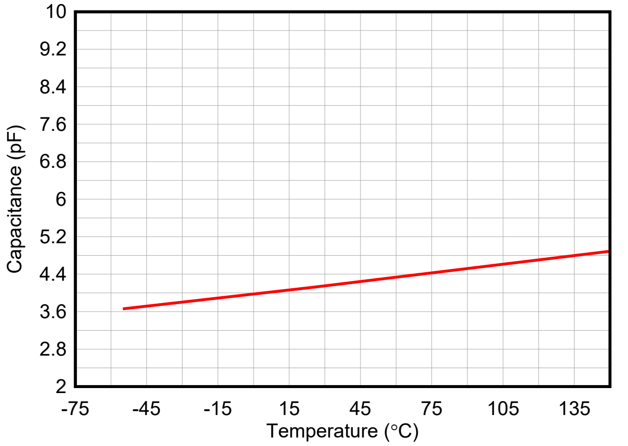


Figure 5-10. Capacitance vs Temperature - TSD05C

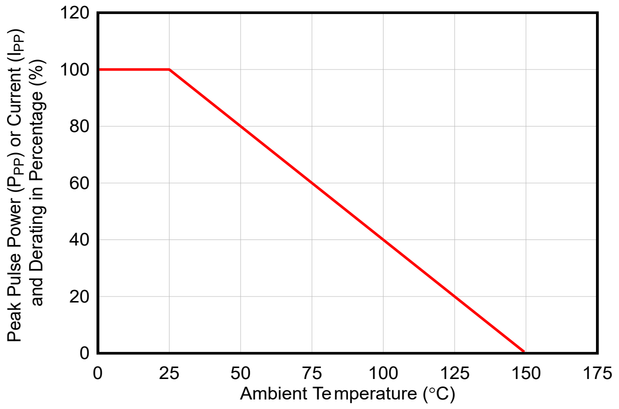


Figure 5-11. Peak Pulse Power Derating Curve

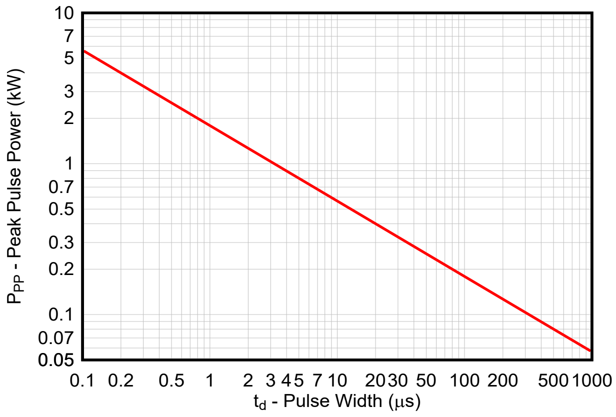


Figure 5-12. Pulse Power Rating Curve

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The TSDxxC are TVS diodes that provide a path to ground for dissipating transient voltage spikes (such as ESD or surge) on signal lines and power lines. Connect the device in parallel to the down stream circuitry for protection. As the current from the transient passes through the TVS, only a small voltage drop is present across the diode. The small voltage drop is presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC. For more information on how to properly use this device, refer to the *ESD Packaging and Layout Guide*.

7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Packaging and Layout Guide* application reports
- Texas Instruments, *ESD Layout Guide* application reports
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2024) to Revision C (October 2024)	Page
• Added TSD12C, TSD15C, TSD18C, and TSD24C to the data sheet	1

Changes from Revision A (July 2023) to Revision B (July 2024)	Page
• Added TSD36C to the data sheet	1
• Changed the status of the data sheet from: *Advanced Information* to: *Production Data*	1

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSD05CDYFR	ACTIVE	SOT	DYF	2	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	33KF	Samples
TSD12CDYFR	ACTIVE	SOT	DYF	2	3000	RoHS & Green	SN	Level-3-260C-168 HR	-55 to 150	3JMF	Samples
TSD15CDYFR	ACTIVE	SOT	DYF	2	3000	RoHS & Green	SN	Level-3-260C-168 HR	-55 to 150	3MLF	Samples
TSD18CDYFR	ACTIVE	SOT	DYF	2	3000	RoHS & Green	SN	Level-3-260C-168 HR	-55 to 150	3JQF	Samples
TSD24CDYFR	ACTIVE	SOT	DYF	2	3000	RoHS & Green	SN	Level-3-260C-168 HR	-55 to 150	3GWF	Samples
TSD36CDYFR	ACTIVE	SOT	DYF	2	3000	RoHS & Green	SN	Level-3-260C-168 HR	-55 to 150	3GNF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TSD12C, TSD15C, TSD18C, TSD24C :

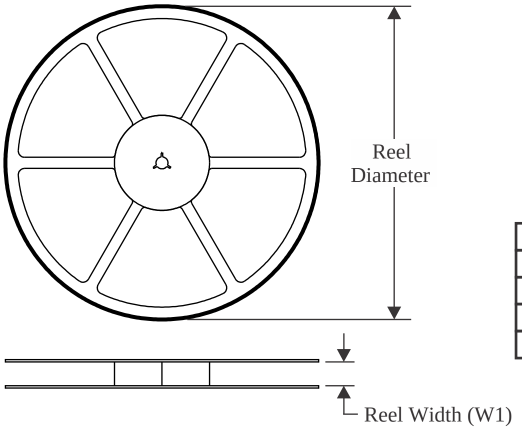
- Automotive : TSD12C-Q1, TSD15C-Q1, TSD18C-Q1, TSD24C-Q1

NOTE: Qualified Version Definitions:

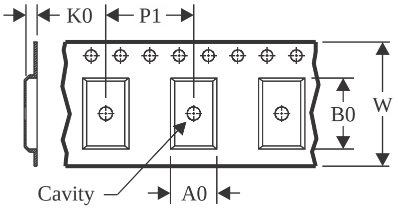
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

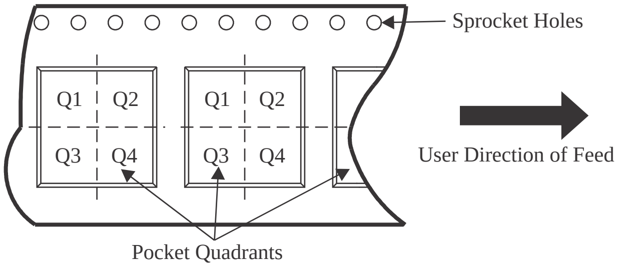


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

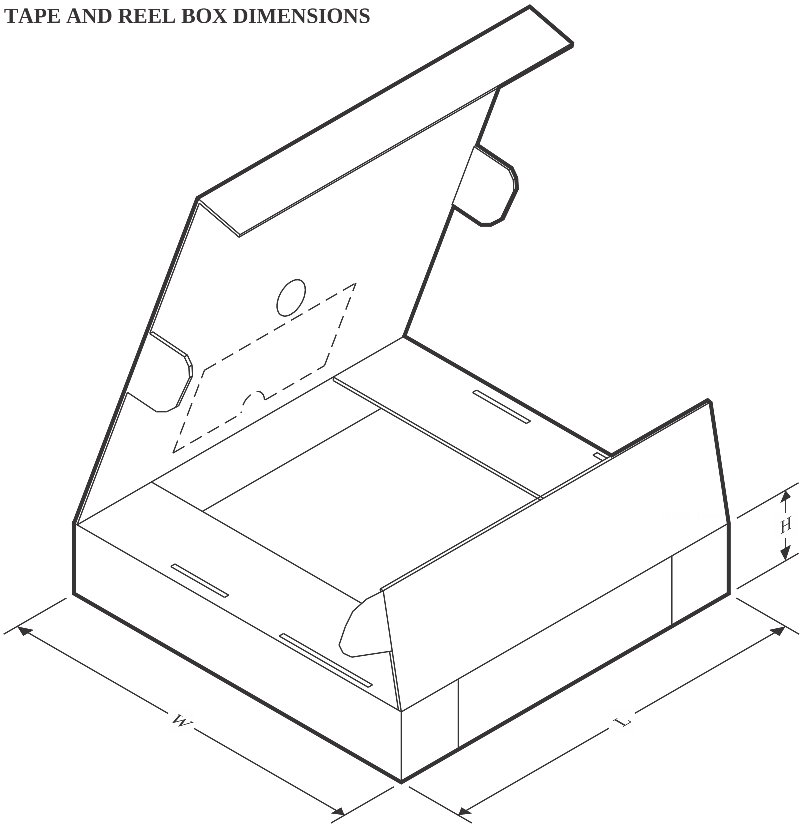
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSD05CDYFR	SOT	DYF	2	3000	178.0	9.5	1.48	3.3	1.25	4.0	8.0	Q1
TSD12CDYFR	SOT	DYF	2	3000	178.0	9.5	1.48	3.3	1.25	4.0	8.0	Q1
TSD15CDYFR	SOT	DYF	2	3000	178.0	9.5	1.48	3.3	1.25	4.0	8.0	Q1
TSD18CDYFR	SOT	DYF	2	3000	178.0	9.5	1.48	3.3	1.25	4.0	8.0	Q1
TSD24CDYFR	SOT	DYF	2	3000	178.0	9.5	1.48	3.3	1.25	4.0	8.0	Q1
TSD36CDYFR	SOT	DYF	2	3000	178.0	9.5	1.48	3.3	1.25	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

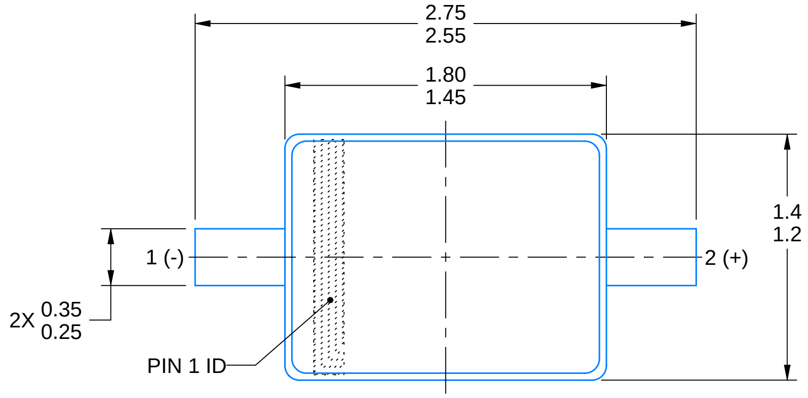
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSD05CDYFR	SOT	DYF	2	3000	210.0	200.0	42.0
TSD12CDYFR	SOT	DYF	2	3000	210.0	200.0	42.0
TSD15CDYFR	SOT	DYF	2	3000	210.0	200.0	42.0
TSD18CDYFR	SOT	DYF	2	3000	210.0	200.0	42.0
TSD24CDYFR	SOT	DYF	2	3000	210.0	200.0	42.0
TSD36CDYFR	SOT	DYF	2	3000	210.0	200.0	42.0

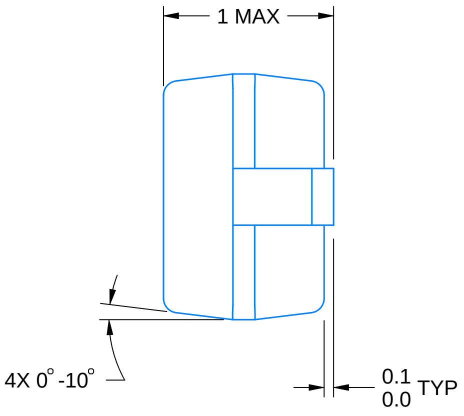
DYF0002A

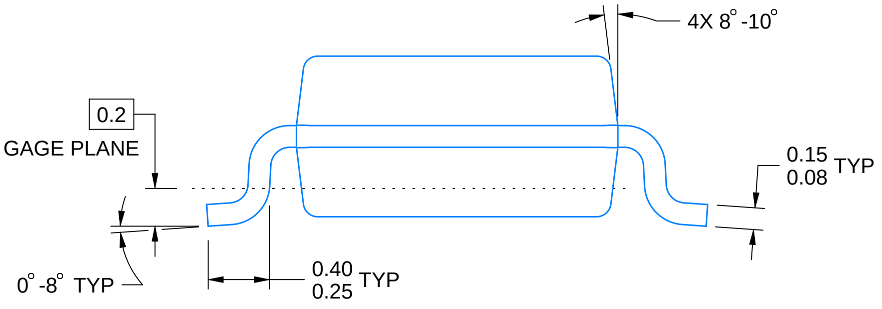
PACKAGE OUTLINE

SOT(SOD-323) - 1 mm max height

SMALL OUTLINE TRANSISTOR

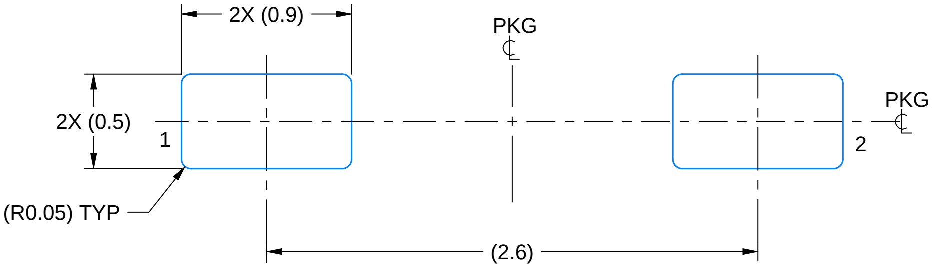




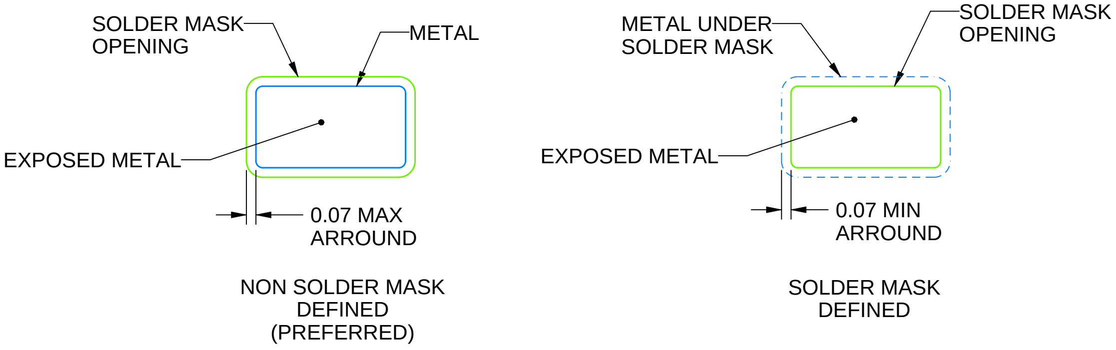


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

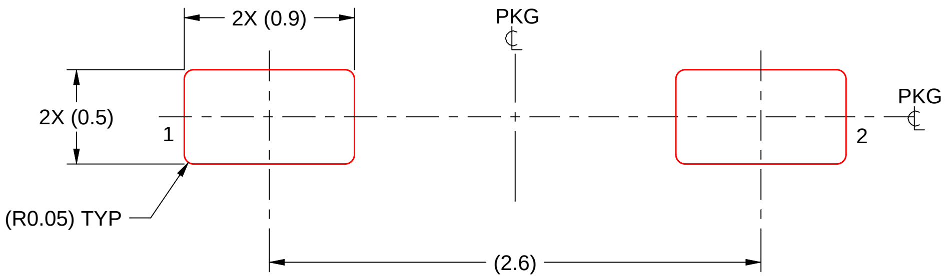


SOLDER MASK DETAILS

4228484/C 12/2024

NOTES: (continued)

3. Publication IPC-7351 may have alternate designs.
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:25X

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
6. Board assembly site may have different recommendations for stencil design.

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